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Original Article

Design of Ultra-Low-Power, Wide-Band Operational Amplifier Using the Programmable MOS Devices

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Abstract *- This paper presents a new approach for designing an ultra-low power, two-stage, rail-to-rail CMOS operational amplifier operating with a dual power supply of ±0.1V using an electrical programming technique. A self-compensation technicality instead of an external compensation capacitor has been used in this work to gain higher bandwidth with guaranteed stability. In addition to using the self-compensation technique, the constant transconductance technique across the common-mode input range was used to achieve full output swing. The operational amplifier has recorded a DC gain of 136dB and a unity gain bandwidth of 4.2GHz with a phase margin of 41° and power consumption of 5.39µW. Due to using Electrically Programmed MOSFETs (EPMOSFETs) that featured perfect matching, along with the use of current sources that are independent of the power supply voltage and temperature, the operational amplifier has recorded a common-mode rejection ratio of 200dB, with a 228dB rejection ratio of power supply.*

Keywords *- Op Amp, Low power, Self compensation, Constant transconductance, Electrical programming technology.*

1. Introduction

In the design of an op-amp, the lower the supply voltage, the better because with the supply voltage, or input bias current, lowered, the power consumption reduces without compromising the speed performance. However, reducing the input bias current leads to the degraded dynamic range of output swing, and reducing the supply voltage leads to difficulty in keeping transistors in a saturation condition. Thus, there are various issues associated with lowering the supply voltage. As the popular approach used in the design of the op amps is Complementary MOSFETs (CMOS) topology, the drivability of MOSFETs will decrease, signals will become smaller, the threshold voltage variations will become more restricted, and the gate delay time will increase even when scaling down the device dimensions.

The low threshold voltage is preferable to preserve the optimum performance when the power supply voltage is low. However, because the lowering of the threshold voltage causes a significant increase in the cut-off current passing through the channel of the MOSFET, the lower limit of the threshold voltage should be neatly considered by observing the stability of the circuit operation and the power dissipation.

Due to the prominent characteristics of the MOS transistor, it became a subject of research to develop a new generation of field-effect transistors for utilization in the design of the next generation of op amps that operate within ultra-low power ranges. The technology adopted in developing the new generation of MOS devices is micro-technology, through which the channel length of these devices is scaled down to the sub-micrometer range.

As a result of the scaled-down channel length of planar MOSFET into the sub-micrometer range, so-called short channel effects arise, such as Drain-Induced Barrier Lowering (DIBL), surface scattering, velocity saturation, and impact-ionization [1]. These unwanted effects are attributed to two physical phenomena: the restriction imposed on carriers' drift characteristics in the channel and the threshold voltage variation due to the shortening of the channel length.

2. Literature Review

Many researchers have proposed a variety of methods in the design of low voltage and low power op amps with the use of different MOS technology, such as 0.13µm with a supply voltage of 1.2V [2], 0.1µm with a supply voltage of 1V [3], 0.18µm with a supply voltage of 2.5V [4], 0.18µm with a supply voltage of 1V [5], 0.6µm with a supply voltage of 5V [6] and 0.13µm with a supply voltage of 1.8V [7]. However, the op-amps proposed by those researchers still exhibit a reduction ratio in the output swing with a low response. The reduction in the swing dynamic range is regarded to be very problematic when operating in low-range supply voltages and within low power range.

Therefore, a rail-to-rail two-stage op-amp has been proposed to address this problem. When designing the low-power rail-to-rail CMOS op-amp, the Common-Mode Feedback (CMFB) technique has been used for low-voltage op-amp circuits [8]. In this method, the loop created between output and internal nodes can set up several additional poles and zeros that could change the transfer function behaviour of the op-amp. The bulk-driven approach has been used to reduce the threshold and supply voltage. A low-voltage cascode biasing circuitry model was also employed in this method to ensure proper operation of the input stage of the op-amp [9]. In this method, the gain and gain-bandwidth product performance is similar to that of an amplifier using a gate-driven approach, where a push-pull stage, which is biased in class-AB with a static feedback loop, should be used for achieving output rail-to-rail operation.

CMFB strategy has been used for high-speed, high-gain, and low-noise CMOS op-amp [10]. In this method, in addition to the short channel effects that arise because of the 0.18µm process, the loop created between output and internal nodes can set up some additional poles and zeros that could change the transfer function behaviour. A 0.18µm CMOS technology has been used when designing low-power, rail-to-rail op-amp to achieve a constant transconductance [11]. In the simulation of this op-amp, the total power consumption was 39.6µW, with the transconductance change rate of the input stage being 2.1%.

3. Methodology

A new approach is presented in this paper for the design of an Op-Amp that is Electrically Programmed (EPOPAMP) to achieve wider bandwidth and constant transconductance while operating in the ultra-low power range. The new approach adopts the use of two types of techniques: the self-compensation process in the separation of the poles to guarantee stability with a wide bandwidth instead of using the external compensation capacitor and the stable bias currents technique for achieving a constant transconductance along the common-mode input range.

The self-compensation technology is achieved by using Electrically Programmed MOS devices (EPMOSFETs) of a high transconductance, where electrical programming technology is specially designed for the MOS devices to increase the transconductance and reduce the consumed power by enabling precision control of specific parameters such as threshold voltage of gate. The stable bias currents, which produce a constant overall transconductance, will guarantee a perfect output voltage swing even when operating at a low power range. In all of the previous propositions in the design of a low-power op-amp, an external compensation capacitor was used to separate the poles to guarantee stability. As a result of using a pure capacitor to separate the poles, one zero is introduced in the transfer function of the two-stage op-amp. This zero lies in the right half of the s-plane where, due to the location of this zero, a reduction in the phase margin, gain margin, and bandwidth occurs. Therefore, to increase the stability of the two-stage op amp, the nulling resistor RN has been added in series with the compensation capacitor to give the zero described by Equation (1) [12],

$$z = 1/[(1/g_{m}P) - R_N]C_C \quad (1)$$

Where g_{mP} is the transconductance of the P-type MOSFET, and C_C is the compensation capacitor. To guarantee stability, this zero is moved to the left half of the s-plane by choosing a value for R_N so that $R_N > 1/g_{mP}$. Thus, this resistance will contribute to increasing the power dissipation. Moreover, it is worth noting that the compensation capacitor should be large enough to separate the poles far from each other, where the high value of C_C results in degradation in the unity gain frequency, bandwidth, and slew rate.

In this work, the EPOPAMP is designed using electrically programmed MOS devices with zero threshold voltage to guarantee ultra-low power consumption. The new design of EPOPAMP adopts two types of techniques: the self-compensation technique in the separation of the poles to achieve a higher stability and wide bandwidth, and the stable bias currents technique for achieving a constant transconductance over the common-mode input range, and thus a perfect output swing with a stabilized voltage gain.

3.1. Self-Compensation Technique

In this work, the poles are separated away from each other by the high-transconductance EPMOSFETs instead of using an external compensation capacitor to address the issues resulting from this capacitor and achieve higher unity-gain frequency, wider bandwidth, and higher slew rate with lower power consumption. In this case, the transfer function of the EPOPAMP has no zeros, but it has a pair of real poles, p_1, and p_2, which are given by:

$$p_1 = -\frac{1}{g_m(r_{oN}||r_{oP})^2 C_{gd}} \quad (2)$$

$$p_2 = -\frac{1}{(r_{oN}||r_{oP})C_{gd}} \quad (3)$$

Where g_m is the transconductance of the P-type or N-type EPMOSFET, r_{oN} and r_{oP} are the output resistances of the N-type and P-type EPMOSFETs, and c_{gd} is the internal parasitic capacitance of the P-type or N-type EPMOSFET. Since the output resistances r_{oN} and r_{oP} have a very high value (in order of mega ohm) and the parasitic capacitance c_{gd} is of low value (in order of pico farad), the non-dominate pole p_2 is separated far from the dominant pole p_1 by the large transconductance of the EPMOSFET. Thus, the EPOPAMP will behave like a first-order system, with high stability and wide bandwidth.

3.2. Stable Bias Currents Technique

The instability reason for the overall transconductance (G_{mt}) along the common-mode input range is the instability of the bias currents along the input range. Therefore, to achieve high and constant G_{mt} over the common-mode input range and thus a perfect output swing with a stable voltage gain, the bias currents of the input stage are stabilized along the common-mode input range. In this work, the bias current (I_{bN}) of the N-type differential pair and the bias current (I_{bP}) of the P-type differential pair is stabilized along the common-mode input range by two circuits of the current sources. These circuits are designed using electrically programmable MOS devices as they are featured fully matched in structure with the possibility of programming the voltage threshold for the MOSFET devices to zero volts. Moreover, these two circuits of the current sources are designed such that the bias currents are functions to the aspect ratios (W/L) of the MOS devices, as shown in Figures 1 and 2.

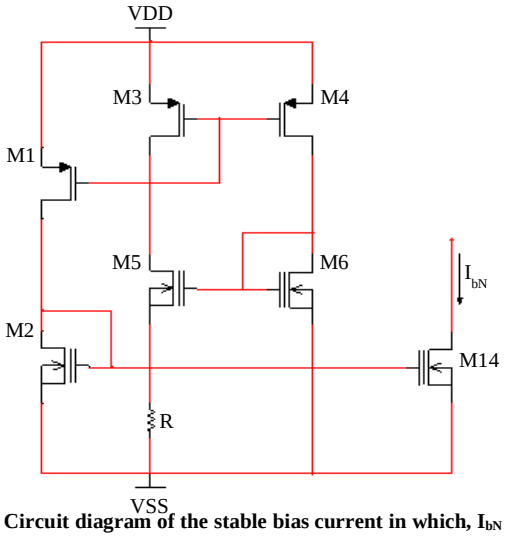

Fig. 1 Circuit diagram of the stable bias current in which, I_{bN} is a function of $(W/L)_{M5}$ using the EPMOSFETs

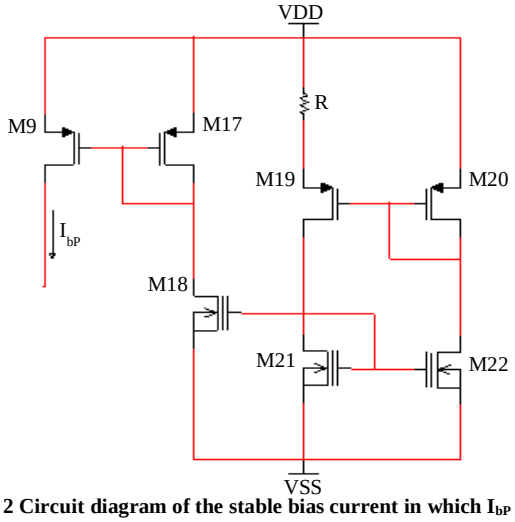

Fig. 2 Circuit diagram of the stable bias current in which I_{bP} is a function of $(W/L)_{M19}$ using the EPMOSFETs

In these two topologies, it is found that,

$$I_{bN} = \frac{2(1-\sqrt{(W/L)_{M6}/(W/L)_{M5}})^2}{R^2 k_{n6}} \quad (4)$$

$$I_{bP} = \frac{2(1-\sqrt{(W/L)_{M20}/(W/L)_{M19}})^2}{R^2 k_{p20}} \quad (5)$$

Where k_{n6} and k_{p20} are the device parameters of M6 and M20 respectively. Since the EPMOSFETs are structurally matched, the transistors M5 and M19 should be resized such that, $(W/L)_{M5} > (W/L)_{M6}$ and $(W/L)_{M19} > (W/L)_{M20}$. The resizing process is by a parallel connection of the EPMOSFETs group with M5 and M19 to give the bias currents I_{bN} and I_{bP} as:

$$I_{bN} = \frac{2(1-\sqrt{(1/n)})^2}{R^2 k_n} \quad (6)$$

$$I_{bP} = \frac{2(1-\sqrt{(1/n)})^2}{R^2 k_P} \quad (7)$$

Where n is the total number of the paralleled EPMOS devices.

As the EPOPAMP has a rail-to-rail input stage, it has two types of differential amplifiers: N-type differential amplifier and P-type differential amplifier. Thus, from the small-signal circuit model, it can be shown that the transconductance (G_{mN}) of N-type differential amplifier and the transconductance (G_{mP}) of P-type differential amplifier are,

$$G_{mN} = \sqrt{k_n I_{bN}} \quad (8)$$

$$G_{mP} = \sqrt{k_p I_{bP}} \quad (9)$$

Substituting Equations (6) and (7) in Equations (8) and (9) gives,

$$G_{mN} = \frac{\sqrt{2}\,(1-\sqrt{1/n})}{R} \quad (10)$$

$$G_{mP} = \frac{\sqrt{2}\,(1-\sqrt{1/n})}{R} \quad (11)$$

It follows that the overall transconductance G_{mt} of the EPOPAMP is,

$$G_{mt} = G_{mN} + G_{mP} = \frac{2\sqrt{2}\,(1-\sqrt{1/n})}{R} \quad (12)$$

Equation (12) states G_{mt} is constant and independent of device parameters. That means that the EPOPAMP is stable against supply voltage changes and temperature. Figure 3 shows the EPOPAMP circuit, where the EPMOSFETs were designed by Multisim software with the Spice model: the aspect ratio of all MOS devices is 2, k_n = 3.2, k_p = 1.3 and V_{TH} = 0V to achieve the properties of the EPMOSFETs.

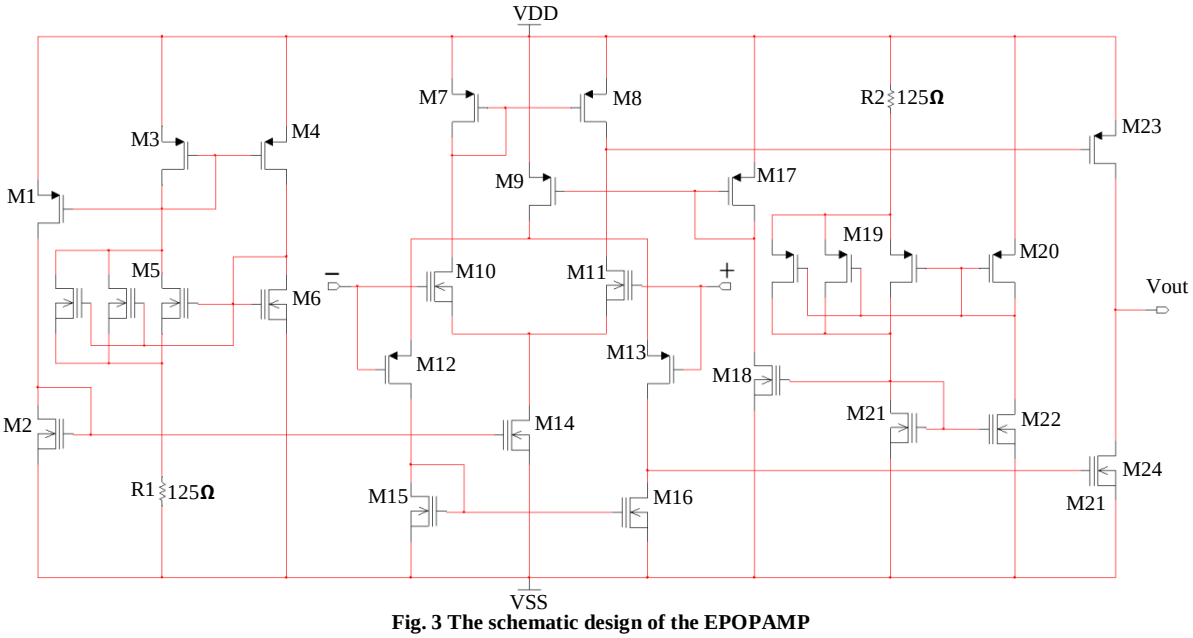

Fig. 3 The schematic design of the EPOPAMP

4. Simulation Results

4.1. Open-Loop Gain and Unity-Gain Bandwidth

The open-loop gain test has shown that the EPOPAMP has a high open-loop gain, where the DC gain was in the value of 136dB with a Unity-Gain Bandwidth (UGB) of 4.2GHz and a breakpoint frequency of 667Hz, as shown in Figure 4.

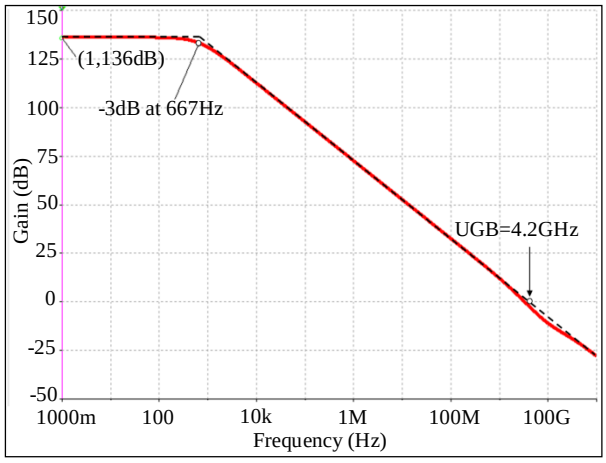

Fig. 4 Open-loop gain vs. Frequency of the EPOPAMP

4.2. Phase Margin and Gain Margin

Phase Margin (PM) and Gain Margin (GM) test results have shown that the EPOPAMP exhibits a PM of 41° and GM of 11dB, as shown in Figure 5.

4.3. Bandwidth

In this aspect of the test, the bandwidth of the EPOPAMP is measured by using it as an inverting amplifier. Because of the wide unity-gain bandwidth, the EPOPAMP has recorded a wide bandwidth when configured as an inverting amplifier. Figure 6 shows the bandwidth of the EPOPAMP versus frequency when configured as an inverting amplifier while considering two values of closed-loop gain, 10V/V and 100V/V.

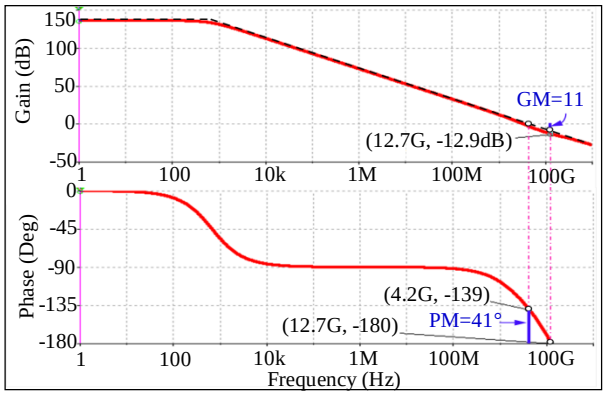

Fig. 5 Phase Margin and Gain Margin of the EPOPAMP

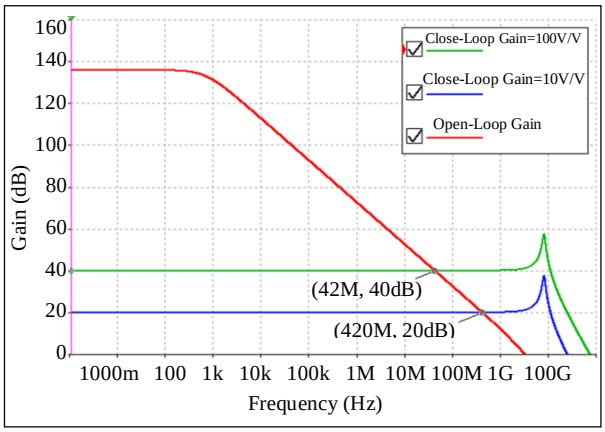

Fig. 6 Bandwidth vs. Frequency of the EPOPAMP corresponding to two values of closed-loop gain when configured as inverting amplifier

4.4. Output Voltage Swing

When using positive and negative voltage follower configurations to examine the output swing, the EPOPAMP exhibited an ideal output swing equal to the power supply voltage rails. Figure 7 shows the output of the positive rail circuit and the output of the negative rail circuit at VDD = 100mV and VSS = -100mV with input peak-to-peak amplitude of 200mV.

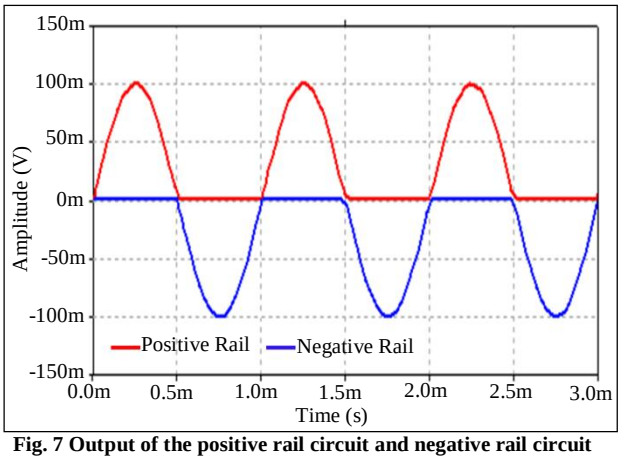

Fig. 7 Output of the positive rail circuit and negative rail circuit

Thus, the ideal output swing results in stable voltage gain and distortion-free output with wide bandwidth.

4.5. Input Offset Voltage

The offset voltage of an op amp is a random variable and can take either positive or negative values. However, the output voltage will not be zero due to the input offset voltage, even if the input voltage is zero. The input offset voltage (Vio) is measured by utilizing the characteristics of the negative feedback circuit with grounded inputs. For measuring the offset voltage accurately, the ratio of the negative feedback resistors should be high, especially for the op-amps that exhibit a very low offset voltage. Using the ratio 100 for the negative feedback resistors, Vio and Vout of the EPOPAMP were 0.47pV and 47pV, as shown in Figure 8.

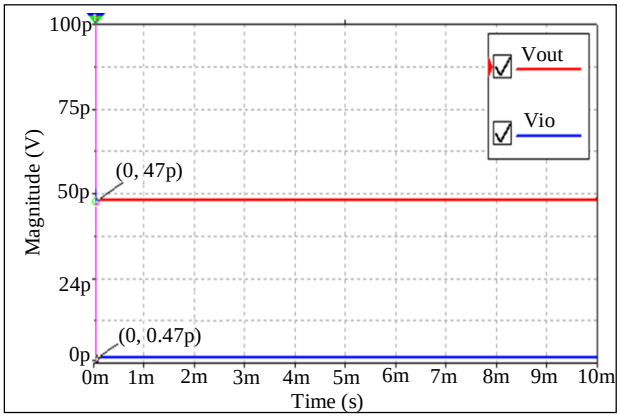

Fig. 8 Input offset voltage of the EPOPAMP and the corresponding output voltage

Accordingly, the input offset voltage required to set the output to zero volts is 0.47pV, which is almost equal to zero volts.

4.6. Common-Mode Rejection Ratio

The Common-Mode Rejection Ratio (CMRR) indicates the ability of the operational amplifier to suppress the conjoint signals between the two input terminals, where this parameter determines the precision output of the op-amp. In the ideal op-amp, the CMRR is of infinite value. Therefore, as this parameter increases, the op-amp tends to behave ideally in suppressing the conjoint input signals between the inverting and non-inverting terminal. For measuring the CMRR, the EPOPAMP is configured as a differential amplifier using four precision resistors; a signal is applied to both inputs, and the output is measured. Figure 9 shows the signals of the input and output of the EPOPAMP when configured as a differential amplifier.

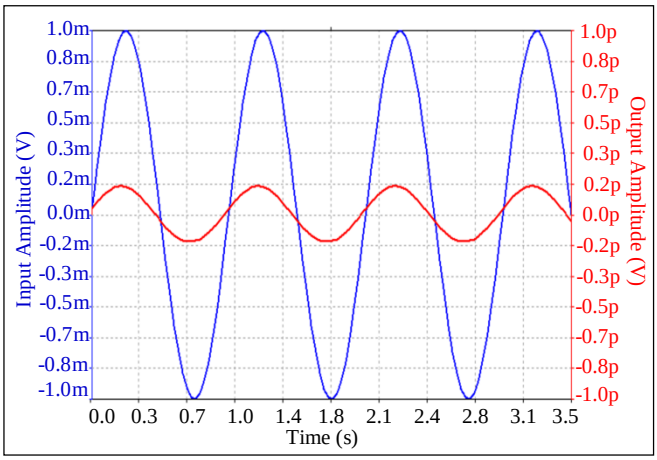

Fig. 9 Input and output amplitude of the EPOPAMP for measuring the CMRR

With the negative feedback resistors ratio of 2, the Common-Mode Rejection Ratio is expressed in decibels as [13]:

$$\text{CMRR(dB)} = 20\log\left(\frac{2\Delta V_{in}}{\Delta V_{out}}\right) \quad (13)$$

Thus, from Equation 13,

$$\text{CMRR(dB)} = 20\log\left(\frac{2x2mV}{0.4pV}\right) = 200\text{dB} \quad (14)$$

4.7. Power Supply Rejection Ratio

Power Supply Rejection Ratio (PSRR) refers to the ability of the op-amp to reject any variations in supply voltage that might reflect at the output. Thus, this parameter should be as large as possible in the design of the op-amps. The power supply rejection ratio is measured by testing the change in input offset voltage concerning the change in supply voltages and is usually expressed in decibels.

When testing the power supply rejection ratio of the EPOPAMP, it is found that the rate of change in the input offset voltage resulting from the variations in the supply voltages VDD and VSS are 4pV/V and 10pV/V. In general, the CMRR and the PSRR are frequency-dependant parameters, where those parameters decrease with increasing frequency. Figure 10 illustrates the relationship of the CMRR and the PSRR of the EPOPAMP with the frequency.

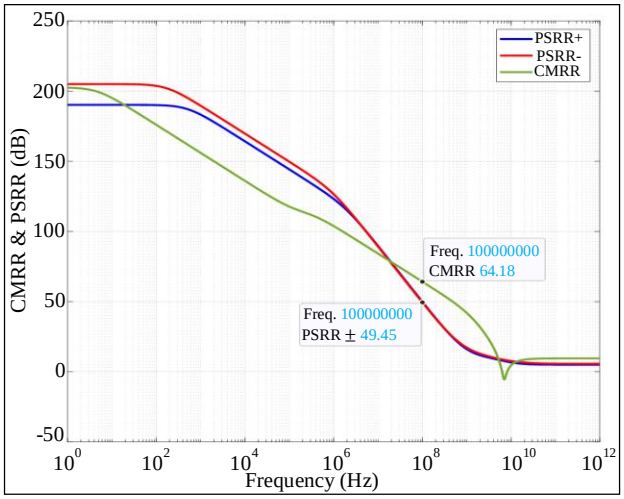

Fig. 10 Relationship of CMRR and PSRR of the EPOPAMP with the frequency

4.8. Slew Rate

Through using an input step with a final value of 0.1V and supply voltages of ±0.1V with configuring the EPOPAMP as a voltage follower, the test result has shown that the output of the EPOPAMP behaves ideally in tracking the input (infinite slew rate) as shown in Figure 11.

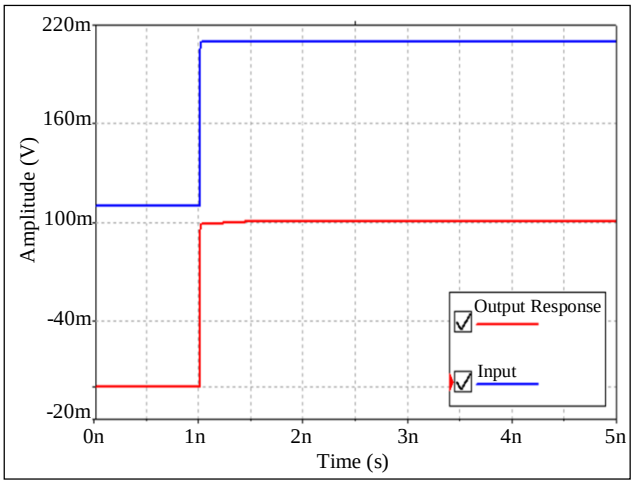

Fig. 11 Slew rate of the EPOPAMP

The infinite slew rate of the EPOPAMP is due to the use of the self-compensation technique instead of the external compensation capacitor, which causes a reduction in the slew rate.

4.9. Power Consumption

Power consumption in an op-amp, also known as quiescent power, is the amount of energy that the op-amp consumes when no signal is processed. The quiescent power consists of the total quiescent current that refers to the amount of current drawn by the op-amp to keep the op-amp's stages biased at the operating point. Power consumption is measured by configuring the EPOPAMP as a voltage follower with dual supply voltages of ±0.1V. The test result of the power consumption has shown that the EPOPAMP consumes only 5.39µW at a total quiescent current of 53.9µA.

4.10. Noise Analysis

The noise analysis for the EPOPAMP at the very high gain mode (open loop gain) has shown that the EPOPAM attenuates the noise at the output even when the input noise increases, as shown in Figure 12.

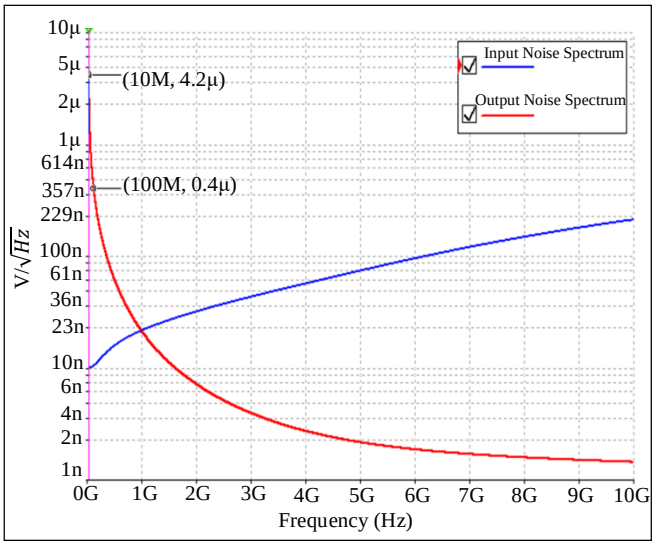

Fig. 12 The input and output noise spectrum of the EPOPAMP versus frequency

In addition, the noise test has shown that, at the frequency that covers the bandwidth of the EPOPAMP, which is 500MHz, the Noise Figure (NF) is -11dB, which means that the noise Factor (F) at this frequency is 0.07.

5. Conclusion

The results of this study have shown that the new topology of the op-amp has successfully satisfied all the design specifications given in advance. This study has significantly contributed to reducing power dissipation and highly optimizing the performance of the op-amps close to the ideal through electrical programming technology.

Thus, it is possible to release a new generation of op amps that operate at ultra-low power and wideband to cover a variety of applications within a single integrated circuit.

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