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Review Article

A Review on Low-Power Two-Stage CMOS Operational Amplifiers

Alaa H. Mohammed[1], Maizan Muhamad[2], Hanim Hussin[3]

[1,2,3]*Integrated Microelectronic System and Application (IMSaA), College of Engineering, Selangor, Malaysia.*

[2]*Corresponding Author : maizan@uitm.edu.my*

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Abstract *- Due to the increasing demand for low-power integrated analog circuits such as operational amplifiers, the design of these amplifiers for operating within the sub-threshold voltage range has become more substantial. This paper represents a review of the proposed techniques in the design of low-power operational amplifiers. In addition to presenting the parameters related to reducing the power consumption, such as supply voltage, bias current, and MOS devices technology, this paper presents the frequency-dependent parameters like slew rate, unity-gain bandwidth, and phase margin with the limitations that arise due to using the proposed techniques in optimizing of these parameters.*

Keywords *- Low-power operational amplifier, Limitations of low-power operation, Low-power consumption techniques, Bandwidth, Stability.*

1. Introduction

An Operational Amplifier (Op-Amp) is a DC-coupled high-gain voltage amplifier with a differential input and usually a single-ended output. The Op-Amp is a core part of linear and non-linear analog circuits and a building block that covers wide applications such as signal processing, filtering, power harvesting, electronic control, etc.

The optimum performance of the Op-Amps became increasingly challenging in the direction of reducing the supply voltage and power consumption without neglecting other performance parameters. Therefore, a new approach has been adopted in designing such amplifiers by using near-ideal components in power consumption and operation at low supply voltage, such as Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs).

Semiconductor technology continues scaling down the MOS transistor size to achieve faster processing, lower power consumption, and large-scale integration on a single chip. Although the smaller size technology provides a potential for operation at higher frequencies and less power consumption, this fact partially applies to analog circuits because there is a need for additional current to keep the same performance when the power supply voltage decreases.

The power consumption is minimized in analog electronic circuits by reducing the supply voltage, reducing the total input bias current, or reducing both. For an Op-Amp, reducing the bias current leads to degrade the dynamic range of output swing, and reducing the supply voltage makes it hard to keep transistors in a saturation condition [1].

Furthermore, a decrease in the supply voltage without a similar reduction in threshold voltage leads to bias issues. Thus, it became necessary to propose a typical topology in the design of such amplifiers. Although Op-Amps have a very high voltage gain, this gain level starts to fall with increasing the input frequency. An Op-Amp of high gain is built by cascading multiple gain stages. In theory, the Op-Amp gain increases with increasing cascaded stages. However, increasing the number of cascaded stages will result in introducing additional poles in the Op-Amp's transfer function, H(s), which is given by,

$$H(s)= \frac{A_{vo} p_1 p_2 p_3 \ldots p_n}{(s+p_1)(s+p_2)(s+p_3)(s+p_{n)}} \quad (1)$$

Where A_{vo} is the open-loop DC voltage gain and p_2, p_3, …, p_n, are the added poles due to increasing the cascaded gain stages. These additional poles reduce the bandwidth of the Op-Amp, as demonstrated in Figure 1. Several methods in the design of multi-stage, low-power Op-Amps have been proposed to achieve wide bandwidth and high voltage gain. The two-stage Op-Amp is one of the multi-stage Op-Amps that characterized optimum performance in both gain and bandwidth and the potential to operate within a low power range. However, implementing a two-stage CMOS Op-Amp, a second-order system, still encounters stability problems because its transfer function has two poles. Generally, the

second-order system with unity feedback has the following transfer function [2].

$$H(s)=\frac{\omega_n^2}{S^2+2\zeta\omega S+\omega_n^2} \quad (2)$$

Where ζ is the damping ratio, and ω_n is the natural frequency. Thus, the second-order system in standard form has the characteristic equation $s^2 + 2\zeta\omega_n s + \omega_n^2$, where the roots for this system are $s_1, s_2 = -\zeta\omega_n \pm j\sqrt{1-\zeta^2}$. However, if $\zeta < 1$, the poles are complex conjugate pairs, and the system oscillatory at the initial condition. If $\zeta \geq 1$, the system will not exhibit oscillations at the initial condition, where the poles are real. Stability criteria state that, for the system to be stable, the Phase Margin (PM) should be at least 45°, where PM in terms of ζ is given by [3]:

$$PM= tan^{-1}(2\zeta/\sqrt{\sqrt{4\zeta^4+1}-2\zeta^2}) \quad (3)$$

Figure 2 demonstrates the corresponding time response to the effect of poles in the second-order system. It is concluded that, as ζ increases, the poles tend to be real and are separated far from each other. Therefore, in the design of a two-stage Op-Amp, the two poles should be separated so that the system behaves like a first-order system and thus guarantees stability.

Furthermore, achieving a higher unity-gain frequency (at which the Op-Amp's voltage gain equals 1) is a complex problem in designing such amplifiers. Therefore, near-ideal design methodologies are needed to optimize the performance of the two-stage Op-Amp.

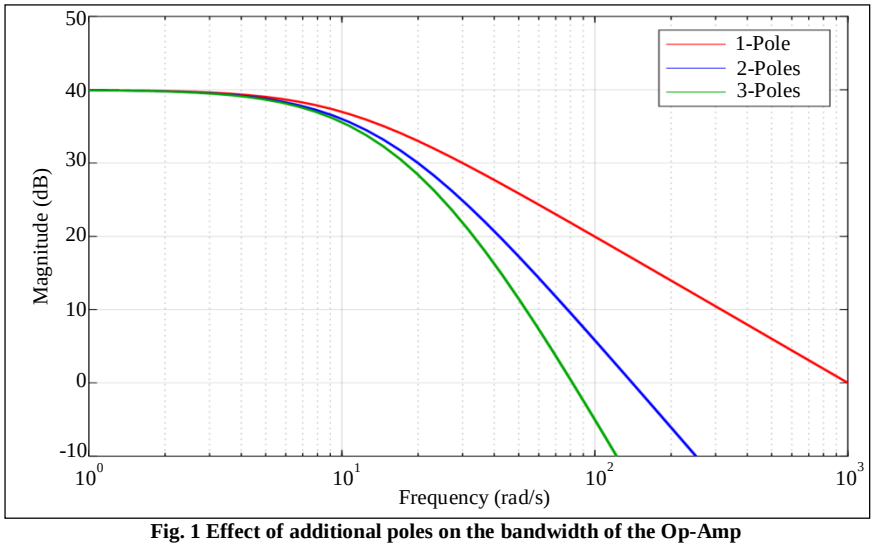

Fig. 1 Effect of additional poles on the bandwidth of the Op-Amp

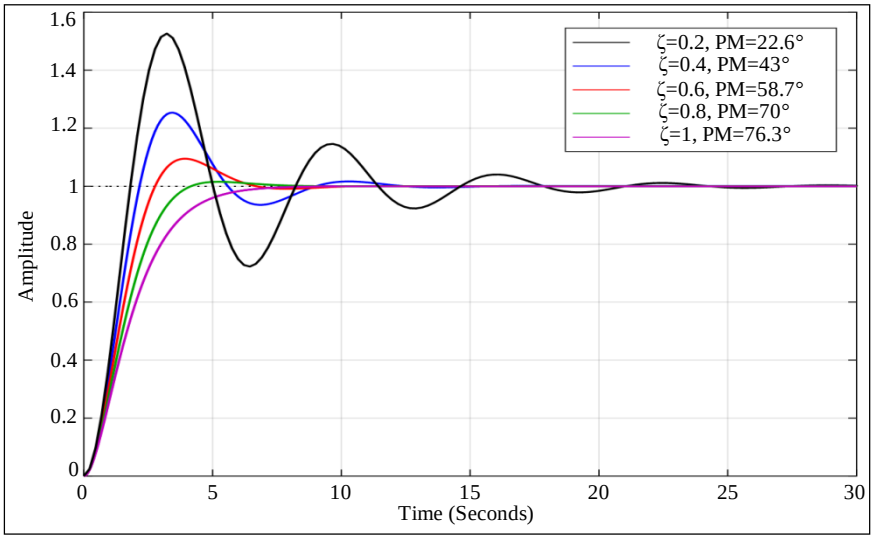

Fig. 2 Output response to a unit step input of the second-order system

2. The Two-Stage CMOS Op-Amp

Figure 3 depicts the general block diagram of the two-stage CMOS Op-Amp.

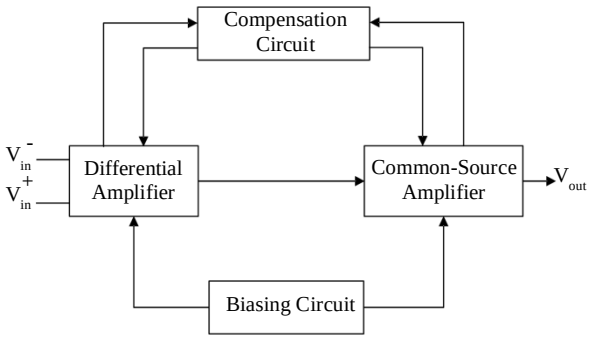

Fig. 3 Block diagram of two-stage CMOS Op-Amp [4]

The first block (input stage) is a differential amplifier (usually an N-type differential MOSFET amplifier) with two input terminals, an inverting terminal and a non-inverting terminal, and a single-ended output that depends only on the differential input voltage. The second block (output stage) is a common-source amplifier (usually a P-type common-source MOSFET amplifier) driven by the first stage to increase the overall voltage gain. The biasing circuit here provides an appropriate operating point for transistors in the saturation region, and the compensation circuit includes the techniques for optimizing the Op-Amp stability.

2.1. Circuit Diagram of Two-Stage CMOS Op-Amp

There are two main cascaded stages for amplification in the design of the two-stage CMOS Op-Amp: the differential amplifier and the common-source amplifier, as shown in Figure 4. The differential amplifier (input stage) achieves very high input impedance, high Common-Mode Rejection Ratio (CMRR), better Power-Supply Rejection Ratio (PSRR), low noise, and high gain with low offset voltage. The common-source amplifier (output stage) increases the overall voltage gain and converts the differential output to single-ended [5].

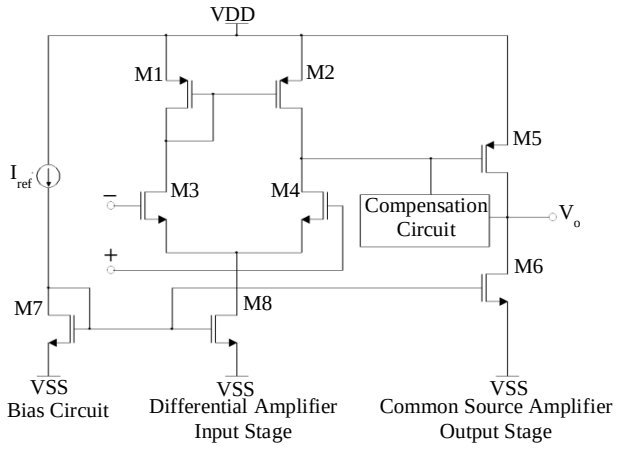

Fig. 4 Circuit diagram of two-stage CMOS Op-Amp

In the circuit of Figure 4, M1 and M2 are N-type MOS transistors, and M3 and M4 are P-type MOS transistors. These transistors configure the differential amplifier in CMOS topology to minimize the consumption of power [6]. The biasing circuit is a mirror circuit (M5 and M6) controlled by a programmed current (I_{ref}) to supply an appropriate bias current to the differential and common-source amplifiers. The compensation circuit involves the techniques of frequency compensation, where the goal of using these techniques is to avoid the unintended creation of positive feedback that causes oscillations in the Op-Amp output and to control the overshot at the response to the unit step function [7]. Frequency compensation techniques include the Miller compensation technique, the nulling resistor technique, and the voltage buffer or current buffer technique.

Miller compensation, also called direct feedback compensation, includes the connection of a single compensation capacitor C_c (Miller capacitor) between the outputs of the two stages. The working principle of the Miller capacitor is to separate the two poles from each other so that one dominant pole is achieved to force the two-stage Op-Amp to behave as a first-order system and thus guarantee stability. However, a zero is introduced in the transfer function of the two-stage Op-Amp due to the feed-forward current passing through the compensation capacitor from the output of the first stage to the production of the second stage, where this zero lies onto the Right Half of the s-Plane (RHP) [7]. The RHP zero is substantial in CMOS technology because it causes a low device transconductance (g_m) for a specific bias current, causing the value of this zero and the non-dominant pole to be comparable [8].

The nulling resistor technique has been proposed to eliminate the impact of the RHP zero by moving it away to the right by adding a nulling resistor RN in series with the compensation capacitor [9]. However, due to using this technique in separating the poles, another zero is added to the transfer function of the two-stage Op-Amp, where this zero is given by,

$$z_2 = \frac{1}{[(\frac{1}{g_m}) - R_N]C_c} \quad (4)$$

Thus, R_N should be chosen such that $R_N = 1/g_m$ to move this zero to infinity. However, this technique causes a narrower bandwidth. Therefore, the technology of the voltage buffer or current buffer in series with the compensation capacitor was proposed to guarantee stability and achieve wider bandwidth [10, 11].

3. Limitations of Low Power in the Op-Amp

In designing analog circuits such as two-stage Op-Amp, power is necessary to maintain the signal energy higher than thermal noise energy to achieve the desired Signal-to-Noise Ratio (*S*/*N*). Necessary power (*P*), produced from a voltage

source (V_B), to create a sinusoidal signal of peak-to-peak amplitude (V_{PP}) with a frequency (f) across a capacitor is expressed by [12]:

$$P = 8\frac{V_B}{V_{PP}}kTf(S/N) \quad (5)$$

Where k is Boltzmann's constant (1.38×10^{-23} Joule per Kelvin) and T is the temperature in Kelvin. As the peak value of a signal cannot exceed the supply voltage, the required minimum of this power (P_{min}) is when the peak-to-peak amplitude of signal V_{PP} is equal to the voltage source V_B, that is,

$$P_{min} = 8kTf(S/N) \quad (6)$$

Thus, the power should be increased 10-fold for every 10dB of S/N. This limit is an essential restriction that does not depend on the design technique of the two-stage Op-Amp or the power supply voltage. However, several limitations relate to low power consumption in the practical circuits of the two-stage Op-Amps:

Capacitors increase the power necessary to achieve a specific bandwidth. Therefore, they are only acceptable if their existence reduces the noise power by the same amount through reducing the noise bandwidth. For instance, the internal parasitic capacitors of MOS devices [13] used in the design of the two-stage Op-Amp often increase power consumption.

Power consumption is often in the bias circuits, but it should be minimized in the design of the two-stage Op-Amp. However, the bias circuits may increase the noise, resulting in a proportional increase in power consumption. For example, a bias current is noisier if it rises to compensate for the difference between the mismatched bias currents resulting from the structural mismatch in the MOSFETs structure.

According to Equation (5) the necessary power increases if the signal has peak-to-peak voltage amplitude V_{PP} smaller than the supply voltage V_B and a frequency within the bandwidth. Thus, care should be taken when amplifying the signal to its maximum possible voltage value, revealing a trade-off between power consumption and amplification of small signals of high frequency in such amplifiers.

In the MOS devices used in the design of the two-stage Op-Amp, the thermal noise voltage in the conducting channel and the flicker noise voltage [14] are considered the two prime sources of the noisy voltage. Thus, the presence of these noise sources in the circuit of the two-stage Op-Amp means increasing power consumption. In the case of capacitive loads imposed on the two-stage Op-Amp, the current, I, which is necessary to obtain a given bandwidth, is inversely proportional to the transconductance-to-current ratio g_m/I. Thus, the small value of gm/I of the MOS transistors that operate in a strong inversion may cause an increase in power consumption.

The dimensions of the MOS devices are directly proportional to the parasitic capacitor value. Therefore, the larger MOS transistors used in the Op-Amp design increase the power consumption. Thus, alternative techniques should be found when designing such amplifiers to overcome the effect of these limitations.

4. Op-Amp for Low Power and Low Voltage

For analog design, the essential behaviour that the MOS transistor is characterized by is the symmetrical model in which the drain current I_D is decomposed into a forward component I_F (drift current) and a reverse component I_R (diffusion current). If both I_F and I_R are in weak inversion, where the drain-to-source voltage V_{DS} is higher than zero and less than threshold voltage V_{TH}, then the MOS transistor is said to operate in a weak inversion, and the drain current I_D is given approximately by [15]:

$$I_D \approx I_{D0}e^{\frac{V_{GS}-V_{TH}}{\eta V_T}} \quad (7)$$

Where V_{GS} is the gate-to-source voltage, I_{D0} is the drain current at which $V_{GS} = V_{TH}$, η is the slope factor, which is weakly dependent on V_{GS} (tends to be 1 for V_{GS} very large), and $V_T = kT/q$ is the thermal voltage (about 26 mV at room temperature).

Derivation of Equation (7) concerning V_{GS}, gives the drain-to-gate g_m at weak inversion as:

$$\frac{\partial I_D}{\partial V_{GS}} = g_m = \frac{I_D}{\eta V_T} \quad (8)$$

Hence, the ratio g_m/I_D in the weak inversion is,

$$g_m/I_D = 1/\eta V_T \quad (9)$$

From Equation (9), it is noticed that the weak inversion provides the maximum value of g_m/I_D, resulting in a decrease in power consumption. This maximum value of g_m/I_D also provides a maximum value of the voltage gain, which helps simplify the structure of the two-stage Op-Amp.

Moreover, in weak inversion mode, MOS devices can operate at a minimum value of drain-to-source saturation voltage, which helps keep peak-to-peak signal amplitudes close to the bias voltage. Thus, at this mode of inversion, the maximum value of g_m and a wider bandwidth (g_m/C) for a given value of capacitive load C is achieved. Weak inversion mode is not viable at very high frequencies, where it cannot exceed a few hundred MHz for a MOSFET channel length of

1µm. In addition, this mode causes high relative noise content of the drain current and threshold voltage mismatch, where both effects result from the maximum value of g_m/I_D. Thus, using the weak inversion mode to cover operation requirements within a low power range leads to inaccurate and noisy currents. Achieving higher operating frequencies and higher precision of currents is possible by operating the MOS transistors in strong inversion. Operation of the MOS transistors in strong inversion requires a quadratic increase in drain bias current, which causes an increase in power consumption and loss of all the attractive features of weak inversion. Hence, it is probable that the MOS transistors operate duly between these two regions. In the strong inversion, the ratio g_m/I_D is given by [15],

$$\frac{g_m}{I_D} = \frac{2}{\varepsilon_x L + (V_{GS} - V_{TH}) - \varepsilon_x L\sqrt{1 + \frac{V_{GS} - V_{TH}}{\varepsilon_x L}}} \quad (10)$$

Where ε_x is the horizontal electric field strength along the channel, and L is the length of the channel. When ε_x exceeds a critical value (ε_c) that is on the order of 10-100 KV/cm [16], the velocity will saturate, and Equation (10) collapses to:

$$\lim_{\varepsilon_x \to \infty} (g_m/I_D) = 2/(V_{GS} - V_{TH}) \quad (11)$$

Thus, to estimate the transition possibility from weak to strong inversion, the ratios described by Equations (9) and (11), should be equated, that is,

$$V_{GS} - V_{TH} = 2\eta V_T \quad (12)$$

Although this estimation implies that the transition from weak to strong inversion occurs suddenly, a non-zero transition width occurs between weak and strong inversion. This non-zero transition width refers to a moderate inversion region, where the MOS transistor operates in this region with relatively high drift and diffusion currents. Assuming that η = 1 and L = 1µm, Figure 5 plots the ratio g_m/I_D versus overdrive ($V_{GS} - V_{TH}$) for the three regions.

For a simple model, the plot of moderate inversion has been ignored in this figure as it is unknown in practical application. When the overdrive is negative but enough to cause a depletion at the surface, the MOS device operates in weak inversion, and the ratio g_m/I_D is constant. At $V_{GS} - V_{TH}$ = 0, the concentration of electrons at the surface is equal to the concentration of holes in the bulk, where this point is referred to as the upper bound of the weak inversion region. At $V_{GS} - V_{TH} > 2\eta V_T$, g_m/I_D is given by Equation (10) where $\varepsilon_x << \varepsilon_c$ with the velocity being unsaturated yet, while Equation gives it (11), where $\varepsilon_x >> \varepsilon_c$ and the velocity is saturated.

In the design of a two-stage CMOS Op-Amp, a high ratio of g_m/I_D may obtained by increasing the ratio of channel width to its length (W/L) of MOS devices, where this ratio predominantly exceeds a value of 1000 [17]. The high W/L may result from wide-channel MOSFETs to achieve high g_m or short-channel-length MOSFETs to operate with high frequencies. Channel width affects the MOSFET breakdown voltage, where based on the gate voltage, the wide-channel devices have 10-30% lower breakdown voltage than the narrow-channel devices [18]. The short-channel causes the so-called short-channel effects, including drain-induced barrier lowering, surface scattering, velocity saturation, impact-ionization, and hot electrons [19].

Therefore, some researchers proposed biasing the MOSFETs used in the design of the Op-Amp within moderate inversion region for maximum voltage gain, low power dissipation, and minimum total harmonic distortion, and others proposed using MOS devices with a high aspect ratio or the sub-micrometer technology.

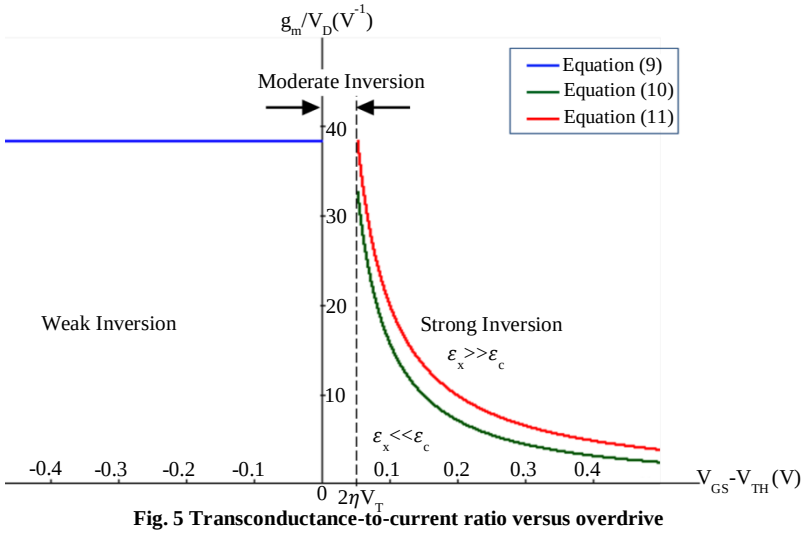

Fig. 5 Transconductance-to-current ratio versus overdrive

5. Low-Power Two-Stage CMOS Op-Amp

One of the proposed methods in the design of a two-stage Op-Amp that operates within a low power range is by maximizing the ratio gm f_T/I_D by operation in a moderate inversion region, where f_T is the frequency at which the current gain of the Op-Amp reaches one when the source and drain are short circuit. In this method, the measurement results have shown a noise figure of 4.9dB and a small signal gain of 15.6dB with a power dissipation of 100µW [20]. For reducing the power dissipation by reducing the bias current, the method of input-dependant bias using feedback loops in the input transistors of the differential pair has been proposed, where a bias current of 1µA and dissipated power of 16.8µW have been recorded using this method [21]. However, using these two methods, the proposed Op-Amps operate at a 2V power supply. The method of forward biased source substrate junction, along with a low voltage current mirror and low-power Op-Amp (40µW), has been proposed, where in this method, it was noted a degrading in performance in terms of the Unity Gain Bandwidth product and the slew rate [22].

Two Op-Amp types that consume less than 500µW power have been proposed, but their designs also suffer from the low gain bandwidth product [23, 24]. Various design methods for low-power operational amplifiers that include the technique of telescopic Op-Amp were proposed, where all of them suffer from limitations on the open loop gain or the Unity Gain Bandwidth product [25]. Another design method has been proposed to cover the requirements of operating the Op-Amps in a low supply voltage and low power, where this method includes scaling down the channel length of MOS transistors into fractions of micrometre technology. Table 1 lists the improved parameters of the two-stage low-power Op-Amps proposed by several researchers using this method.

Table 1. The improved parameters of the low-power two-stage Op-Amps proposed by some researchers using fractions of the micro-technology

Op-Amp Parameters	References								
	[26]	[27]	[28]	[29]	[30]	[31]	[32]	[33]	[34]
Supply Voltage (V)	1.2	1.5	1.2	1	1.8	1.8	1.5	1	0.8
MOS Technology (µm)	0.13	0.18	0.13	0.1-0.8	0.18	0.15	0.18-0.065	0.18	0.18
DC Gain (dB)	54.8	92.5	85.9	–	66	59.5	73.57	96.38	83
Slew Rate (V/µs)	5.8	16.7	44.2	–	–	185	10.1	–	–
UGB (MHz)	32.5	236	55	–	100	504	1.084	4.077	–
Phase Margin (degree)	–	81.3	–	–	57	60.6	65.89	71.46	–
Output Swing (V)	–	1.26	1.1	–	–	–	–	–	–
CMRR (dB)	–	–	61	130	75	–	147.9	–	–

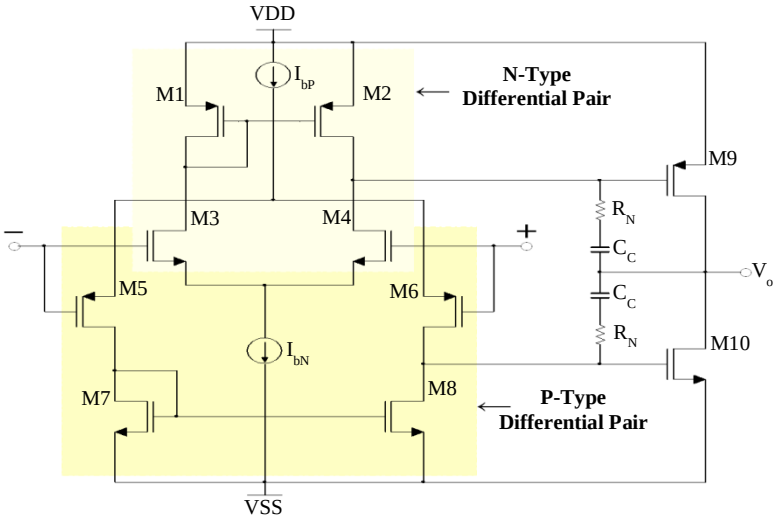

Fig. 6 Circuit diagram of the rail-to-rail two-stage Op-Amp

However, the two-stage Op-Amps proposed by those researchers still exhibit a reduction ratio in the output swing. The reduction in the swing dynamic range is problematic when operating in low-range supply voltages and within ultra-low power range. Therefore, a rail-to-rail two-stage Op-Amp has been proposed to address this problem.

Rail-to-rail is a term used to describe the Op-Amp that has the potential to make whose dynamic output range reaches the extreme values of the supply voltages. The rail-to-rail technique implies a design of the two-stage Op-Amp by a couple of N-type and P-type differential amplifiers in a complementary configuration as the input stage. Figure 6 depicts the circuit diagram of a rail-to-rail two-stage Op-Amp with the nulling resistor technique.

Through this topology, it is supposed that the input of the N-type differential pair has the potential to reach the value of the positive bias voltage, and the input of the P-type differential pair has the potential to track the value of the negative bias voltage. Thus, it is supposed that the overall transconductance (Gm) of the Op-Amp is equal to the sum of the transconductances of the N-type and P-type differential pairs, which means that the output voltage gain will increase, and the output swing will improve.

Although the rail-to-rail two-stage Op-Amp improves the output swing through doubling Gm, this improvement is restricted by the contribution mechanism of the differential pairs in increasing Gm along the input range, where at the extreme input ranges, one of the differential pairs tends to be active. That will cause Gm to be non-constant over the common-mode input range, where it will be halved at the maximum input ranges, resulting in open-loop gain instability. Therefore, various methods were proposed in designing a low-power rail-to-rail CMOS Op-Amp with a constant Gm. Table 2 surveys the proposed techniques in the designing of such Op-Amps.

Table 2. Methods for design low-power rail-to-rail Op-Amps with a constant G_m

References	Method	Limitations
[35]	Biasing the input stage by processed currents rather than the tail current for selecting the maximum G_m as a constant-transconductance of the input stage.	In this method, even if the maximum G_m is chosen, the value of the total transconductance in the transition region is still lower than the maximum G_m, and this method needs fully matched MOS devices.
[36]	The sum of VSG and VGS of the PMOS and NMOS devices is constant using three kinds of current bias circuits with a common unit structure.	This method requires MOS devices that are structurally matched.
[37]	Overlapping the transition region of the tail currents for both complementary differential pairs of the input stage.	In the simulation of this method, it was found that the most constant Gm is achieved at a transconductance factor (β) equal to $9\mu A/V^2$. This leads to degrading in noise performance because the input-referred noise is inversely proportional to G_m.
[38]	Using a reference circuit consisting of a PMOS differential pair the same as the input PMOS differential pair, which share the same load, generates a reference transconductance.	This technology requires N-type and P-type MOS devices that are structurally matched to maintain a constant G_m under any condition.
[39]	A transconductance control circuit maintains the constant sum of the currents in the complementary differential pairs of the input stage.	In this method, the currents in the N-type differential pair are regulated using a negative feedback loop to keep the sum of the currents in the complementary differential pairs constant. This technique produces a constant G_m operating in the weak inversion. Therefore, there is a trade-off between the frequency response and the constancy of G_m.
[40]	Bulk-driven approach was used to reduce the threshold voltage and supply voltage. A low-voltage cascode biasing circuitry model was also employed in this method to ensure proper operation of the input stage of the proposed Op-Amp.	In this method, the gain and gain-bandwidth product performance is similar to that of an amplifier using a gate-driven approach is obtained. In addition, a push-pull stage, which is biased in class AB using a static feedback loop, should be used to achieve output rail-to-rail operation.
[41]	0.18μm CMOS technology	Total power consumption is 39.6μW, with the transconductance change rate of the input stage at 2.1%.

Many researchers have proposed a variety of techniques in the design of an Op-Amp operating with a low power and low supply voltage, such as cascaded three stages with Miller frequency compensation by Nested [42], where this Op-Amp is designed in 180nm technology and operates at a 3V power supply with a gain of 115 dB, bandwidth of 103MHz and phase margin of 45ºC. Chanapromma and K. Daoden have proposed a low-power, low-voltage operational amplifier that operates in a weak inversion region with a power consumption of 221nw and voltage supply of ±0.7V [43]. A rail-to-rail operational amplifier with improved DC gain and reduced power consumption by adding a partial feedback loop has been presented by T.V. Cao et al., [44], where, in this topology, the standby power consumption was 96µW.

With the use of the flipped differential pairs technique, a CMOS operational amplifier with constant transconductance along the common-mode input stage has been proposed by C. Guo et al., [45], where this Op-Amp operates in low voltage environments with a closed-loop Unity-Gain Bandwidth of 7.6MHz and open-loop gain of 73dB. This Op-Amp was designed to operate at a 1V power supply and implemented in 0.18µm technology.

A low-power two-stage operational amplifier has been proposed by Mohammadpour and M. Rostampour using the indirect Miller effect method for separating the poles and guaranteeing stability [46], where this method was implemented by 50nm CMOS technology and a 50fF capacitor as a compensation capacitor. S. Thanapitak presented a low power wide linear range operational amplifier that operates in the weak inversion region by employing three different transconductance linearization techniques: bulk-driven, floating gate MOSFET, and drain current normalization [47]. The proposed Op-Amp was designed by a 0.1µm CMOS process, where the power consumption of this Op-Amp was 48.98nW at 10nA bias current.

A low-power CMOS Op-Amp has been proposed by K.J. Raut et al. using a standard 180nm digital n-well CMOS process [48]. In this design, the open loop gain of the Op-Amp was 74.89 dB, the Unity Gain Bandwidth was 7.3 MHz, and the phase margin was 48° with 10pF capacitive and 1MΩ resistive load, where the average power consumption was 0.402mW, and slew rate was 10V/µs.

D.J. Dahiga onkar et al. proposed a low voltage low power CMOS Op-Amp with 90nm technology for high-frequency applications [49]. In this design, the bandwidth was 10GHz with 0.721mW power consumption, where the total harmonic distortion for 100mV input at a frequency of 1MHz was 1.54%. A low-power Op-Amp with a high slew rate has been proposed by B. Panda et al. using an adaptive biasing circuitry with an auxiliary circuit to improve the slew Rate [50]. The Op-Amp was designed by 90nm CMOS technology, where the DC gain was 40.09dB with a slew rate of 31.31V/µs for a load capacitor of 2pF. A CMOS Op-Amp with variable-gain voltage and a feedback current has been presented by F. Esparza-Alfaro et al., where the implementation of this Op-Amp was based on class-AB second-generation current conveyors and exploited an electronically tunable transistorized feedback network [51]. This Op-Amp was designed with 0.5µm technology and a supply voltage of 3.3V with a static power consumption of 280.5µW.

M. Akbari et al. proposed an ultra-low-power CMOS operational amplifier based on flicker noise reduction using a weak inversion technique for recycling folded cascode and folded cascode [52]. This Op-Amp was designed by 0.18µm CMOS technology, where the power dissipation was 480nW. A low-power and digitally programmable Op-Amp using 0.35µm technology has been proposed by I.P. Singh, M. Dehran, and K. Singh [53]. This Op-Amp maintains a constant current and bandwidth for different load capacitors without increasing the standby power consumption.

A.N. Bhatkar et al. presented a low-power Op-Amp operating at 0.4V supply voltage with 90nm technology [54]. In this Op-Amp, adaptive bias circuits were used to increase the slew rate without sacrificing the power consumption. This Op-Amp works in class AB, where the common-mode feed-forward circuit was employed to optimize the Common-Mode Rejection Ratio. Simulation of this Op-Amp has shown that the DC gain was 51.15 dB. The Unity Gain Bandwidth of this Op-Amp was 876.5 KHz with a 77.7° phase margin for 10pF capacitive load and a slew rate of 0.1V/µs. The Common-Mode Rejection and Power Supply Rejection Ratios were 116.9 and 97.30dB, with a power dissipation of 4.78µW for this Op-Amp.

A low-power, two-stage Op-Amp designed with 180nm technology has been proposed by T. Kackar, S. Suman, and P.K. Ghosh to be widely used for on-chip applications [55]. The Op-Amp has been designed using CMOS technology with a power consumption of 1.320mW. K.B. Maji et al. presented a low-power three-stage CMOS Op-Amp using a simplex-PSO algorithm [56]. This algorithm is based on the mechanism of learning, competition, and cooperation, where the primary goal of this design is to optimize the MOS device's dimensions utilizing simplex-PSO to minimize the areas occupied by the circuits.

With the use of a power-efficient charge steering technique, a low-powered Op-Amp designed with 180nm CMOS technology has been presented by R. Ranjan [57], where in this Op-Amp, the power consumption was minimized to 87%. K.J. Raut et al. proposed a low voltage high-gain Op-Amp for low-voltage analog and mixed-signal applications [58]. The Op-Amp was designed using standard 180nm digital n-well CMOS technology with a single supply

voltage of 1.8V. The simulation results of this design showed that the small-signal AC gain was 90.79dB, the slew rate was 11.5V/us, the gain bandwidth was 14.23MHz with a phase margin of 54.8°, and the consumed power of 167µW. In the design of a low-power Op-Amp, B.P. Sharma and R. Mehra proposed a CMOS Op-Amp, designed with 180nm technology by using an amplifier at the gain stage in the saturation region and a difference amplifier at the output stage in the sub-threshold region to achieve high gain and high Common-Mode Rejection Ratio [59]. This Op-Amp achieved an overall gain and Common-Mode Rejection Ratio of 79.16dB and 98dB with a consumption power of 409µW at an input referred voltage noise of 9.65µV/√Hz.

D. Dave Ditucalan and A.C. Lowaton proposed an ultra-low powered Op-Amp using the g_m/I_D method [60]. In this design, the Op-Amp recorded an open loop gain of 60.5dB, phase margin of 64.4°, Unity-Gain Bandwidth of 233 KHz, slew rate of 4.66V/µs, Common-Mode Rejection Ratio of 70dB, Power Supply Rejection Ratio of 74dB and a consumed power of 0.5µW. A low-power CMOS Op-Amp has been proposed by A. Katara et al. operating in the sub-threshold region at 2V power supply and input bias current of 1µA with 0.8µm technology [61].

L.L. Malavolta et al. proposed a design of a low-power Op-Amp operating at a 1.5V power supply with constant transconductance and rail-to-rail operation in 130nm technology [62]. In this Op-Amp, a simple shift level circuit at the input, a self-biased folded cascode as the intermediate stage, and a push-pull output stage have been used to provide a high gain.

The simulation results show that this Op-Amp offers an open loop gain of 125dB with a consumed power of 215µW. The design of ultra-low power Op-Amp operating in weak inversion mode has been reported by F. Akbar et al. [63]. This Op-Amp was designed using CMOS technology with a 1.8V power supply and bias current of 932n. A.S.S. Rajput et al. proposed a low-power, high-gain Op-Amp with 90nm technology for bio-medical applications [64]. The design of this Op-Amp uses a current mirror with a class-A output stage having capacitive Miller compensation. This Op-Amp operates at ±0.75V supply voltage and consumes a total power of 1.83mW with an open loop gain of 90dB. A low-noise, low-voltage, and low-power bulk-driven Op-Amp with a chopper stabilization technique has been proposed by Zhipeng Xiang et al. [65]. This Op-Amp achieves a noise of 400nV/√Hz and offset voltage of 366µV, with 346nW power consumption under 0.5V supply voltage.

By C. Yadav and S. Prasad, a design of a low-voltage, low-power Op-Amp that operates in the sub-threshold region with 180nm technology has been reported [66]. This Op-Amp offers an open-loop gain of 40dB, Unity-Gain Bandwidth of 114KHz, phase margin of 72°, and total power consumption of 112nW with 0.8V power supply. A low-power compact class AB Op-Amp designed by 0.18nm technology and operating with a supply voltage of 0.9V to 1.4V has been proposed by S. Del Cesta et al. [67]. This Op-Amp provides a gain-bandwidth product of 8MHz and a maximum output short-circuit current of 1mA with 120µA quiescent supply current.

V. Raghuveer et al. proposed a low-power Op-Amp using the continuous-time auto-zero technique to reduce the offset voltage for sensing the small analog signals [68]. This Op-Amp was designed using 180nm technology with a supply voltage of 1.8V. The simulation results show that this Op-Amp offers an offset voltage of 2µV, an open loop gain of 131dB, a gain bandwidth product of 1.5MHz, a Power Supply Rejection Ratio of 131dB, and noise of 0.2µV/√Hz with a consumed power of 27µW.

An ultra-low power Op-Amp with high gain and high Common-Mode Rejection Ratio has been proposed by F. Hussain and P. Ray [69]. This Op-Amp has been designed in 45nm technology using a bulk-driven differential pair in the input stage to achieve operation in a low voltage range and increase the Common-Mode Rejection Ratio. In addition, this design employs an auxiliary differential pair to enhance the effective transconductance and achieve high gain and Unity-Gain Bandwidth. The simulation results show that this Op-Amp operates at 350mV power supply and offers a DC gain of 77.03dB, Common-Mode Rejection Ratio of 130.8dB, Unity-Gain Bandwidth of 456.9kHz, and a phase margin of 82.47° with a power consumption of 21.75nW.

T. Mai et al. presented a low-power, low-voltage Op-Amp with a new chopping technique without switching transistors in the high gain path [70]. This Op-Amp was designed using 180nm technology with a 5V power supply. A low-voltage, rail-to-rail Op-Amp with enhanced gain has been proposed by A. Far for energy harvesting applications [71]. This Op-Amp has an open loop gain of 130dB and a bias current of 150nA and operates with a power supply voltage of 0.8V. S.I. Singh presented a low-voltage, two-stage Op-Amp using a feed-forward compensated technique to provide wider bandwidth [72]. This Op-Amp was designed in a 0.18µm technology with a supply voltage of 0.7V, where the simulation results show that this Op-Amp offers a DC gain of 57.4dB, phase margin of 60.3° and unity gain frequency of 4.5MHz for load capacitance of 5pF.

A design for a high-speed CMOS Op-Amp with a low static current consumption has been proposed by N.V. Butyrlagin et al. This Op-Amp was implemented by three CMOS technologies with three foundries: 0.25µm SiGe CMOS, 0.35µm SiGe CMOS, and 0.6µm Si CMOS [73]. L.H. Rodovalho presented a push-pull-based operational amplifier topology for ultra-low voltage supplies [74]. This Op-Amp operates at a 0.5V power supply in the 180nm

technology, with an additional bias circuit that employs an adaptive body bias technique for calibration of output common-mode voltage. A. Faheem et al. reported a low-voltage Op-Amp designed in 180nm technology with current feedback [75]. This Op-Amp operates on the current mode technique and voltage mode technique, with a supply voltage of 1.2V.

S. Chauhan and L.M. Saini proposed a low-power and low-noise Op-Amp using a chopper-stabilized technique, where the proposed design was implemented in 180nm technology with a power supply of 1.8V [76]. Architecture for the low-voltage class-AB output stage was proposed by A. Ria et al. [77] for designing a compact class-AB fully differential operational amplifier operating at a supply voltage of 0.8V and a maximum output current of 7.5 mA with 156μA of quiescent supply current.

A.J. Kumar et al. proposed a high-gain, low-power Op-Amp operating at 1.5V using the class AB output stage [78]. Simulation results have shown that this Op-Amp provides a DC gain of 66.4dB, Unity-Gain Bandwidth of 228MHz, a slew rate of 248.2V/μs, and a Common-Mode Rejection Ratio of 116.6dB with a power dissipated of 74μW. A high-performance, low-power CMOS Op-Amp designed by 90nm technology has been reported by A. Parthipan et al. [79]. This Op-Amp operates at a 1.5V power supply and provides a DC gain of 88dB, Unity-Gain Bandwidth of 1.45GHz, slew rate of 174.2V/μs, Common-Mode Rejection Ratio of 92dB with a power dissipation of 224.8μW. A low-noise, low-power two-stage Op-Amp design using a standard CMOS process has been presented by H. Wang et al. [80]. This Op-Amp was implemented in 0.18μm technology and with a technique of folded cascade input and Class AB output.

Implementation of a CMOS low-power Op-Amp using composite cascode Stages has been proposed by K. Sai Kumar et al. [81]. This Op-Amp operates at a 1.5V power supply with a DC voltage gain of 68.6dB, Unity-Gain Bandwidth of 420MHz at 0.2pF, power dissipation of 114μW, slew rate of 72.8V/μs and a Common-Mode Rejection Ratio of 102.6dB. S. Srivastava and T. Sharma proposed an Op-Amp for high-gain and low-power applications [82]. This design utilizes diverse technologies to improve the Op-Amp parameters such as DC gain, slew rate, Unity-Gain Bandwidth, power consumption, area, and settling time.

A low-voltage two-stage Op-Amp has been proposed by Y.W. Kuo et al. used the RC frequency compensation technique [83]. This technique cancels the pole resulting from the load capacitance using a Miller zero generated by the frequency compensation network. A design of a bulk-driven two-stage Op-Amp for low-power applications has been presented by D. Panchal and A. Naik [84]. In this Op-Amp, the first stage is a non-tailed differential amplifier with bias current control, and the second stage is a common source amplifier with a capacitive load. This Op-Amp operates at 0.3V power supply with a total power consumption of 15.77nW. By L.V. and SEES, a low-power, low-voltage Op-Amp designed by 45nm technology has been reported using incorporating Miller compensation [85]. With the Miller compensation technique, this design works based on a bulk-driven concept for ultra-low power applications. This Op-Amp consumes a power of 262.4077pW with an input supply current of 524.8154pA.

A low-power CMOS operational transconductance amplifier designed by 0.13μm technology has been proposed by N.J. Maia et al. [86]. In the design of this amplifier, paralleled transistors have been added to the input transistors to improve the Common-Mode Rejection Ratio, where this amplifier achieved an open loop gain of 87.34dB with a power consumption of 9.65μW.

K.C. Cajucom et al. proposed a low-power Op-Amp designed in 40nm technology and operating at a 0.6v power supply [87]. This Op-Amp operates in the sub-threshold region with a consumed power of 10μW. A low-power Op-Amp with a high slew rate based on the super-class AB recycling folded cascode has been proposed by A. Yen and B.J. Blalock [88]. This Op-Amp was implemented by 180nm technology, and it employs adaptive biasing and local common-mode feedback for enhancing gain bandwidth, slew rate, and power efficiency. The simulation results show that this Op-Amp offers an open-loop gain of 80.5dB, gain bandwidth of 10.7MHz, slew rate of 202V/μs, and phase margin 60°C.

Stanescu et al. presented a dual low-voltage chopper offset-stabilized operational amplifier with symmetrical RC notch filters [89]. This Op-Amp was designed with a 0.25μm technology and operates at a 1.6-5.5V power supply range. The test results show that this Op-Amp provides a typical offset voltage of 1μV, a Power Supply Rejection Ratio of 128dB, a Common-Mode Rejection Ratio of 120dB, a noise PSD of 42nV/√Hz, and Unity Gain Bandwidth of 1.5MHz. A high-gain, low-power Op-Amp utilizing the BiCMOS class AB output stage has been reported by I.T. Shruthi et al., where this Op-Amp operated at a supply voltage of 3.3V [90].

L. Xie proposed a two-stage low-power Op-Amp with class A and B output stages [91]. This Op-Amp offers an overall output voltage swing of 0.8V and a Unity-Gain Bandwidth of 27.54MHz with a moderate DC bias of 1.4V. A design of a dual-stage CMOS Op-Amp in sky-water technique and with 130nm technology has been proposed by M. Kadam [92]. This Op-Amp operates at a supply voltage of 1.8V and provides a voltage gain of 62dB, Unity-Gain Bandwidth of 20MHz, and output slew rate of 38V/μs with a power consumption of 54μW. The design of a switched-

mode Op-Amp operating at a 0.5V supply voltage has been proposed by J. Al-Hashimi and K. Abugharbieh [93]. This Op-Amp consists of two stages: the first stage is a low supply voltage operational amplifier that utilizes common-mode feedback techniques to eliminate current sources and increase the output voltage swing, and the second stage is a pulse width modulator that transforms the output signal information from voltage to time domain. This Op-Amp was implemented in 28nm technology, where it offers 500MHz pulse width modulation frequency and consumes a power of 1.5mW while achieving a 740mV peak-to-peak differential output voltage swing with a total harmonic distortion of 43.9dB. A design and comparative analysis of a two-stage, ultra-low-power Op-Amp in 180nm, 90nm, and 45nm technology has been presented by S. Nitundil et al., [94]. This Op-Amp achieved an open loop gain of 75dB, a phase margin of 76°, and power consumption of 140nW with a supply voltage of 0.5V.

P. Chandra and U. Bansal proposed a three-stage CMOS Op-Amp designed in 0.18µm technology with high gain and phase margin [95]. This design can drive large capacitive loads and provides an open loop gain of 122dB, Unity-Gain Bandwidth of 2.77MHz, and phase margin of 82.61º. A class AB Op-Amp, designed in 55nm technology, has been proposed by P. Pieńczuk, et al. [96]. This Op-Amp was implemented by a folded-cascode architecture with an inverter output buffer to provide a bandwidth of 2MHz, DC gain of 85dB, and phase margin of 67° with a Common-Mode Rejection Ratio and Power Supply Rejection Ratio of 85.9dB and 62.5dB.

A low-noise and low-power CMOS Op-Amp has been presented by M.A. Dehkordi et al. [97]. This design was implemented by an active feed-forward network based on the current mirror structure using 90nm technology. The simulation results show that this Op-Amp provides a unity-gain frequency of 1.7GHz and open loop gain of 54.53dB with a consumption of power of 2mW and input referred noise of 12.6pA/√Hz. H.J. Park et al. presented an 18µA rail-to-rail class-AB Op-Amp with a high slew [98]. This Op-Amp was designed using the technique of Miller compensation and current limiter for the output stage to provide a slew rate of 30V/µs and consume a low quiescent current of 18µA.

K. Vicuña et al. presented a low-power, low-cost Op-Amp in 0.18µm technology [99]. This Op-Amp consists of three stages designed with Miller compensation, where the third stage acts as an output buffer to drive large loads. The test results showed that this Op-Amp exhibits 20µW power consumption with a 1V supply voltage, Unity Gain Bandwidth of 69.18MHz, an open loop gain of 49.63dB with a phase margin of 86° and a slew rate of 19.87V/µs. A design and analysis of low-power, high-gain amplifiers for DAC application have been presented by S.P. Surabhi and Deepa [100]. These designs include a common source amplifier, differential amplifier, and operational amplifier with different loads such as resistive load, active load, and current mirror. These amplifiers were designed in 130nm technology, where in these designs, it was found that the differential amplifier, with active load using a current mirror, had lower power dissipation of 0.376nW and the operational amplifier had the highest gain of 159.42dB. N. Prokopenko et al., proposed a CMOS Op-Amp with a low level of the systematic component and zero offset voltage, where the computer modelling showed that this Op-Amp exhibits a voltage gain of 80dB [101].

A 0.5V variable gain amplifier using dynamic threshold MOS for ultra-low power applications has been reported by D. Panchal and A. Naik [102]. This Op-Amp was designed with dynamic threshold MOS as the first stage with a cascaded current mirror as a load. The second stage utilized the Miller capacitance compensation method for stability. The Op-Amp was performed in a 180nm technology with power dissipation of 8.35µW, gain range of 19.9dB-35.25dB, bandwidth of 5.16 kHz, and gain bandwidth product of 353 kHz.

C. Stancu et al. presented methods to reduce the offset voltage and power consumption of a two-stage folded cascode Op-Amp [103]. This Op-Amp was designed with a two-stage folded cascode using a differential input stage and an AB class output stage for low power consumption with low offset voltage. A 0.47µW multi-stage low noise Op-Amp employing a 0.2V power supply has been proposed by V. Nguyen-Thien et al. [104].

The proposed Op-Amp was designed in a 180nm technology, where the simulation results showed that this Op-Amp achieved an input-referred noise of 0.9µVrms over a bandwidth of 1kHz, power consumption of 0.47µW, noise efficiency factor of 1.47, power efficient factor of 0.55 over a frequency bandwidth of 10kHz, and closed-loop gain of 40dB with a bandwidth of 200Hz to 10kHz.

6. Conclusion

This paper described the low-power two-stage CMOS Op-Amp that employs the first stage as a differential input amplifier or rail-to-rail input stage and the second stage as a common source amplifier. Compared to single-stage and multi-stage amplifiers, a two-stage CMOS amplifier has a higher voltage gain, higher output swing, wider bandwidth, and higher stability.

However, from the details listed in Tables 1 and 2, it is observed that the proposition of methods used in the design of the low-power, constant-transconductance Op-Amps was on two aspects of technology, the sub-micro-technology that includes scaling down the channel length of the planar

MOSFET into fractions of micron for increasing the channel conductivity and decreasing the power dissipation, and the perfect matching of the MOS devices used in design of the Op-Amp. For the sub-micro-technology, this technology is a complex and expensive process in production. In addition, the short-channel effects and some parameters, such as the non-zero threshold voltage, do not precisely satisfy the need to operate in rail-to-rail and stability of transconductance using this technology. As for the perfect matching of the MOS devices, it is hard to obtain fully matched MOS devices even if they are processed on a monolithic slice of semiconductor because there are some differences in the time recombination of the current carriers between one device and another.

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