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Original Article

Efficient Leakage Reduction Approach for Low Power VLSI Design Using Modified Feedback Sleeper Stack Technique

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Abstract - *In the quest for ever more power-efficient VLSI circuits, mitigating leakage power has become a paramount concern. As the demand for energy-efficient electronic devices continues to surge, low-power VLSI design has become prominent in modern semiconductor technology. One of the most significant challenges in achieving low power consumption is mitigating leakage currents, which have become a substantial contributor to power dissipation in nanoscale CMOS circuits. This paper introduces a novel approach for leakage reduction in VLSI designs. The technique builds upon the principles of traditional stack-based sleep transistors to suppress leakage currents in standby mode but introduces innovative modifications for enhanced efficiency. By strategically combining feedback mechanisms with sleep transistors, this method achieves significant leakage reduction while maintaining excellent area and performance characteristics. The suggested method is evaluated on both the NAND-3 circuit and the C17 benchmark circuit for performance comparison. The utilisation of the suggested power reduction methods involves implementing each circuit with low-Vth, high-Vth, and dual-Vth techniques. The assessment of logic circuits primarily focuses on two critical metrics: leakage power and power delay product. The outcomes of the simulations have conclusively demonstrated that the adoption of high threshold voltage transistors emerges as a highly effective strategy for mitigating static power consumption while incurring minimal delay degradation. The proposed technique holds great promise in the pursuit of ultra-low power consumption, making it a valuable addition to the toolkit of VLSI designers in an era where energy efficiency is paramount.*

Keywords - *CMOS, Deep submicron technology, Leakage reduction, Nanoscale CMOS, Power dissipation, Semiconductor technology.*

1. Introduction

Technological advancements are rapidly evolving, leading to the creation of increasingly sophisticated computing devices that offer users the flexibility to access them from anywhere. Users now demand not only high-speed performance but also affordability. However, these expectations come with constraints related to device size and power consumption. Portable devices such as smartphones and laptops need energy-efficient circuits to meet these demands. Furthermore, modern cell phones are designed to transmit both voice and data seamlessly.

Complex video processing methods and speech recognition algorithms are essential components of modern electronic devices. However, these processes, including video compression, decompression, speech compression, and multimedia file access, consume a significant amount of power, which can pose challenges for power-efficient device design. Simply reducing circuit size is not a sufficient solution, as it can lead to issues with transistor density [1]. To achieve low power consumption in electronic circuits, there is a need for highly efficient architectural designs [2].

Very Large-Scale Integration (VLSI) technology offers a means to create smaller and lighter devices. Within this technology, various architectural approaches have been developed to produce lightweight, high-speed devices with minimal power consumption [3].

According to Moore's law, which has stood the test of time for three decades [4], the density of Integrated Circuits (ICs) rises twice every two years. This development will be possible in 10 more years because of recent advancements in semiconductor production. The International Technology Roadmap for Semiconductors (ITRS) survey found that as circuit complexity increases, a device's static power consumption rises [5]. The ITRS leakage power dissipation curve is depicted in Figure 1.

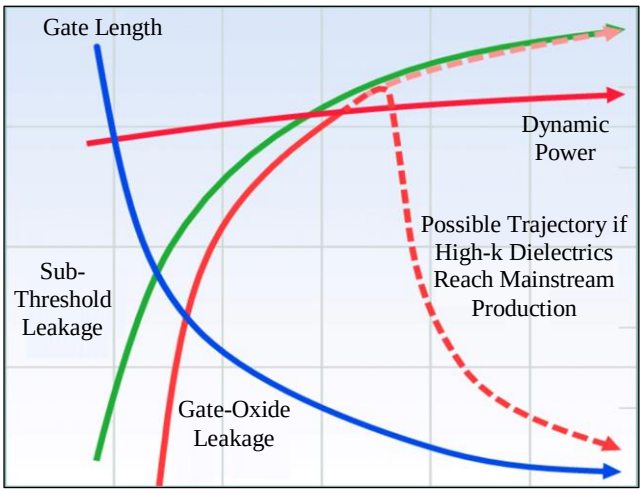

Fig. 1 ITRS trajectory of leakage power dissipation [6]

The graph clearly illustrates a direct correlation between the increase in the device's channel length and the corresponding rise in sub-threshold leakage current. There are various methods used to limit leakage power since the sources of leakage power vary.

The processing speed and battery lifespan of modern electronic devices like computers, laptops, and mobile phones must be high since they must carry out highly complicated processes. The battery drains and the device becomes hot when executing multiple operations at once. Therefore, the devices must be made with circuits that use less energy. Reducing the supply voltage is essential for addressing power dissipation concerns, as the circuit's power consumption varies in response to changes in the supply voltage.

However, it is essential to note that lowering the supply voltage also results in a decrease in the operational speed of the logic circuit. Therefore, the threshold voltage is reduced to avoid this undesirable process. However, due to the sub-threshold current flow through the MOSFETs during this process, there is higher leakage or standby power dissipation [7]. The standby leakage power can even be caused by the presence of switches with very low thresholds. As a result, in order to calculate the power dissipation in a circuit, one must also take standby power dissipation into account in addition to dynamic power. Many strategies have been proposed to mitigate leakage power in low-threshold devices through alterations at both the circuit and process levels.

The design of portable systems and effective processors is a significant challenge in terms of power dissipation reduction in ICs [8]. The power consumption in portable systems affects the battery life. Deep submicron circuit designers must consider a number of important factors, including the rise in leakage currents with VLSI technology scaling [9]. The size of the device gets smaller as VLSI technology advances while the leakage current gets stronger.

The threshold voltage is lowered to significantly increase performance by reducing the leakage current of the device. Device delay is inversely correlated with threshold voltage. Hence, the leakage power plays a substantial role in the total power consumption across active and standby modes of operation. So, to achieve reduced power consumption in low-voltage circuits, it is imperative to mitigate and control leakage power.

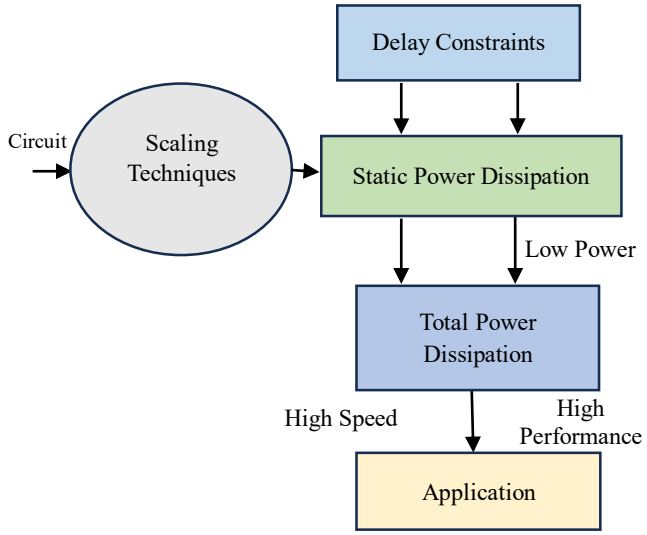

Fig. 2 Hierarchical power reduction approaches

Both process-level and circuit-level strategies can be used to reduce leakage. Leakage reduction at the process level involves fine-tuning various parameters such as oxide layer thickness, well region depth, channel length, and doping concentration. These adjustments play a pivotal role in mitigating leakage currents and enhancing the overall efficiency of semiconductor devices.

Leakage current and threshold voltage can be efficiently regulated in circuit-level techniques by having control over the gate voltage, source voltage, drain voltage, and substrate voltage [10]. Power dissipation rises exponentially with each process generation in VLSI technology due to continuous scaling. This imposes a fundamental restriction on the ability of high-speed processors to expand performance and functionality. Leakage current reduction is crucial in current VLSI technology. Power leakage has grown to such a size that it cannot be disregarded.

Mitigating leakage is a crucial aspect of low-power VLSI design, as it tackles a major hurdle within contemporary electronic devices. As transistors continue to shrink in size, subthreshold leakage currents in CMOS circuits have become a substantial source of power consumption. These techniques, which include power gating, voltage scaling, and advanced transistor design, help mitigate leakage currents when components are in standby mode or idling. By minimising leakage power, these techniques extend the battery life of

portable devices, reduce heat dissipation in data centres, and enhance energy efficiency in a wide range of electronic systems, making them essential for achieving low-power VLSI designs in today's energy-conscious world. In this paper, a practical leakage reduction approach was presented for low-power VLSI design.

The significant contribution of the proposed work includes:

- Efficient leakage reduction method using Modified Feedback Sleeper Stack (MFSS) Technique.
- Efficient leakage reduction technique for low-power logic circuit.

The paper is organised as follows: Section two delves into the literature review and identifies the existing research gaps. In section three, an in-depth overview of the methodology employed in this study was presented. Section four offers a thorough analysis of the outcomes generated by the proposed approach and includes a performance comparison. Finally, in section five, the conclusions drawn from this research were offered.

2. Related Works

T. Santosh Kumar and Suman Lata Tripathi [11] presented a groundbreaking 7T SRAM cell designed for use in 18 nm FinFET technology. The novel approach incorporated the SVL circuit to successfully address and reduce the issue of leakage power in the system. The proposed design demonstrated exceptional performance, setting a new benchmark with the lowest leakage current ever reported, measuring at just 16.56 nA and achieving a remarkable reduction in leakage power consumption, registering at a mere 11.59 nW. This remarkable achievement in reducing both leakage current and power consumption resulted from the synergistic application of LSVL and USVL techniques. The entire circuit design and simulation procedures were carried out utilising Cadence Virtuoso, leveraging the capabilities of advanced 18nm FinFET technology.

R. Krishna and Punithavathi Duraiswamy [12] introduced a novel SRAM cell design with a focus on minimising leakage. This innovative design centres around a source-biased inverter configuration. This novel approach incorporates two additional transistors to reduce leakage power while keeping dynamic power consumption unchanged effectively. The proposed source-biased inverter demonstrated an impressive 66.1% reduction in leakage power at 100°C for the 32 nm technology node and was further evaluated in the 22 nm and 16 nm technology nodes. Moreover, the source-biased inverter was seamlessly integrated into a 10T SRAM cell, replacing conventional 6T SRAM cells at the 32 nm node. This 10T SRAM design exhibited remarkable improvements, with an 86.24% reduction in leakage power at 100°C. Additionally, the introduced 10T low-leakage SRAM cell demonstrated superior stability in comparison to its 6T counterpart, with all simulations conducted using H-spice simulators and predictive technology models.

Neetika Yadav et al. [13] introduced an innovative approach to mitigate leakage power in DML circuits by incorporating Gated Leakage Transistors (GLTs). The method effectively reduces leakage power in footed DML designs, whether used with or without a footed diode transistor. Simulations for NAND, NOR, and full adder circuits at 90 nm and 45 nm technology nodes demonstrated increased efficiency as technology nodes scaled down. The proposed GALEOR algorithms yielded outstanding results, achieving up to 74.1% and 70.7% average power savings in static mode for type A and B topologies, respectively, using the GDML technique. GDMLD provided even more significant leakage power reduction.

Ananth Kumar Tamilarasan et al. [14] presented an innovative technique known as Keeper in Leakage Control Transistor (KLECTOR) for reducing leakage currents in SRAM architecture. During "standby mode," characterised by lower threshold voltage fabric, the leakage current significantly affects SRAM performance. The KLECTOR circuit achieves power savings by constraining current flow through components with reduced voltage drops, predominantly leveraging a self-controlled transistor at the output node.

To enhance power efficiency in SRAM and sequential circuits, C. Ashok Kumar et al. [15] introduced an advanced clock gating strategy. The approach incorporates an extended clock gating mechanism with a D-latch model to reduce power consumption. This improved method refines the conventional clock gating technique to address clock-switching issues like glitches and high clocking activity. It achieves this by introducing clock triggering within the LATCH circuit and inserting a buffer circuit between the source and load circuits. These innovations are applied to sequential counters and SRAM circuits, offering power-saving solutions suitable for a range of practical applications, including FPGA and DSP-specific circuits.

Yasodai and Ramprasad [16] introduced an innovative method for creating CMOS domino logic circuits that leverages a lecturer approach and a modified inverter to reduce leakage power and improve noise performance. A comprehensive study has been conducted involving the design and comparison of NAND and NOR gates, employing both conventional and the proposed techniques. The evaluation was carried out on CMOS designs at 250 nm nodes, with TSPICE simulations performed at a 5GHz clock frequency. The results revealed substantial power reductions, ranging from 25% to 80%, for various logic circuits when using the proposed domino approach compared to traditional domino logic

circuits. Additionally, the proposed method demonstrated a maximum delay reduction of 7% to 20%.

A practical method for reducing leakage power was proposed by Kothamasu Jyothi et al. [17]. The major objective of this work is the implementation of multiple threshold self-controllable voltage level circuits (LSVL and USVL) to curtail leakage power in SRAM 9T cells. Simulation outcomes indicated that the MT-SVL technique outperforms the modified SVL technology in terms of minimising leakage power dissipation. The comprehensive simulations were conducted using CMOS 180nm technology and the Cadence Virtuoso tool.

T. Thamaraimanalan and P. Sampath [18] presented a novel power gating approach aimed at reducing leakage power in adders and multipliers. Power gating, a widely adopted method for mitigating leakage power in CMOS design, was explored among various techniques. The proposed method underwent validation through both fine-grain and coarse-grain power gating strategies. Experimental analyses were conducted to assess the effectiveness of this technique, focusing on metrics such as leakage power and area.

A. Karthikeyan et al. [19] developed a new charge pump and transistor-based leakage reduction domino logic circuit to enhance the functionality of high fan-in circuits. The introduced circuit controls the input of the keeper transistor. The suggested method is also used with two input domino OR gates. The suggested domino OR gate has a lower power delay product than lector with footed diode logic, high speed domino logic, and regular domino OR logic. The suggested method can be used for high fan-in gates and is better suitable for domino OR logic with high speed and low power.

T. Santosh Kumar and Suman Lata Tripathi [20] introduced a 7T SRAM cell designed for low power consumption, minimised leakage currents, and reduced power dissipation. The innovative cell is integrated with effective leakage reduction techniques. Simulation outcomes highlight the 7T SRAM cell as the preferred choice among the compared circuits due to its significantly lower leakage power and overall power consumption.

An innovative technique has been presented by Sufia Banu and Shweta Gupta [21] to reduce the leakage current at various technologies using a 6T SRAM cell. The 6T SRAM cell leakage power is reduced using three source biasing techniques. The three techniques are NMOS, PMOS, and NMOSPMOS diode clamping at 45 nm and 90 nm technology nodes, respectively. The simulation succeeds, and different power dissipations are examined at supply voltages.

Kajal and Vijay Kumar Sharma [22] developed the Cascaded Leakage Control Transistors (CLCT) technology, a novel solution aimed at reducing power losses in active and standby modes, catering to both static and domino logic circuits. The study delves into the impact of technology scaling, utilising models to analyse power dissipation and delay in logic circuits at the 16 nm and 14 nm technology nodes.

The simulations clearly highlight a substantial increase in power dissipation accompanied by more excellent delays at lower technology nodes. This innovation substantially enhances energy efficiency, outperforming traditional methods by a notable margin, achieving a 34.14% increase in energy efficiency.

Fahim Abrar et al. [23] introduced an innovative design approach for dynamic logic circuits, offering substantial reductions in leakage power. The method incorporates delay components and modifies the stacking effect circuitry beneath the PDN to mitigate leakage power. By scaling down the transistors as per this proposal, a significant reduction in leakage power is achieved. Notably, the model outperforms existing models, delivering a minimum 18% improvement in leakage power reduction for wide fan-in gates.

Md Maharaj Kabir et al. [24] developed an innovative, dynamic logic model that effectively reduces both leakage current and propagation delay by incorporating delay components and optimising stacking effect circuitry. The design utilises 45nm PTM technology for OR logic gates and demonstrated robustness through LTSpice simulations.

Compared to existing models, this technique outperforms by achieving a minimum 21% reduction in propagation delay for wide fan-in gates and at least a 5% reduction in leakage current. As a result, this approach is well-suited for applications requiring both low power consumption and high-speed performance.

To enhance circuit design for high processing speed and low power consumption, Sandeep Garg and Tarun K. Gupta [25] introduced the concept of series-connected dynamic node-driven transistor domino logic. This method is applicable in both LP and SG modes. Notably, in the FinFET short gate mode, this approach achieves a remarkable 73.16% reduction in power consumption, while with FinFET technology, it attains a 68.47% decrease. Comparative analysis against existing techniques, using both CMOS and FinFET technology, reveals the superior performance of this suggested circuit in terms of propagation latency, power efficiency, and noise resilience.

2.1. Research Gap

Several approaches can be employed for leakage reduction, but they come with their limitations. Implementing leakage reduction techniques can lead to higher propagation delays and increased chip area, affecting overall performance and efficiency. Traditional methods may struggle to mitigate

half-select and read-disturb problems, which can result in errors and reliability issues during read-and-write operations.

Hot Carrier Injection, Time-Dependent Dielectric Breakdown, and Negative Bias Temperature Instability can pose significant reliability challenges, potentially leading to device failures and reduced lifespan. In advanced device sizes (e.g., 65 nm and below), Negative Bias Temperature Instability becomes a dominant failure mechanism, causing performance degradation over time.

High substrate doping densities in scaled devices can result in band-to-band tunnelling leakage current, contributing to power dissipation and reducing overall energy efficiency. Managing dynamic V_{th} can be difficult, making it challenging to optimise power consumption while maintaining performance. Implementing leakage reduction techniques often increases fabrication costs due to the complexity of design and manufacturing processes. Leakage reduction techniques can add complexity to the circuit design, making it harder to achieve low-power goals without sacrificing performance.

Traditional techniques may have limited applicability as technology nodes continue to shrink, making it harder to achieve significant leakage reduction. These techniques may limit the amount of current that can be handled by the circuit, restricting its usefulness in specific applications. Implementing leakage reduction techniques can extend the design time required for VLSI systems. Leakage reduction techniques may introduce additional noise into the circuit, potentially impacting signal integrity and reliability.

Maintaining the desired state of the circuit can be challenging due to the complexities introduced by leakage reduction methods. Traditional techniques can lead to longer delay times, which can be problematic for real-time or low-delay applications. VLSI systems employing these techniques may become highly sensitive to even minor fluctuations in input voltage.

Circuit performance may heavily depend on the tolerance levels of individual components, making it harder to achieve consistent results. These techniques can impose capacity constraints on VLSI systems, limiting their ability to handle larger workloads. Circuit behaviour may be sensitive to changes in load conditions, complicating power management. Achieving rapid regulation of power consumption can be challenging with traditional leakage reduction techniques. The overall design complexity can increase significantly when attempting to implement effective leakage reduction methods, potentially leading to design challenges.

3. Materials and Methods

The need for efficient leakage reduction techniques in low-power VLSI design is essential for the development of advanced and power-efficient ICs. Leakage power has emerged as a prominent concern in the realm of low-power VLSI design, exerting a significant influence on the system's overall power consumption.

Consequently, there is a growing imperative for the development and implementation of efficient techniques to curtail leakage and enhance system performance. These techniques encompass a diverse range of strategies, including gate sizing, threshold voltage scaling, circuit topology optimisation, voltage scaling, clock gating, and power gating.

They collectively contribute to minimising the current leakage through transistors within the circuit, fostering not only efficiency and scalability but also improved reliability. Furthermore, these approaches have the added benefit of reducing heat generation, further enhancing the circuit's dependability.

3.1. Power Dissipation in CMOS Circuits

Digital logic circuits primarily incur two categories of power dissipation: Dynamic power dissipation and Static power dissipation. Dynamic power dissipation is most pronounced during a circuit's typical operation, particularly at higher operating frequencies. In contrast, static or leakage power dissipation becomes more conspicuous during extended periods of idleness or standby mode.

3.1.1. Static Power Dissipation

The power consumption in a circuit is dictated by the flow of leakage current through its transistors. Specifically, static power dissipation results from the multiplication of the leakage current and the supply voltage [26]. This static power dissipation can be expressed as:

$$P_{static} = I_{static} V_{DD} \quad (1)$$

The main components in static power dissipation depicted in Figure 3 are as follows:

- Subthreshold conduction through OFF transistor (I_1)
- Tunneling current through gate oxide (I_2)
- Leakage through reverse-biased diodes (I_3)
- Contention current in ratioed circuits

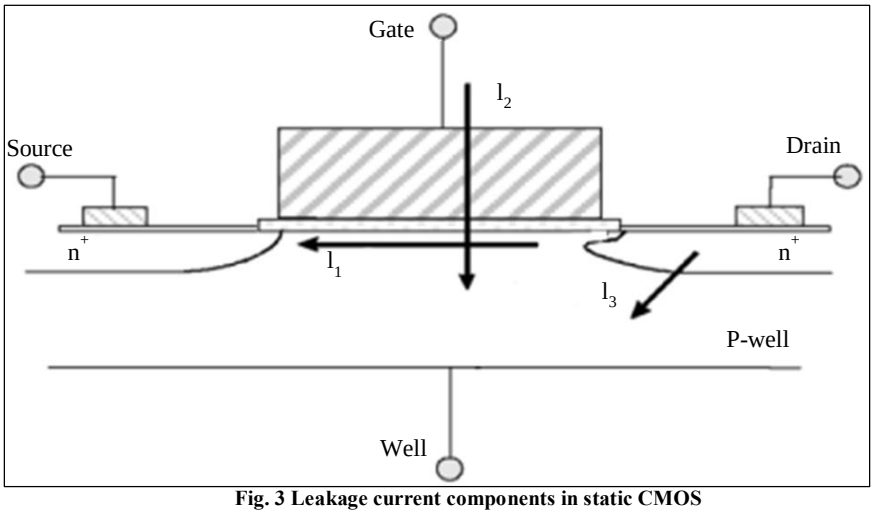

Fig. 3 Leakage current components in static CMOS

3.1.2. Dynamic Power Dissipation

Dynamic power dissipation primarily results from the processes of charging and discharging the load capacitance, along with contributions from short circuit power. This dissipation of dynamic control can be expressed as:

$$P_{dynamic} = \alpha C {V_{DD}}^2 f \quad (2)$$

Where α is the activity factor, C is the load capacitance switched between ground and supply voltage at an average frequency of f_{sw}, f is the clock frequency, and V_{DD} is the supply voltage.

3.2. Proposed Leakage Reduction Technique

Currently, static power dissipation stands as the predominant contributor to the overall power dissipation in low-power VLSI circuits. Due to the leakage components, the static power dissipation increases drastically in the scaled devices. Therefore, in order to minimise overall power consumption, it is crucial to decrease leakage power during both standby and active operational modes.

A Modified Feedback Sleeper Stack (MFSS) technique has been proposed for leakage reduction. This structure is a combination of sleeper transistor and forced stacking techniques, which reduces the leakage current drastically. The sleeper transistor power reduction technique can attain ultra-low power dissipation while losing the normal circuit logic state during the sleep mode of circuit operation.

At the same time, forced stacking power reduction techniques retain the exact logic state with reduced leakage power consumption. The circuit diagram of the proposed MFSS technique is shown in Figure 4.

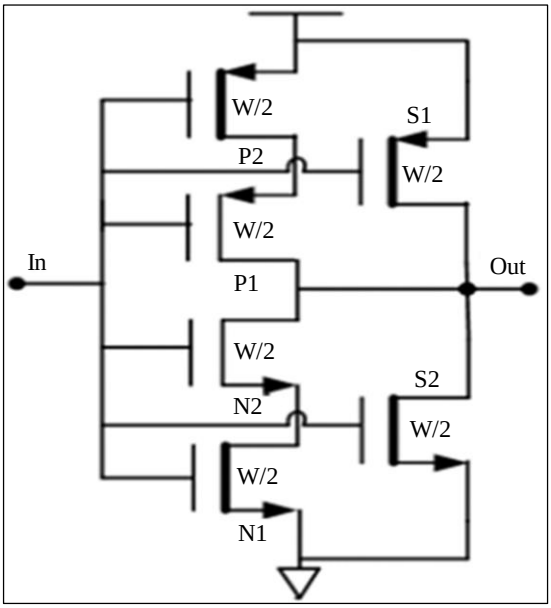

Fig. 4 Circuit diagram of proposed MFSS

In Figure 4, P1 and N2 are the low- V_{th} transistors and P2 and N1 are the high-V_{th} stacked transistors, respectively. Then, the sleep transistors S1 and S2 are connected parallel to these stacked transistors. S1 and S2, when connected in parallel, serve as the high-threshold voltage sleep transistors within the MFSS circuit configuration.

The sleep transistors S1 and S2 receive input feedback from the parallel stacked transistors P1, P2, N1, and N2, corresponding to their respective inputs. As a result, both the sleep and active modes are directly influenced by the input logic states. The flowchart of leakage power reduction using the proposed circuit is shown in Figure 5.

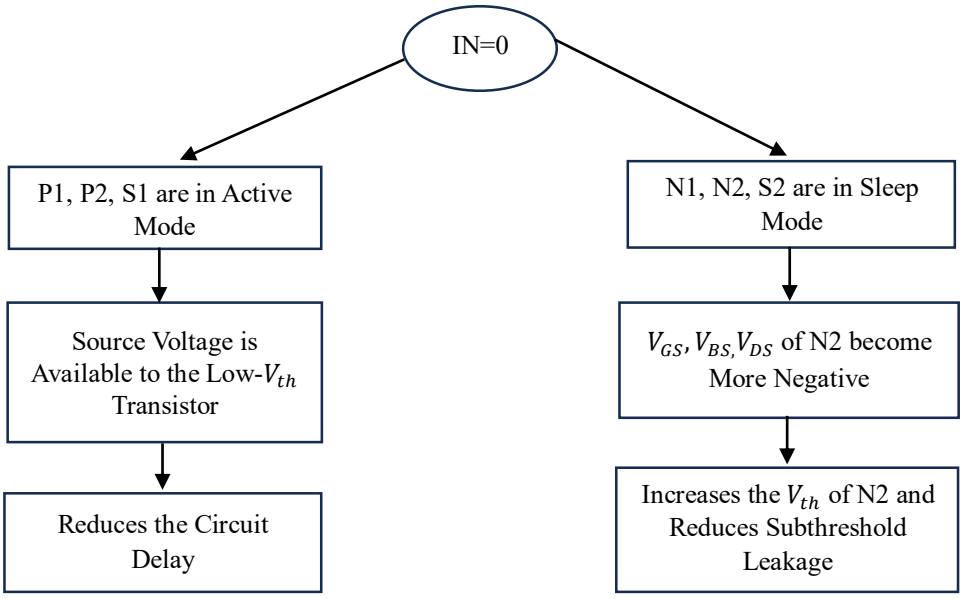

Fig. 5 Basic operation of MFSS

In the scenario where IN is set to 0, P1, P2, and S1 operate in their active mode, ensuring a frequent source voltage connection to the low-V_{th} transistor through the sleep transistor. This parallel connection of P1, P2, and S1 significantly minimises circuit delay.

Simultaneously, NMOS transistors and S2 remain in the switch-off mode, effectively reducing subthreshold leakage. With both NMOS transistors N1 and N2 forced into stacking mode, the intermediate node voltage turns positive, causing V_{GS}, V_{BS}, and V_{DS} of N2 to become more negative. This, in turn, elevates the threshold voltage of N2, leading to a reduction in subthreshold leakage. As the NMOS sleep transistor, S2 features a high-V_{th}, its leakage current is remarkably low. When IN switches to 1, P1, P2, and S1 turn off, while the stacked NMOS, in parallel with S2, switch on, thereby minimising propagation delay.

3.3. Proposed Circuit Application to Logic Circuits

The proposed MFSS technique was employed to implement both a three-input NAND gate and the C17 benchmark circuit. These circuits were constructed using low $-V_{th}$, High$-V_{th}$ and dual$-V_{th}$ power reduction method.

Performance evaluations were conducted considering leakage power and power delay products. Figure 6 illustrates the circuit diagram of the three-input NAND gate created using the MFSS approach.

In Figure 6, a NAND 3 gate is depicted, employing the MFSS technique. In this configuration, the sleep transistors S1 and S2, S3 and S4, as well as S5 and S6, are connected to the inputs A, B, and C, respectively. The overall power consumption is assessed by accounting for all possible input combinations.

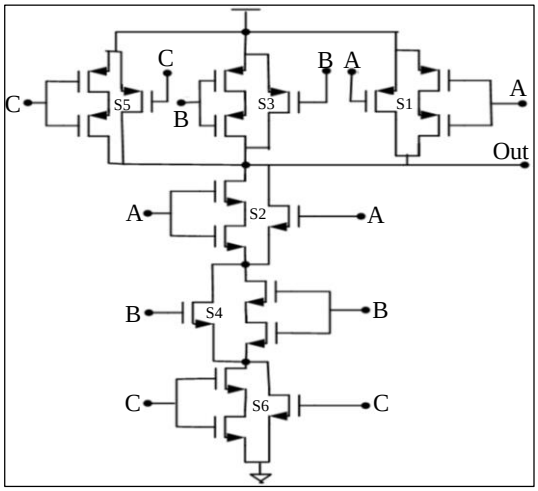

Fig. 6 NAND 3 gate using MFSS

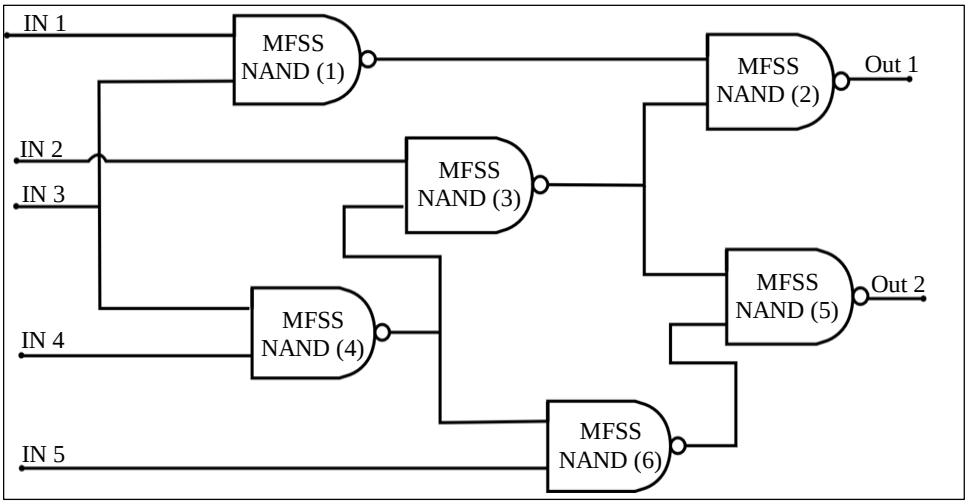

Fig. 7 MFSS C17 benchmark circuit

The evaluation of power reduction through the proposed technique was carried out using the C17 benchmark circuit. Figure 7 illustrates the MFSS C17 benchmark circuit, which comprises six two-input NAND gates realised by the MFSS power reduction approach. This specific circuit is a 72T realisation within the realm of CMOS design.

4. Results and Discussion

4.1. Simulation Setup

The Cadence Virtuoso tool was utilised to create the schematic and layout of the circuit, with a 45nm GPDK model file applied. Subsequently, a netlist was generated from the schematic and utilised in the Spectre simulator to assess power consumption. The total power dissipation was determined by averaging power across various input combinations, encompassing both dynamic and static power components.

The analysis involved considering both high$-V_{th}$ and low $-V_{th}$ scenarios. In the dual $-V_{th}$ approach, high$-V_{th}$ transistors were employed for sleeper transistors and one of the series-connected stacked transistors. For high$-V_{th}$ techniques, only the sleeper transistor adopted a high$-V_{th}$ while all other stacked transistors retained a low$-V_{th}$. In the case of low$-V_{th}$ techniques, both sleeper and stacked transistors were configured with low-$-V_{th}$ settings.

4.2. Simulation Results

The graphical representation in Figure 8 illustrates the comparative results between a NAND 3 gate and the C17 benchmark circuit based on leakage reduction. From Figure 8, it can be observed that dual$-V_{th}$ NAND 3 and C17 show less leakage reduction. The MFSS NAND 3 achieved less leakage reduction compared to the C17 benchmark circuit.

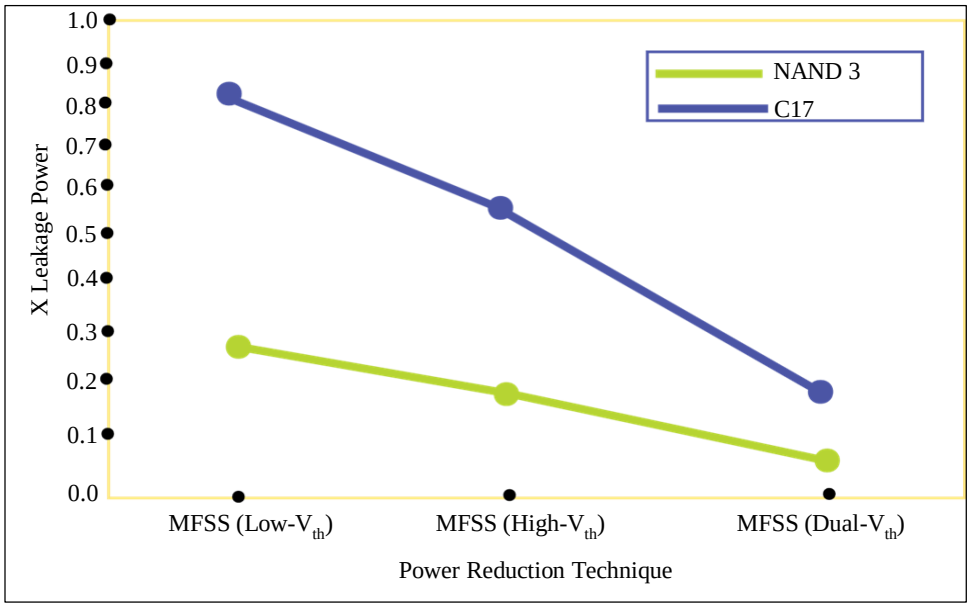

Fig. 8 Leakage power reduction

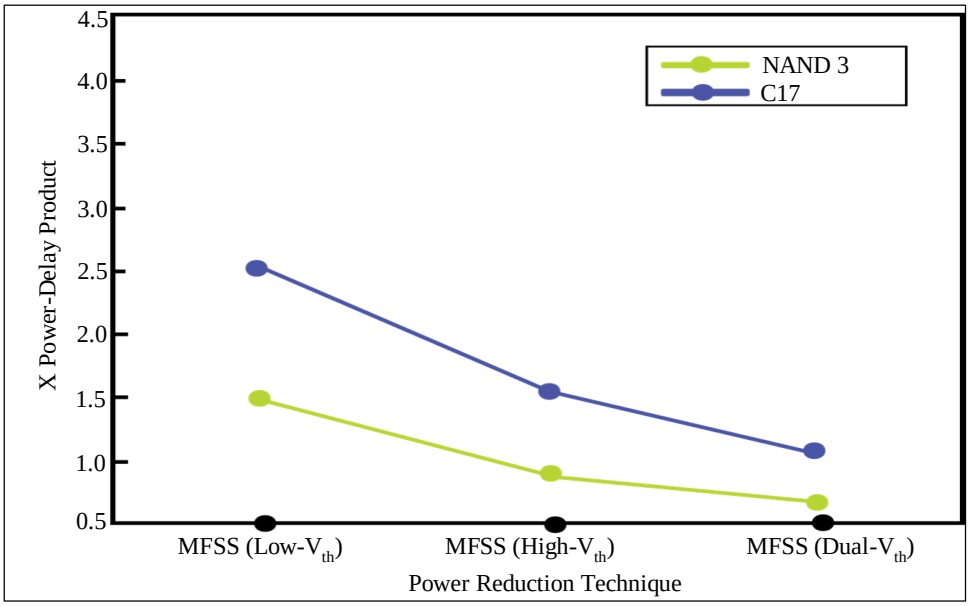

Fig. 9 Power Delay Product

The comparison results of NAND 3 and C17 benchmark circuits based on power delay products are shown in Figure 9. Power Delay Product (PDP) quantifies the trade-off between power consumption and speed performance. A lower PDP signifies a more efficient circuit, as it indicates that the circuit can deliver a given amount of computation with minimal power consumption and reduced delay.

Achieving a lower PDP is of paramount importance as it allows for extended battery life in portable devices, reduces heat dissipation, and enhances overall system performance while complying with strict energy constraints, making it a critical design consideration in the development of CMOS-based integrated circuits. From Figure 9, it can be observed that NAND 3 with MFSS dual$-V_{th}$achieved better PDP reduction compared to the C17 benchmark circuit.

4.3. Comparison of Performance under ISO-Area Scenario

From Table 1, it is clear that in the base case, leakage power is relatively high at 6.00× 10^{-8} W. The proposed technique with low$-V_{th}$ significantly reduces leakage power to 1.73× 10^{-8} W, a 71.2% reduction compared to the base case. When using high $-V_{th}$, the leakage power is further reduced to 4.37× 10^{-9} W, which is 92.8% lower than the base case.

The dual$-V_{th}$ *the* approach minimises leakage power even further, down to 8.02× 10^{-10}W, which is a remarkable 98.7% reduction. These results demonstrate the effectiveness of MFSS techniques, particularly with high and dual $-V_{th}$, in substantially reducing leakage power and thereby enhancing the overall energy efficiency of the semiconductor device.

Table 1. Leakage power comparison of NAND 3 gate under ISO-area scenario

Techniques	Leakage Power (W)	Normalised Value
Base Case	6.00 x10^{-8}	1.00 x10^{+00}
MFSS (Low-V_{th})	1.73 x10^{-8}	2.88 x10^{-1}
MFSS (High-V_{th})	4.37 x10^{-9}	7.28 x10^{-2}
MFSS (Dual-V_{th})	8.02 x10^{-10}	1.33 x10^{-2}

Table 2 shows the leakage power comparison of the C17 circuit under iso-area conditions. In the base case, leakage power is relatively high at 3.81×10^{-7} W. The MFSS technique with low- V_{th} reduces leakage power to 2.21×10^{-7} W, representing a 42% reduction compared to the base case. Using high-low- V_{th}, the leakage power is further decreased to 1.63×10^{-7} W, a reduction of 57.2% compared to the base case. The dual-V_{th} the approach minimises leakage power even more, down to 4.86×10^{-8} W, which is an impressive 87.3% reduction.

Table 2. Leakage power comparison of C17 circuit under ISO-area condition

Techniques	Leakage Power (W)	Normalised Value
Base Case	3.81 x10^{-7}	1.00 x10^{+00}
MFSS (Low-V_{th})	2.21 x10^{-7}	5.8 x10^{-1}
MFSS (High-V_{th})	1.63 x10^{-7}	4.27 x10^{-1}
MFSS (Dual-V_{th})	4.86 x10^{-8}	1.27 x10^{-1}

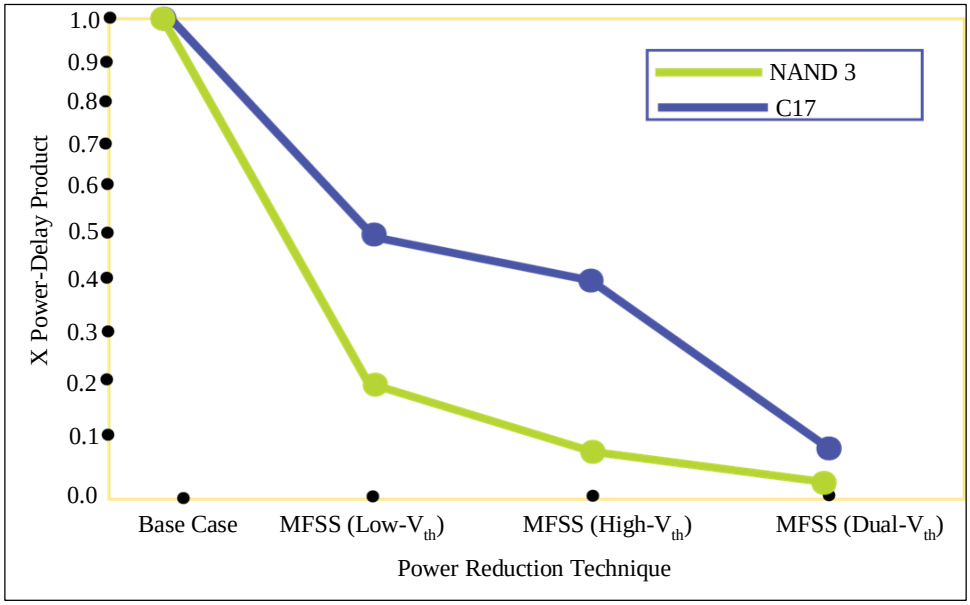

Fig. 10 Leakage power comparison under the ISO-area condition

Figure 10 visualises the leakage power comparison of two circuits under iso-area conditions.

5. Conclusion

Efficient leakage reduction techniques for low power VLSI are of paramount significance in today's technology-driven world. As semiconductor technology continues to advance, the demand for low-power electronic devices becomes increasingly prominent. The importance of efficient leakage reduction techniques cannot be overstated, as they play a crucial role in addressing several critical challenges, such as energy efficiency, battery life extension, and thermal management, in modern VLSI design.

This paper has introduced a novel approach for effectively reducing leakage in VLSI designs. This technique builds upon the foundational concept of using stack-based sleep transistors to curtail leakage currents during standby mode while incorporating innovative modifications to enhance its efficiency. By strategically integrating feedback mechanisms with sleep transistors, the proposed method achieves substantial leakage reduction while preserving both area and performance characteristics. To assess its efficacy, a comparative analysis has been conducted of the proposed technique with a NAND-3 circuit and the C17 benchmark circuit. In each case, the proposed power reduction techniques utilising low - V_{th}, High - V_{th}, and dual - V_{th} methods. The logic circuits were evaluated with a focus on leakage power and power delay products. The simulation results have demonstrated that the incorporation of high- - V_{th} transistors are a particularly effective strategy for reducing static power with minimal delay degradation. In light of these findings, it is evident that the proposed technique holds significant promise in the quest for achieving ultra-low power consumption, making it a valuable addition to the toolkit of VLSI designers, especially in an era where energy efficiency is of paramount importance.

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