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Original Article

A Novel Extended Series Connected Switched Sources 13- Level RSC Multilevel Inverter with Modified Reduced Carrier PWM Technique

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Abstract *- The foremost ambition of the present contribution is to propose a 13-level reduced switch count multilevel inverter with only eight power switches and three diodes suitable for electric vehicle applications. The necessity to reduce the size, expense, and intricacy of multilevel inverters has resulted in the creation of Reduced Switch Count multilevel inverters. The present work implements an Extended Series Connected Switched Sources topology which comprises eight semiconductor devices and three unequal voltage sources. The proposed configuration's ability to reduce the number of semiconductor devices offers a trifecta of advantages: lower costs, a more compact size, and decreased circuit complexity. These benefits not only enhance the practicality and efficiency of the design but also contribute to a more streamlined manufacturing process and improved end-user experience. The operating modes of the proposed topology have been carefully reviewed. The reported configuration is evaluated using a modified, reduced carrier pulse width modulation approach, which has improved the harmonic performance number of comparators, minimizes controller computational burden and produces a better line-voltage harmonic profile than the conventional reduced carrier scheme. To demonstrate the proposed design's improvements, an accurate assessment study with former 13-level topologies is performed, taking into account the number of Insulated Gate Bipolar Transistors, voltage levels, capacitors, total components, diodes, DC sources, and voltage gain. In conclusion, the viability, functionality, and consistency of the proposed layout are evaluated using simulation and hardware setup under various conditions such as load type, power factors, and modulation index variances.*

Keywords *- Extended series connected switched sources, Reduced switch count multilevel inverter, Series-connected switched sources, Pulse width modulation, Insulated gate bipolar transistor, Modified reduced carrier pulse width modulation.*

1. Introduction

Multilevel inverters have played a crucial role in the industrial shift towards their adoption over traditional inverters in recent years. This transition is attributed to several advantages, including reduced Total Harmonic Distortion (THD) in the output waveform, lower switching losses, suitability for high voltage applications, diminished electromagnetic interference, and reduced voltage stresses on devices. Moreover, due to its capacity to function in various applications, Multilevel Inverters (MLIs) prevail over conventional inverters. Particularly at medium and high voltage levels, the MLI delivers the most incredible solution for high-power applications [1, 2].

Specifically, the fundamental topologies of multilevel inverters are the following:

(i) Cascaded H-Bridge (CHB-MLI),
(ii) Neutral Point Clamped (DC-MLI),
(iii) Flying Capacitor (FC-MLI).

A multilevel NPC converter allows for independent regulation of each battery module's current in a DC link, resulting in an equal state of charge across all modules [3]. FCMLI have received more attention due to their voltage-boosting capability without using additional circuits [4]. Another category of MLI, Switched Capacitor MLIs, is limited by the presence of high inrush current during capacitor charging [5]. A CHB-MLI is regarded as one of the most beneficial topologies among the basic configurations due to its modular design, simple control component requirements and related implementation costs [6-8].

They are mainly divided as (a) symmetric, supplied with an equal magnitude of DC voltage sources, and (b) asymmetric, supplied with different values of the DC voltage sources. The higher number of output levels can be acquired from the increased number of sources. The other two types necessitate a greater number of components, and as the number of levels increases, balancing the capacitor voltage

becomes more challenging. Although advantageous, these systems have negative aspects such as unbalanced capacitor voltage, the excessive number of flying capacitors and sensors, and control complexity. The fundamental downside of these architectures is the huge number of power electronic components, especially at high output voltage levels [9-11]. The resultant impact would be high switching losses, size and cost. In an attempt to render the voltage waveform more similar to the shape of a sine wave, the number of levels and steps are elevated in accordance.

Various initiatives have been investigated to enhance the number of voltage levels while utilizing fewer switching devices. Thus, various topologies of RSC-MLI came into existence, considering reducing the number of switches as a key constraint. It also has various boons over traditional two-level inverters, notably the ability to operate at higher voltages using traditional semiconductors, lower common mode voltages, lower dv/dt stresses, a staircase waveform with a better harmonic profile, smaller filter requirements, flexibility to operate at low and high switching frequencies, and fault-tolerant operation. A diverse array of reported RSC-MLI configurations can be classified into different topologies, such as H-bridge and non-H-bridge designs, transformer-based topologies, and switched capacitor-based topologies.

Adopting a Series Connected Switched Sources (SCSS) configuration is driven by the benefits and drawbacks of non H-Bridge setups. In this arrangement, alternating direct current sources are connected in opposite polarities using power switches. To improve alternating output voltage sharpness and reduce switching losses, the present work proposes a topology created by assembling a basic half-bridge chopper module to a Series-Connected Switched Sources (SSCS) design named Extended Series Connected Switched Sources (ESCSS) topology [12].

A variety of control strategies are used to realize topology. The appropriate implementation of a PWM scheme is of the utmost importance in achieving the necessary voltage levels with the fewest number of switches. The most commonly used carrier PWM-based methods, including level-shifted and phase-shift PWM, represent some of the simplest switching logic schemes introduced by Multilevel Inverters (MLIs). However, the simplest PWM schemes (LSPWM and PSPWM) techniques are no longer suitable due to limitations of switching redundancy of RSC-MLIs and a reduced switch count [13].

The realization of RSCMLI's could be made possible with various reported PWM techniques such as multi-reference, switching function and reduced carrier PWM strategies. The primary role of a rectification signal is to produce a stepped waveform that closely mimics certain reference signals. A multi-reference PWM technique is utilized to generate n distinct output voltage levels by using one carrier signal along with (n-1)/2 reference signals. Even though the aforementioned PWM technique applies to all RSC-MLI's its limitation arises towards count of references and deteriorated line total harmonic distortions. To develop a switching function PWM, it is essential to utilize a level-shifted carrier configuration. This setup produces a staircase-switching function, as outlined in an overview table. It enables the generation of the required switching pulses based on the topology.

Switching function: PWM requires the use of a level-shifted carrier arrangement to create staircase switching functions that are followed by an overview table, which allows the achievement of desired switching pulses from topology. This scheme creates switching pulses by integrating each carrier's minimum and maximum limits. On the contrary, in order to achieve the desired switch action on an inverter, reduced carrier PWM consists of a (n-1)/2 unipolar level shifted carrier arrangement and a modulation signal arrangement, which requires user Defined Logical Gate Layouts with Unified Logic Expressions to realize n-level inverter [14, 15].

The present study exhibits a novel PWM scheme for implementing the proposed configuration, which combines decreased carrier and switching function PWM to realize the required topology. Therefore, the reported structure considers the integrated benefits of simplified carried arrangement and symmetrical switching logic for reduced carrier PWM and unified implementation of switched function PWM.

The organization of the paper is outlined as follows: Section II demonstrates the brief description of the proposed topology, Section III presents the execution of the modified reduced carrier PWM strategy and modes of operation of the proposed structure, and Section IV showcases the simulation and experimental performance outcomes of the implemented design. Section V is an abbreviated comparative analysis of various 13-level RSC-MLI's and proposed design. In the end, the conclusion and references are presented.

2. Proposed Topology

2.1. Topological Description

The proposed ESCSS topology is shown in Figure 1. It is developed by assembling a simple half-bridge chopper structure to the conventional SCSS configuration [16, 17]. The implemented setup comprises eight power semiconductor switches, including six unidirectional switches, two auxiliary switches, and three distinct DC voltage sources.

V_1, V_2, and $V_{h,}$ out of which two DC voltage sources are connected in two different horizontal arms. The chopper module selects the DC source value as half the main source value. The deciding factor to obtain even and odd levels is to turn ON and OFF switches in a half-bridge circuit.

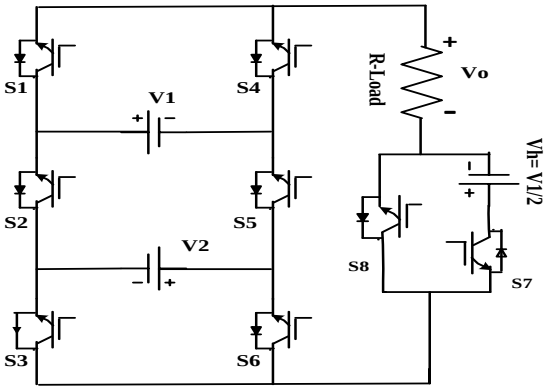


Fig. 1 Proposed configuration

The switches of the chopper module are activated sequentially to prevent a short circuit. This affirms that the proposed configuration can be used for higher levels without substantially boosting the device ratings and without impacting the maximum output voltage. The proposed topology provides multiple advantages over other setups, such as fewer switches needed to achieve more output voltage levels, decreased Total Harmonic Distortion (THD), and reduced switching and conduction losses.

3. Modulation Strategies

The evolution of RSC-MLI has reduced the number of MLI switches, reducing redundancies and changing topologies. As a result, traditional MLI switching schemes (LSPWM and PSPWM) are no longer suitable for RSC-MLI operations [13]. The choice of appropriate implementation of the PWM technique is highly important in acquiring desired voltage levels with the lowest number of switches.

However, PWM adopted to regulate RSC-MLI comprises two crucial factors: Carrier-Modulating Signal Configuration and Switching Logic. Carrier-based PWM schemes have been reported as the most simplified PWM schemes in the literature [18].

Among the reported carrier-based PWM approaches, a multi-reference technique is of the initial category, which involves comparing a number of reference signals and a single modulating signal, and the result is the creation of switching pulses to realize the various topologies [14]. Although many arrangements are being made, this category is restricted to few RSC-MLI as it produces poor THD of line voltage.

The next category of the PWM scheme is the switching function scheme which creates pulses by integrating each carrier's minimum and maximum limits into the system and also more number of comparators. However, this leads to the complexity of the module. To overcome the negativities of the aforementioned methods, an effective pulse width modulation scheme came into existence, namely the reduced carrier PWM technique [19]. It is the most widely utilized and least complicated as it uses half the number of carriers (n-1)/2 dissimilar to (n-1) carriers in conventional schemes to produce n-level inverter.

A switching pulse is obtained by comparing the unipolar reference to the boundaries of carrier 1. This pulse generates a 0-V voltage band in-phase voltage. A pulse is generated when the unipolar reference exceeds carrier 2, which is established by comparing the unipolar reference with carrier 2. This results in a voltage band between V and 2V in phase voltage. The same procedure is applicable to acquire switching pulses of higher levels. Each pulse generates a unique voltage band. As the modified reduced carrier PWM type shows admirable harmonic performance compared to the conventional reduced carrier scheme, present work favors it [20].

The modified, reduced carrier arrangement is illustrated in Figure 2 to actualize the 13-level inverter. The programmatic description of the modulation scheme of the proposed design is such that carriers are arranged from 0 to (n-1)/2. Each carrier is compared with uni-polar reference to secure switching pulses in such a way that it goes high for reference greater than carrier waveform to produce a phase voltage band. The switching pulses obtained when added up using an additive option result in a staircase waveform from 0 to (n-1)/2, as shown in Figure 3.

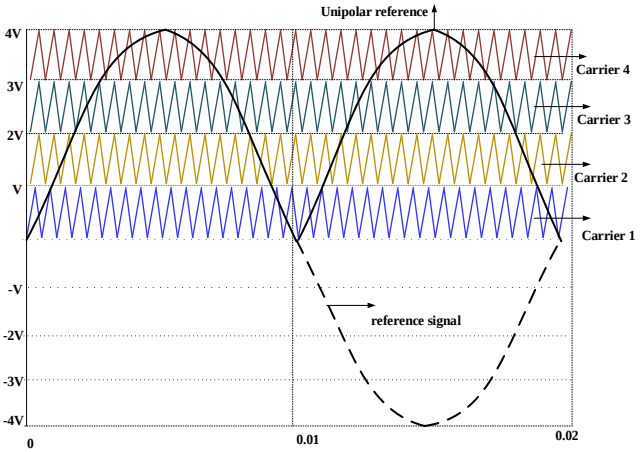


Fig. 2 Carrier arrangement

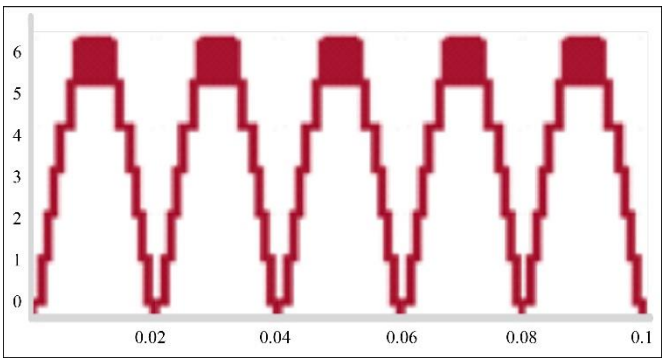


Fig. 3 Staircase waveform

Each band is compared with a constant from 0 to (n-1), and the resultant pulse would be applied based on the look-up table to produce gate signals to control 13 level inverter.

3.1. Operating Modes

The operating concept of the proposed design can be interpreted using thirteen unique modes, as shown in Table 1. It emphasizes the look-up table results in switching combinations of ESCSS topology, which produces thirteen levels of load voltage. The switching configuration demonstrates the operation of the proposed topology as a thirteen-level inverter with a peak output voltage of $\pm(V_1+V_2)$ supplied with unequal V1, V2 and Vh voltages. Overall, Table 1 serves as a valuable resource for understanding the operational capabilities of the thirteen-level inverter, providing a clear and organized representation of how various combinations of DC sources can be utilized to generate a wide range of output voltage levels while also considering the implications of redundancy in the system's design. The various modes of operation of the implemented design are demonstrated in Figures 4, 5, and 6 in both positive and negative directions.

The operating modes of the proposed design are as follows:

Mode I ((V_1+V_2) level generation): A (V_1+V_2) level is generated by the switch on the combination of S_1, S_2, S_3, S_5 and S_8 switches as presented in Figure 4(a). In this state, DC sources (V_1 and V_2) supply current to the load.

Table 1. Switching states of the proposed topology

S. No.	Level voltage	Switching Path
1.	V_1+V_2	S1-S5-S3-S8
2.	V_2+V_h	S3-S5-S4-S7
3.	V_2	S3-S5-S4-S8
4.	V_1+V_h	S1-S7-S6-S5
6.	V_h	S1-S7-S3-S2
7.	0	S1-S8-S3-S2
8.	$V_h- V_1$	S2-S3-S7-S4
9.	$-V_1$	S2-S3-S8-S4
10.	V_h-V_2	S1-S2-S6-S7
11.	$-V_2$	S1-S2-S6-S8
12.	$-(V_2+V_h)$	S4-S2-S6-S7
13.	$-(V_1+V_2)$	S4-S2-S6-S8

Mode II (V_2+V_h level generation): To attain an output voltage (V_2+V_h) in this operational state, switches S_3, S_4, S_5 and S_7 are activated simultaneously. The corresponding circuit diagram for this configuration is presented in Figure 4(b).

Mode III (V_2 level generation): This operational state results in an output voltage magnitude of V2, attributed to the concurrent activation of switches S3, S4, S5, and S8. The relevant circuit diagram for this configuration is illustrated in Figure 4(c).

Mode IV ((V_1+V_h) level generation): To attain an output voltage V_1+V_h in this operational mode, switches S_1, S_5, S_6 and S_7 are activated concurrently. Figure 4(d) shows a circuit diagram exhibiting this setup.

Mode V (V_1 level generation): Switches S_1, S_5, S_6 and S_8 conduct, and the voltage across the load terminals is V_1. Figure 4(e) shows a circuit schematic that illustrates this approach.

Mode VI: (V_h level generation): The conduction path for generating the V_h voltage level is shown in Figure 4(f). Switching combinations to generate V_h voltage levels are S_1, S_2, S_3 and S_7.

Mode VII (zero level generation): Figure 5 illustrates a conduction channel leading to zero voltage. Switches S_1, S_2, S_3 and S_8 are activated to achieve zero voltage.

Mode VIII ((V_h-V_1) level generation): This operational condition results in an output voltage magnitude of (Vh-V1) as a result of the simultaneous activation of switches S2, S3, S4, and S7. The related circuit diagram for this configuration is illustrated in Figure 6(a).

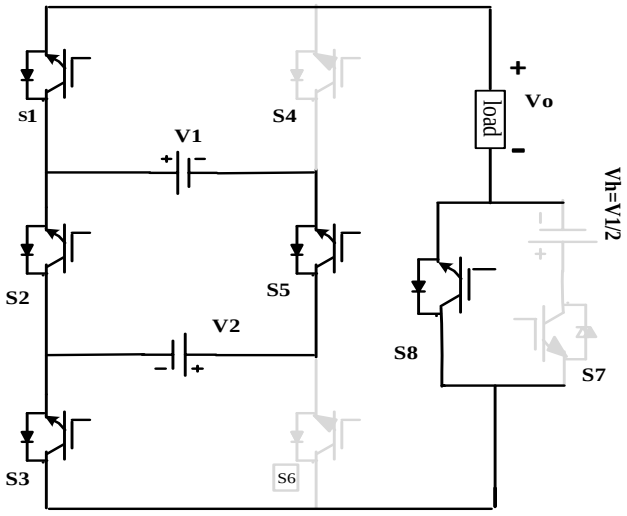
Mode IX: ($-V_1$ level generation): Switches S_1, S_5, S_6 and S_8 conduct, and the voltage across the load terminals is V_1. Figure 6(b) shows a circuit schematic that illustrates this approach.

Mode X ((V_h-V_2) level generation): To attain an output voltage (V_h-V_2) in this operational state, switches S_1, S_2, S_6 and S_7 are activated simultaneously. The circuit diagram that corresponds to this configuration is illustrated in Figure 6(c).

Mode XI ($-V_2$ level generation): This operational state achieves an output voltage magnitude of ($-V_2$) by simultaneously activating switches S_1, S_2, S_6 and S_8. The corresponding circuit representation for this model is presented in Figure 6(d).

Mode XII ($(V_h-V_2-V_1)$ level generation): To attain an output voltage ($V_h-V_2-V_1$) in this operational mode, switches S_2, S_4, S_6 and S_7 are activated concurrently. Figure 6(e) shows a circuit diagram exhibiting this setup.

Mode XIII ($-(V_2+V_1)$ level generation): This operational condition results in a specific output voltage magnitude of $-(V_2+V_1)$ by simultaneously activating switches S_2, S_4, S_6 and S_8. Figure 6(f) shows a circuit schematic that illustrates this approach.



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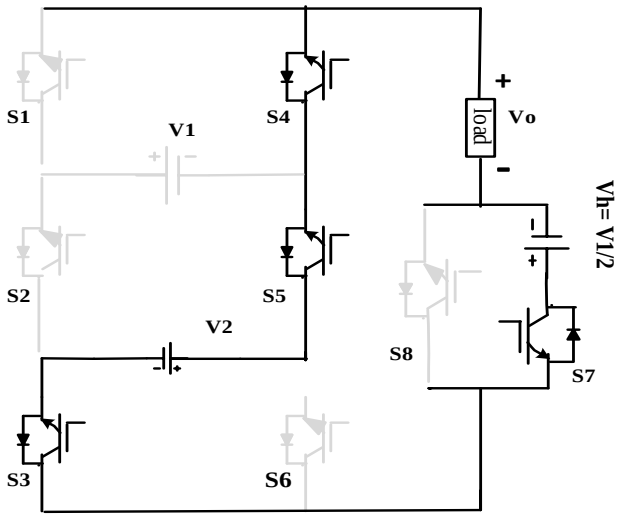

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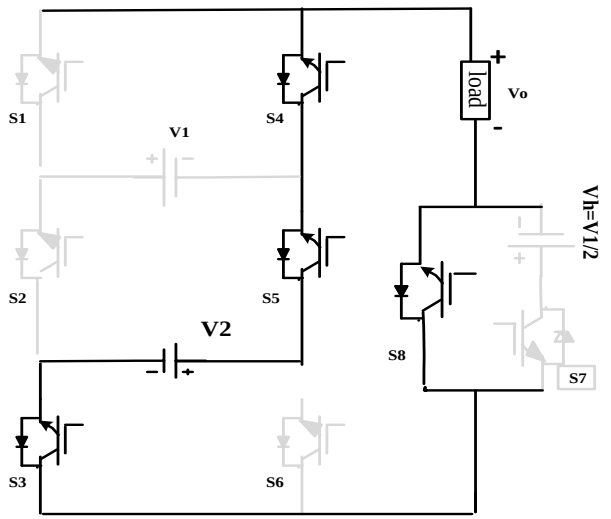

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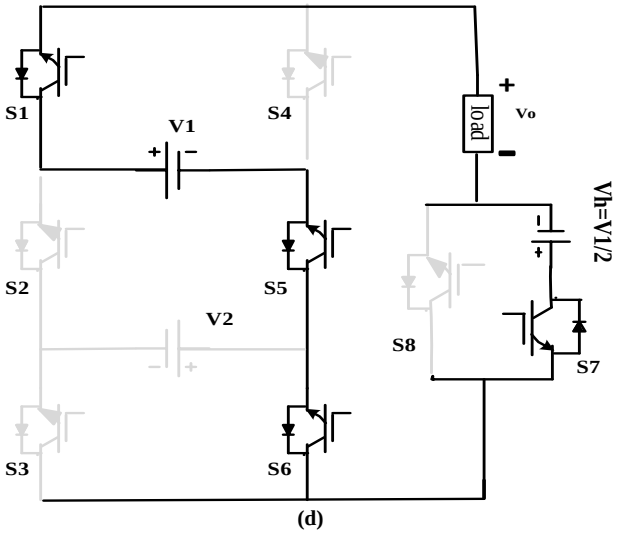

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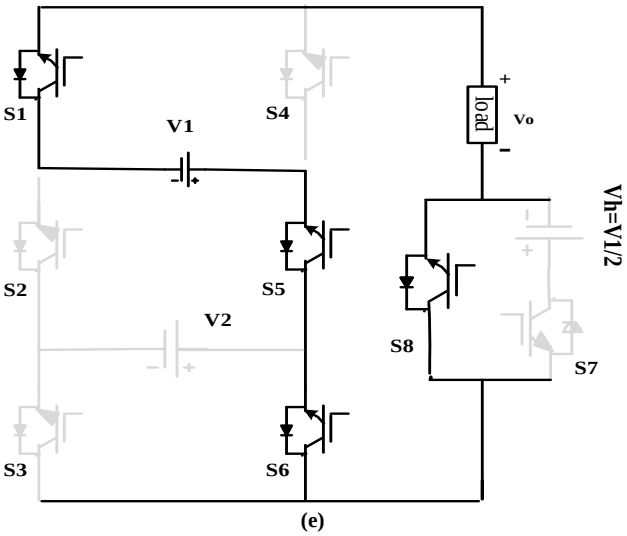

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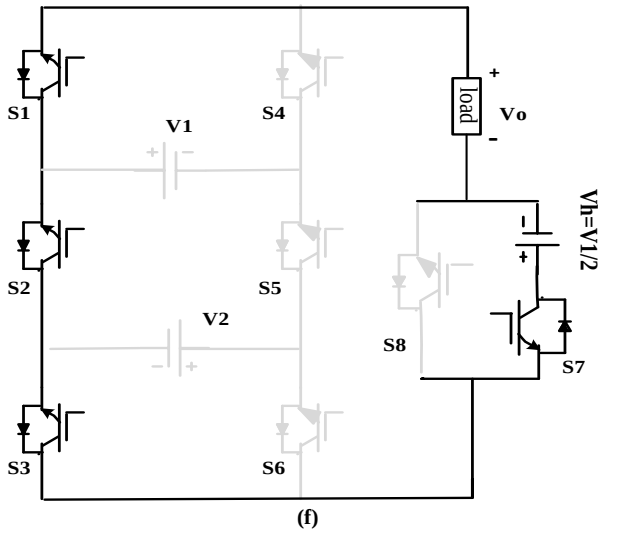


(f)

Fig. 4 Positive output voltage levels

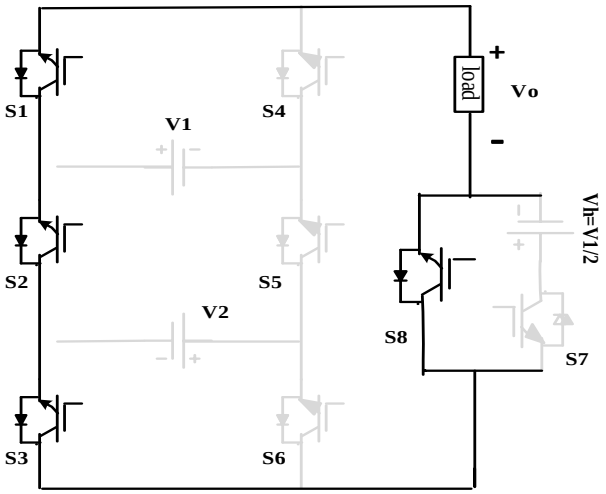
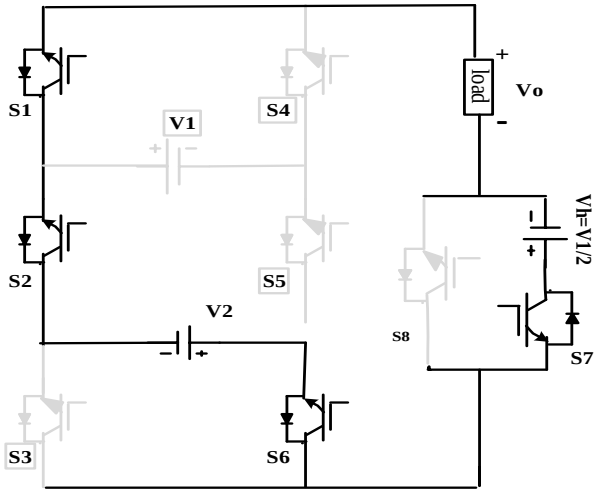


Fig. 5 Zero output voltage level



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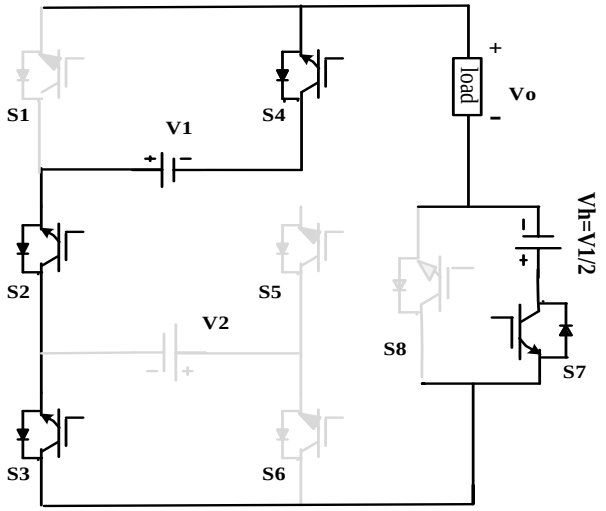

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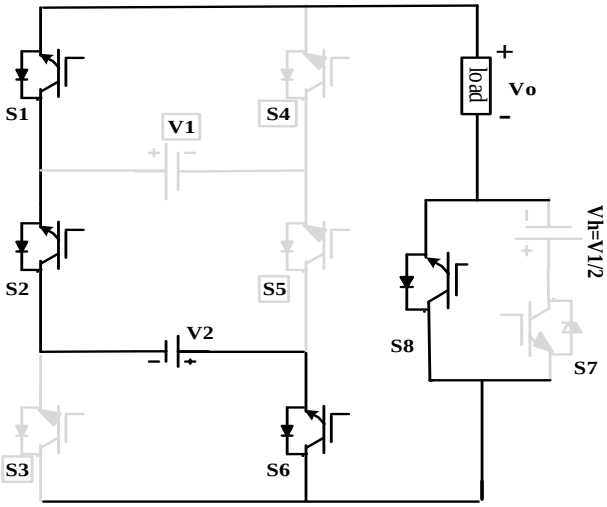

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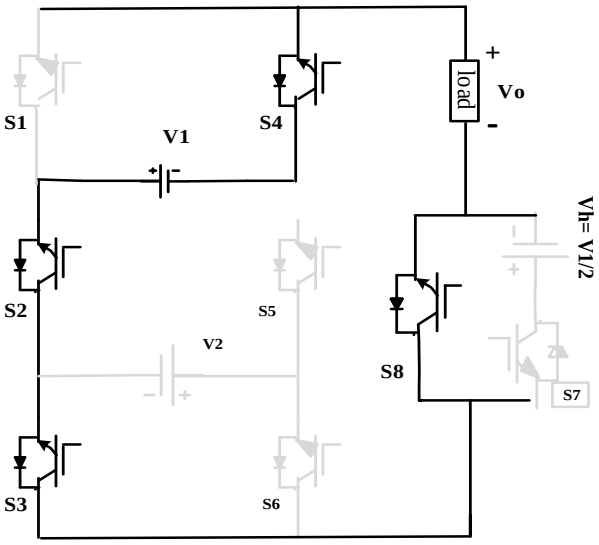

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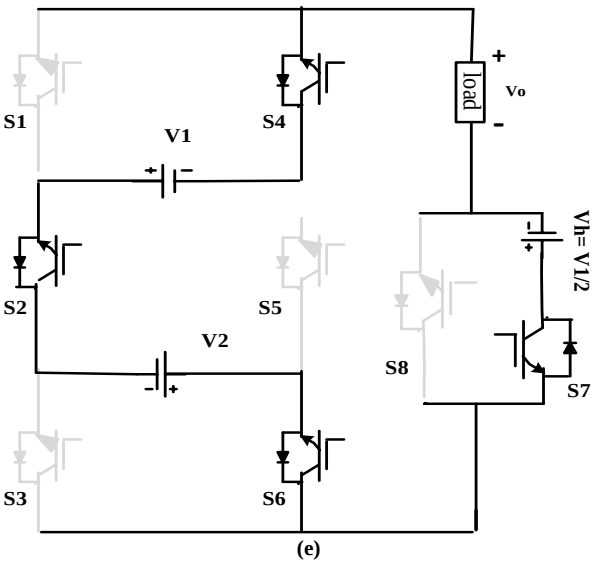

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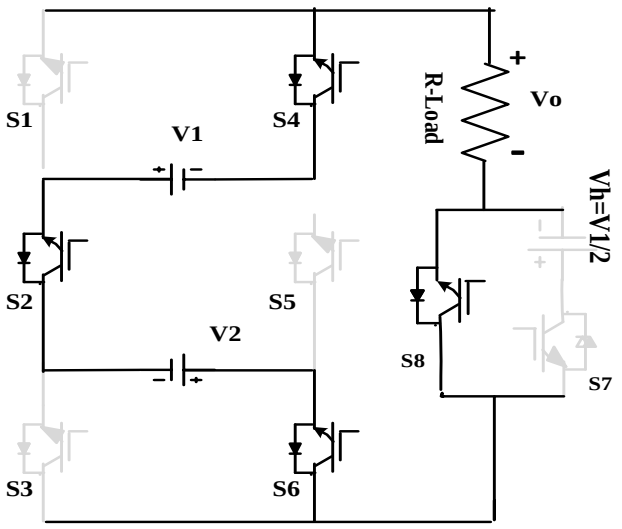


(f)

Fig. 6 Negative output voltage levels

4. Performance Analysis

4.1. Simulation Results

Numerous familiar modulation strategies have been examined, and a suitable arrangement that exhibits lower THD is selected for the proposed configuration. In this section, the design is analyzed using a modified, reduced carrier modulation scheme.

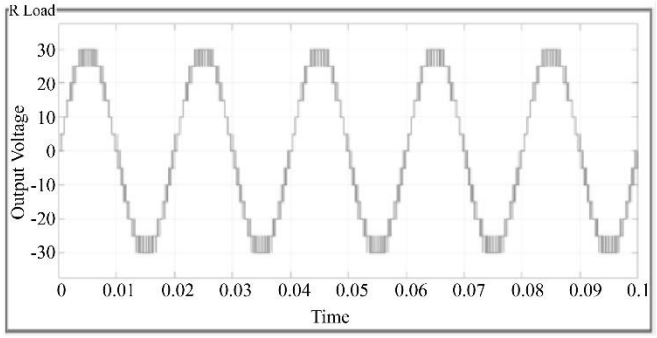
The specifications and components of the proposed topology are shown in Table 2. The entire evaluation is performed using MATLAB/SIMULINK, a robust simulation tool that facilitates detailed modeling and analysis of dynamic systems. This software allows for the visualization of system responses under different scenarios, enhancing the understanding of how the proposed configuration performs across a range of power factors, modulation indices, and switching frequencies.

The insights gained from these simulations will be instrumental in the design and optimization of the configuration for real-world applications. The thirteen-level output voltage attained for unity and lagging power factors is demonstrated in Figure 7. The output current waveforms across the load considering the aforementioned parameters, are depicted in Figure 8.

The total harmonic distortion for various values of cosine angles and amplitude modulation index m_a are displayed in Figure 9 and its values are 6.93% and 6.96% at amplitude modulation index m_a=0.97 and m_a=0.98. The proposed PWM could scatter power evenly without damaging phase or line voltage harmonics, as shown in Figure 9. It proves the reported PWM's potential to deliver good harmonic performance, analogous to level-shifted PWM with In-Phase Disposition (IPD).

Table 2. Simulation and experimental parameters

Notation	Parameters	Specifications
V_1	Input DC Voltage	10V
V_2		20V
V_h		5V
f_{sw}	Switching Frequency	2KHz, 5KHz
f_o	Output Frequency	50Hz
m_a	Amplitude Modulation Index	0.97, 0.98
R, L	Load	10Ω, 50Ω, 5mH, 10mH
IGBTs	Switches	FGW40XS120C



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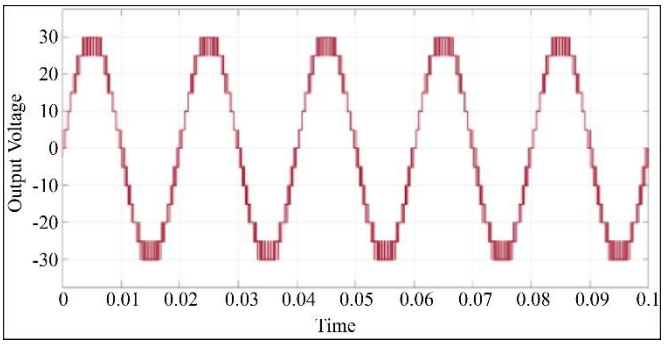
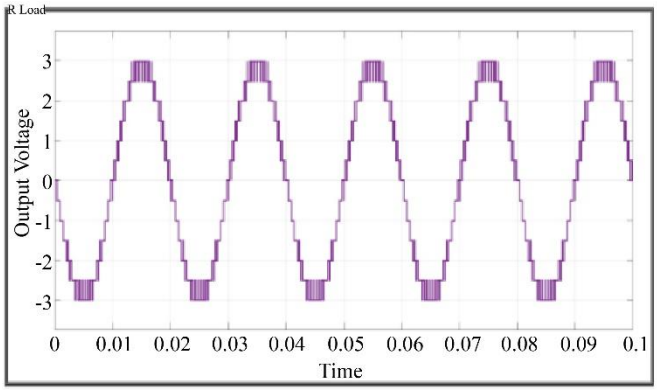


(b)

Fig. 7 Output voltage waveforms at (a) Unity, and (b) Lagging power factor.



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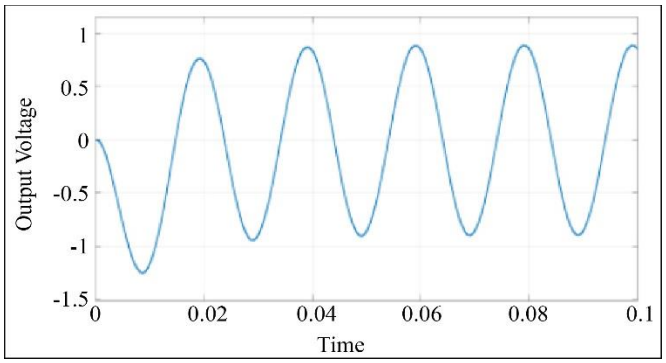
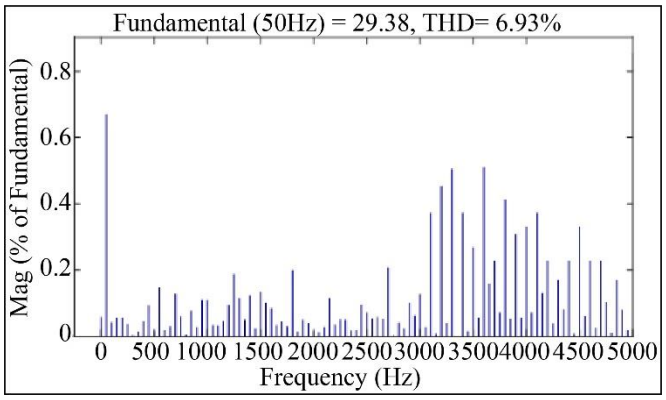


(b)

Fig. 8 Output current waveforms at (a) unity power factor, and (b) lagging power factor.

Figures 10(a), 10(b), and 10(c) show control signals for switches s_1, s_2 and s_3. Figures 10(d), (e), (f) depicts gate signals for s_4, s_5 & s_6. Figures 10(g) and (h) show the gate pulses for s_7 s_8. It is to be noted that device ratings have been reduced to a maximum extent which results in lower switching and conduction losses. The proposed ESCSS RSCMLI design was validated and demonstrated as feasible and effective using both the simulation environment of MATLAB/ SIMULINK and an experimental platform.



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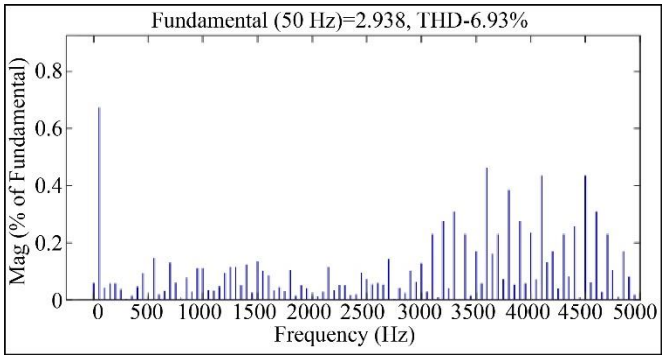

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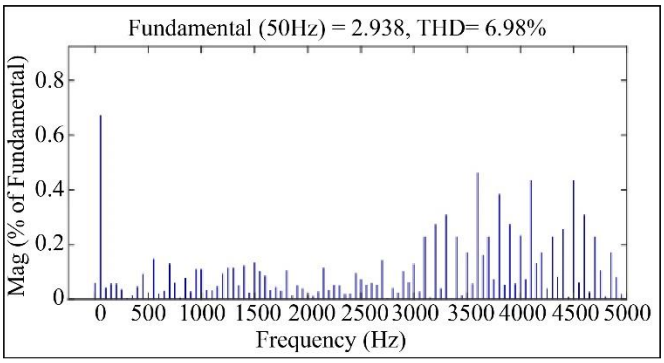

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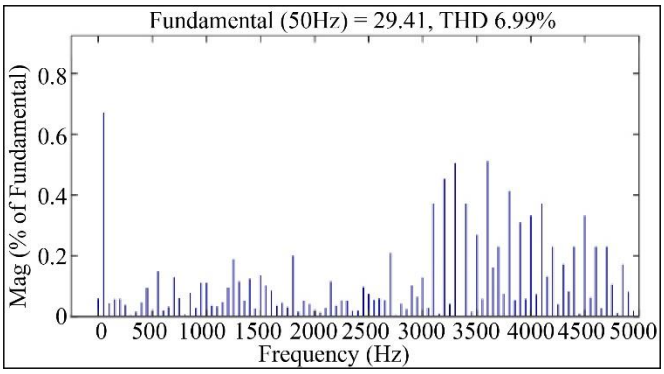
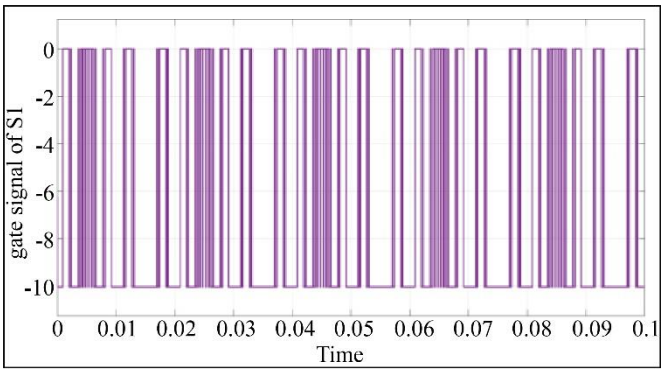
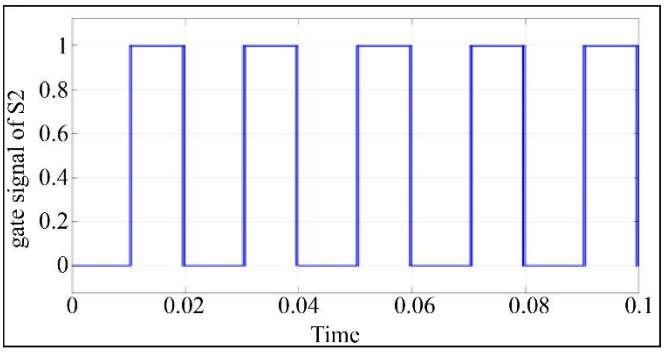


(d)

Fig. 9 THD performance of proposed topology



(a)



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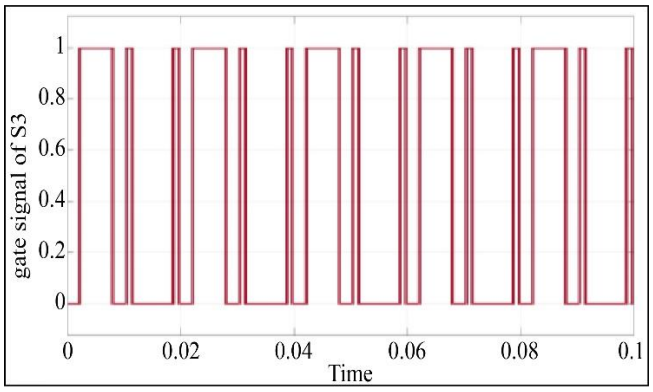

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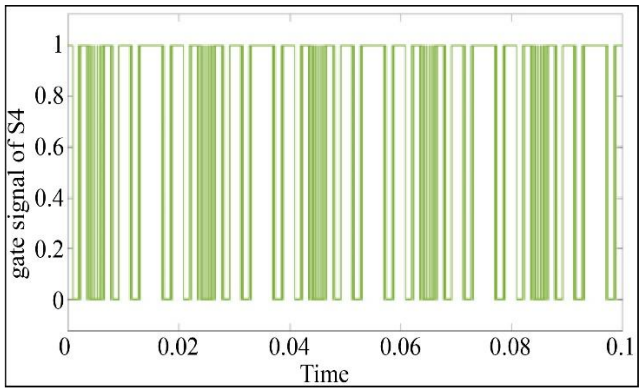

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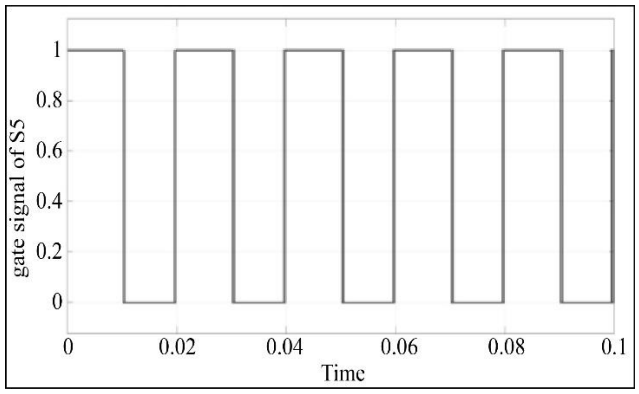

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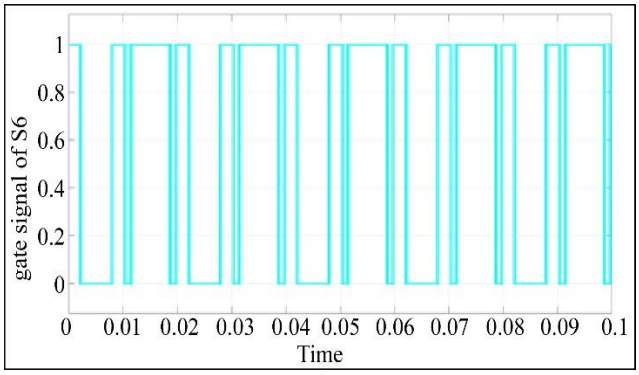

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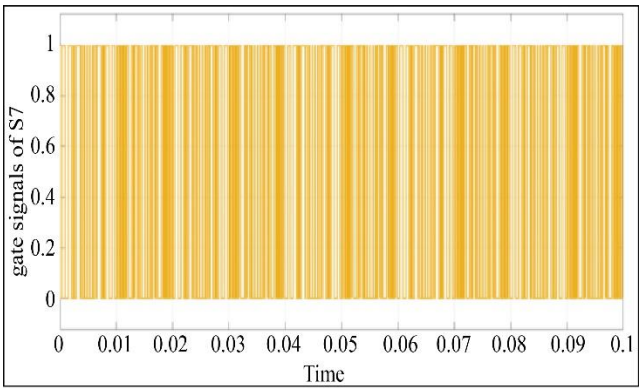

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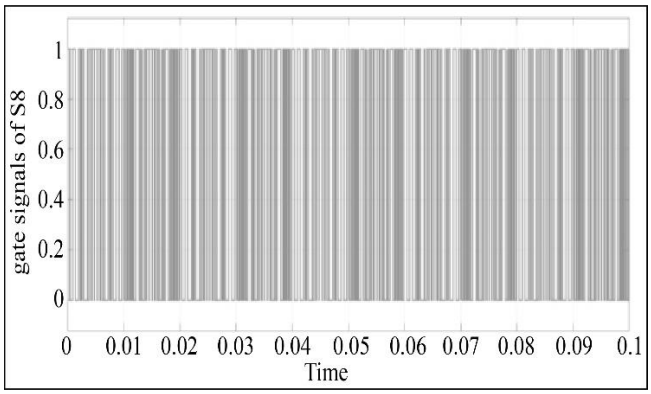


(h)

Fig. 10 Control signals of IGBTs

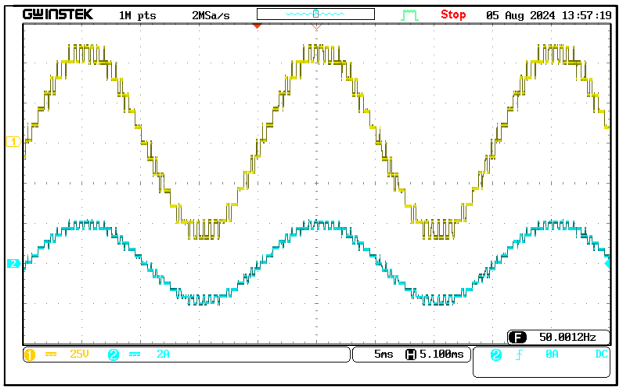
4.2. Experimental Analysis

In order to evaluate the topological performance, a laboratory prototype has been designed using the parameters indicated below. The experimental setup presented in Figure 11 for the suggested prototype demonstrates its feasibility, efficacy, and dependability.

Fig. 11 Hardware module of ESCSS topology

The IGBTs used in the setup are FGW40XS120C. It has properties of 1200V ratings, -20 to 20 V gate emitter voltages. The configurations uses three independent source voltages, V1, V2, and Vh, to provide a maximum output voltage of 25 to 30 volts. The complete cycle comprises of 13 output voltage levels with 6 positive and negative levels including zero level.

Additionally, the switching frequency ranges from 1kHz to 10kHz, loads adopted in prototype dynamically changes from resistive to reactive values. By Reducing the harmonics, recordings of the system are as follows: output voltage V_o = 25V, load current I_o = 2A, frequency f=50.002Hz with unity and lagging power factors. Figure 12 illustrates the recordings of the output voltage and output current of experimental prototype at unity power factor for various time durations. Furthermore, Figure 13 depicts the practical outcomes of load voltage and current at a lagging power factor.



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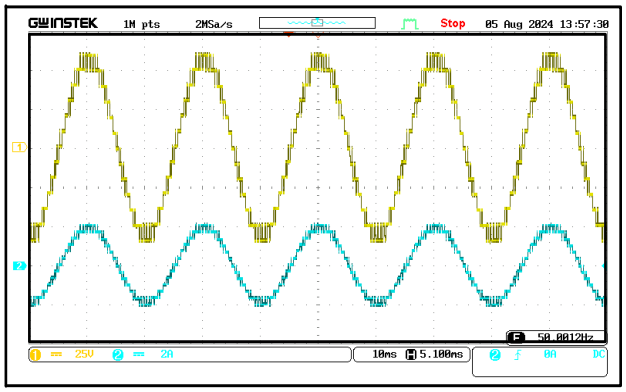

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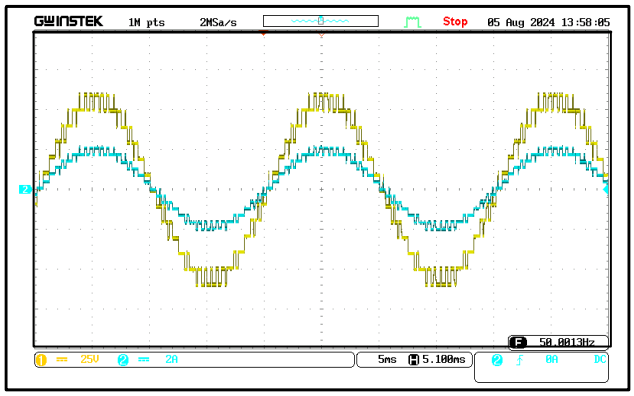
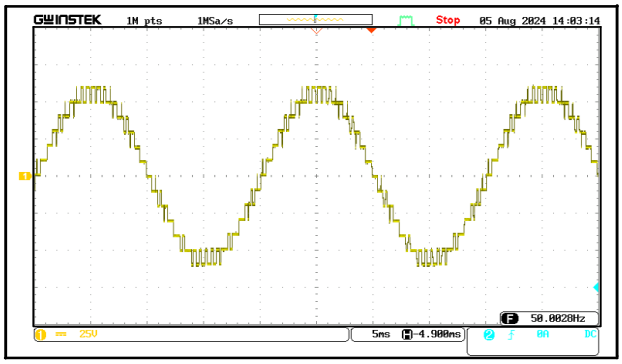


(c)

Fig. 12 Output voltage and current waveforms at unity power factor



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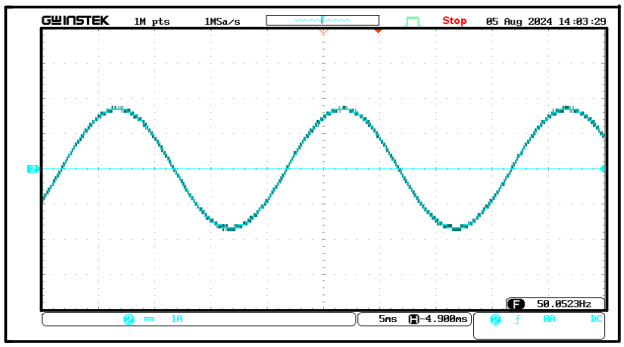

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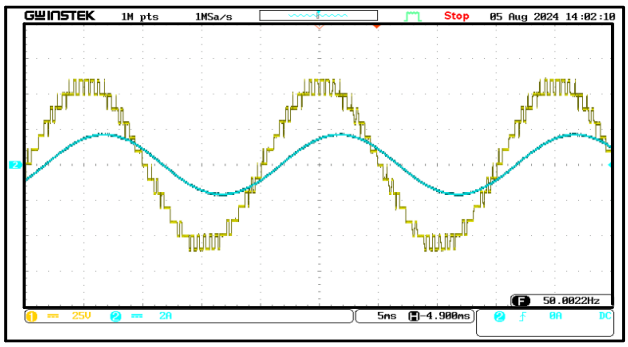
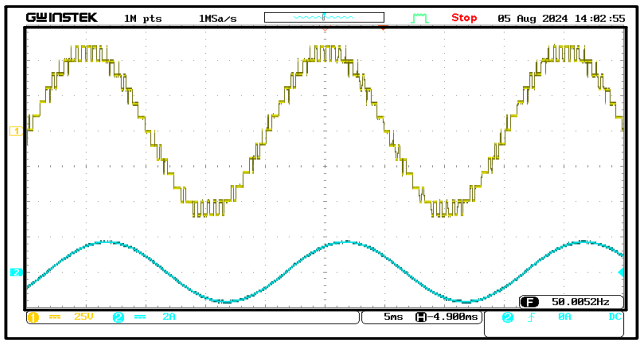


(c)



(d)

Fig. 13 Output voltage, current waveforms at 0.885 lagging power factor

5. Comparative Analysis

An elaborative comparative study is being done in the context of the number of IGBTs, voltage levels, capacitors, total components, diodes, DC sources and voltage gain. The aforementioned studies result in decreased complexity and cost of the proposed topology. The ratings of switches are low as compared to conventional structures. An excessive number of switches impacts the complexity and economy; therefore, the disadvantage is overcome in the present work.

Table 3. Comparison of ESCSS with recent topologies

Topologies	N_{sw}	N_{lv}	N_{cap}	N_c	N_D	$N_{sources}$	V_g
[3]	24	13	8	60	36	12	1
[4]	24	13	5	60	24	12	1.1
[5]	11	13	3	14	0	1	0.9
[11]	12	13	2	22	0	1	2
[13]	42	13	3	45	0	9	1.3
[14]	11	13	0	13	0	2	1.1
[22]	10	13	4	14	4	2	1
[23]	8	11	1	11	0	1	1
[24]	9	9	3	15	3	1	1
[25]	12	9	3	15	0	1	1
Proposed	8	13	0	11	0	3	2.1

Table 3 demonstrates the benefits of the proposed inverter over traditional topology, which includes reduced switch count, output voltage level boosting technique, low ratings of switches, less switching losses, medium voltage gain and many more. In the table illustrated, N_{sw} indicates the number of switches, N_{lv} shows the number of levels, N_{cap} indicates the number of capacitors, N_c denotes the number of components, N_D reflects the number of diodes, $N_{sources}$ indicates the number of sources, and V_g shows voltage gain.

Table 4. Approximate cost comparison

Topologies	Cost of components (Rs)
[3]	1,89,450
[4]	1,89,150
[5]	33,850
[11]	34,050
[13]	1,64,105
[14]	33,540
[22]	34,090
[23]	33,190
[24]	33,910
[25]	34,140
Proposed	28,550

Table 4 depicts the approximate cost involved in implementing conventional and proposed configurations. It infers the cost-effectiveness of the proposed topology and declares it as an economical and penurious. Furthermore, the proposed topology derives the concept of low THD%, economical, sustainable and reliable.

6. Conclusion

An advanced thirteen-level ESCSS topology is implemented to lower the number of gate drivers and active switches. This resulted in lower total expenditures and the number of devices. The switching pattern is effectuated based on the Modified, Reduced Carrier Pulse Width Modulation (MRCPWM) technique, which results in low losses at the fundamental frequency. The modeling and experimental outcomes demonstrated the efficacy of the design by affirming its operational principles along with its ability to withstand distinct load instances. A comparative study is conducted with various conventional 13-level MLI structures, considering the number of factors. In conclusion, the simulation and hardware setup substantiated the explained design's viability, practicality, and consistency.

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