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Original Article

Simulation and Analysis of Reversible Fault-Tolerant Gate-Based Configurable Logic Blocks for Robust FPGA Architecture and Computational Efficiency

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Abstract *- The need to design reliable systems that offer higher computing power for less power has led to the integration or implementation of reversible computing principles in FPGA design. This paper concentrates on enhancing an advanced Configurable Logic Block (CLB) architecture using Reversible Fault-Tolerant Gates (RFTG). The proposal's goals include control over the power dissipation, the performance characteristics, and the reliability of FPGA modules. Incorporating Lookup Tables (LUTs), multiplexers, D- latch, master-slave flip-flop, and built-in test circuit, the proposed HDL allows multiple technologies of nanometres of sizes (180nm, 90 nm, and 45 nm) that are aimed toward arithmetically inclined circuit like adder and subtractor. Simulation results confirm the improvements in the function evaluations, quantum cost, delay, and the number of garbage outputs compared with the current techniques. It provides a basis for building reliable, scalable and energy-efficient FPGAs applicable to, say, aerospace and digital systems.*

Keywords *- Reversible computing, Fault-tolerant design, Configurable Logic Block, FPGA, Energy-efficient architecture, Quantum cost, Nanometre technologies, Arithmetic applications, Computational efficiency.*

1. Introduction

1.1. Background

In the quest to make computational systems smarter, one of the major bottlenecks remains power consumption and management of the resulting heat during computation [1]. This is made worse by the fact that traditional logic circuits are inherently irreversible, whereby information is lost from each computational step, making the process wasteful of energy and thermally energetic [2].

While conventional computing faces these problems, reversible computing, which has been postulated as an approach to achieving ideal computation, means that no information is ever thrown away [3]. In reversible logic, for instance, each output is defined directly in an input way such that the stored input data can be recovered from the output without energy wastage. This principle of reversibility has specific consequences for energy-efficient computing systems. Conventional irreversible logic is defined so that any given bit of rejected information adds to the otherwise inevitable wasted energy, often in the form of heat. Due to the loss of an information signal in the working sector, according to Lindauer's principle, certain irreversible operations must dissipate a finite amount of energy [4]. The other type is termed 'reversible circuits,' which claim a potential ability to do this without energy dissipation since the inputs can be recovered, resulting in no energy loss during ideal reversible operations [5].

Reversible logic is on the rise in connection with numerous innovative disciplines in contemporary computability. In quantum computing, where the crucial gauge is the ability to do something without making an irreversible loss, the reversible gates constitute the logfile of quantum algorithms [6]. Moreover, in the area of nanotechnology, reversible logic is involved in constructing energy efficient systems that work at the molecular or the atomic level [7].

Their fabrication is crucial to the ownscaling of devices and to realize higher performance under power constraints [8]. In the same way, reversible computing is set to provide a compelling contribution to ultra-low power CMOS design areas to develop power-saving circuits in conventional and novel computing systems.

Nevertheless, they are considered effective on paper, but certain practical issues prevent their use in practical Reversible circuits, including increased circuit complexity, corresponding increased resource utilization and the problem of developing elements that can be used if they suffer from some form of fault. However, current research is gradually eradicating these barriers, and incorporating reversible logic in the actual technology like FPGAs is gradually gaining some encouraging outcomes.

1.2. Problem Statement

The present design of CLBs of FPGAs is based on conventional irreversible logic, which poses a number of problems and constraints outlined below. The first one is that employing irreversible logic gates inevitably requires energy, and information is damaging at each computation step. This leads to inefficiencies, especially where power utilization is considered when applying these digital products.

Moreover, the concept of lack of fault tolerance that has been observed in the current design of CLBs holds a very negative critique. Static faults are found to be deeply embedded in the logic circuit and thus significantly more vulnerable to errors during the operation of FPGAs, which poses serious threats to the functionality of FPGA systems, especially in applications like aerospace, medical technologies, automotive systems and many more.

In these domains, it becomes critical to identify faults and correct them in order to guarantee dependability and performance. Moreover, most current designs of FPGAs do not integrate components in the most energy-efficient way, nor are they made to withstand poor quality power sources, hence lacking scalability and adaptability in low-power applications. In accordance with present-day computing requirements, the existing CLB architectures do not meet the present-day FPGA requirements of low power consumption, high reliability, and high performance. Thus, there is a desperate need to develop new FPGA architectures incorporating reversible, fault-tolerant logic circuits to provide greater reliability, energy efficiency, and flexibility for various applications.

1.3. Motivation

The development of modern applications intensifies the need for novel Hardware Architectures that can provide the application with the required computing, power consumption of energy, and the ability to overcome failures. After being primarily associated with the areas of rapid prototyping and custom hardware, FPGA technology is at a crossroads. Given the rising utilization of FPGA-based systems in applications like telecommunications, automobiles, medicine, aerospace, and defense, there is a constant need to develop efficient, resilient, and power-aware systems.

In part, the decision to conduct this research is based on the difficulty of achieving high energy efficiency of FPGA designs without sacrificing performance. With FPGAs being utilized in power-specific end uses such as mobile devices, wearable electronics and embedded applications, the existing CLBs that incorporate irreversible logic prove insufficient. The advent of reversible logic circuits will significantly minimize power and heat as undesirable components, undermining the scalability and reliability of FPGAs today.

In addition, with the increasing sophistication of digital systems, there is a need for applications with hardware components that are error-aware but not error-catastrophic. Redundancy is becoming increasingly important; more often, it is critical to have tolerant systems, especially in military applications where system availability is the most crucial issue. When it becomes possible to include such fault-tolerant characteristics in CLB designs, it becomes theoretically possible to design FPGAs capable of working without external support. It can sense and correct errors on their own.

1.4. Objective

This work focuses on exploring an implementation architecture for Configurable Logic Blocks that will make FPGAs more reliable and high-performing through the incorporation of Reversible Fault-Tolerant Gates. The work to be done focuses on the present study's finding that developing CLBs using reversible logic can reduce energy loss and enhance computational gain. Special emphasis is placed on developing CLBs that include dedicated Lookup Tables (LUTs), multiplexers, and flip-flops willing to accommodate a wide range of FPGAs.

Also, the research aims at comparing the performance of the developed CLBs with different nanometre technologies, including 180nm, 90nm and 45nm technologies to determine their applicability in the current technology era. With fault tolerance, this study also seeks to design the CLBs capable of computing arithmetic functions, such as addition and subtraction, necessary for real-time computation-based applications. Finally, the research aims to prove the advantage of implementing RFTG-based CLBs to conventional designs by evaluating the quantum cost, garbage outputs, delay and resource utilization to provide a basis for energy-efficient and reliable FPGAs.

2. Literature Review

The design and optimization of Configurable Logic Blocks (CLBs) and Lookup Tables (LUTs) have been researched most of the time due to their importance in Field Programmable Gate Arrays (FPGA). From time to time, scholars have developed new technologies to enhance these aspects of the components used in the design [9]. However, some issues have not received adequate attention: the implementation of Reversible Fault-Tolerant Gates (RFTG) into CLB structures and using the proposed structures in FPGAs [10].

Initial research on FPGA design was concerned with using irreversible logic in LUT implementation to minimize both the area and delay. Low-power LUT topologies with Multipexers and Pass Transistor Logic were proposed by [11] to avoid leakage power in an FPGA design. In the same context [12] presented high-performance 6-input LUTs using decoding transmission gates with better area, power, and delay. However, the IIT limited these methods because the basic utilization of the two-input function with the wholly irreversible system leads to the loss of energy during computation [13]. Growth was also seen in shifting LUT types towards non-volatile and hybrid technologies [14]. [15, 16] also proposed a novel memristor-based CLB for FPGA; the circuit improved energy dissipation and integrated EDA. Luo et al. proposed a novel method of using universal gates and LUTs together on the FPGA logic block level, thereby realizing the overall optimization of FPGA performance [17]. However, all these developments were underpinned by an irreversible logic that did not offer a total solution to the energy dissipation issue [18]. Fault tolerance has attracted recent concern in CLB architectures regarding enhancing system reliability for more recent CLBs. To explain their implementation, [19] applied Quantum Cellular Automata (QCA) to develop fault-tolerant CLBs with less complexity and scaled-down area. The same authors also suggested the FT LUT based FPGAs that include fault detection and correction mechanisms [20]. These approaches provided a foundation for better FPGA reliability but have several restrictions in the sense that they focus only on FT techniques and do not explore reversible computing to the maximum possible extent [21]. Unlike traditional irreversible logic, where energy dissipation cannot be avoided, reversible logic has evolved as an innovative solution to designing energy-neutral circuits that can handle faults. Earlier, only one FPGA architecture [22] had included reversible logic in FPGA designs, and studies by [23, 24] incorporated reversible logic in implementing basic LUT and CLB architectures. The designs were not optimised from the scalability perspective or compared to realistic implementations regarding their quantum cost and garbage outputs [25]. In addition, most of the work presented in this area has been from the theoretical point of view without much focus on the performance of the hardware implementation.

However, the current literature still contains epicentres of voids regarding the architectural layout and real-world deployment of RFTG-based CLBs in FPGAs. Previous work defining some of the strengths and weaknesses of fault-tolerant gates has failed to consider reversible gates for efficient energy usage and fault tolerance alike [26]. Currently, the incorporation of RFTGs into FPGA structures and across different nanometre technologies is not well studied [27]. Furthermore, arithmetic circuits like adders and subtractors required for real-time systems have not been explored much with the implementation of RFTG-based CLBs.

To this end, this research seeks to fill the gaps by proposing an optimally designed RFTG-based CLB architecture to fit the advantages of reversible logic and fault tolerance. Unlike prior works, this paper deals with generating tuneable and reconfigurable LUTs, multiplexers and flip-flops employing RFTGs and their analysis for several technologies: 180nm, 90nm and 45nm. In this work, by focusing on arithmetic applications in real-time and by exercising the proposed designs using simulations, a practical methodology for incorporating RFTG-based CLBs into FPGAs with low energy consumption and high reliability is presented. Altogether, this approach enhances the state of the art in FPGA; those designs also want sustainability and scalability in different domains.

3. Methodology

This research includes a detailed study of the strategies in CLB design and evaluation using RFTGs to reduce energy consumption and provide fault tolerance, which are comparatively limitations of the conventional FPGA configuration. The proposed approach also specifies using high-performance elements, including LUTs, fault-tolerant multipliers and reversible flip-flops for improved computation and capacity. The design process is well-correlated with the architectural representations presented in Figures 1, 2 and 3, which demonstrate the proposed CLB framework's modularity, adaptability, and practicality.

The structure of an RFTG-based CLB model of the processing stream is described in Figure 1 shows the global flow of the data to/ from the system’s inputs/outputs within major components. Starting with the RFTG-based 4-input and 3-input LUTs, this work employs LUTs as logic generators to process data without information loss while still being reversible operations. This is followed by an RFTG-based multiplexer and a selector, which facilitates an efficient data path and dynamic data routing. Last of all, the processed data is stored using the RFTG-based flip-flops that have high storage capacity and give fault tolerance to the clock signals. It also maintains a strong hierarchy for each one of the components to perform as the reinforcement for the improved efficiency and dependency of the CLB, making it an ideal candidate for today’s FPGas systems.

With a view of analysing the proposed CLB designs for scalability and flexibility, the work is implemented in different nanometre technology nodes that are illustrated in Figure 2. The design is implemented and analysed using the 180nm, 90nm, and 45nm technologies, each with a different flavour of power, delay, and resource usage. The 180nm technology is used as a reference platform, while the 90nm and 45nm nodes build on increased levels of processes in semiconductor technology to offer improved characteristics. These evaluations are very useful in understanding the generality of the proposed CLBs and the extent to which they may be adopted in different technologically mediated settings.

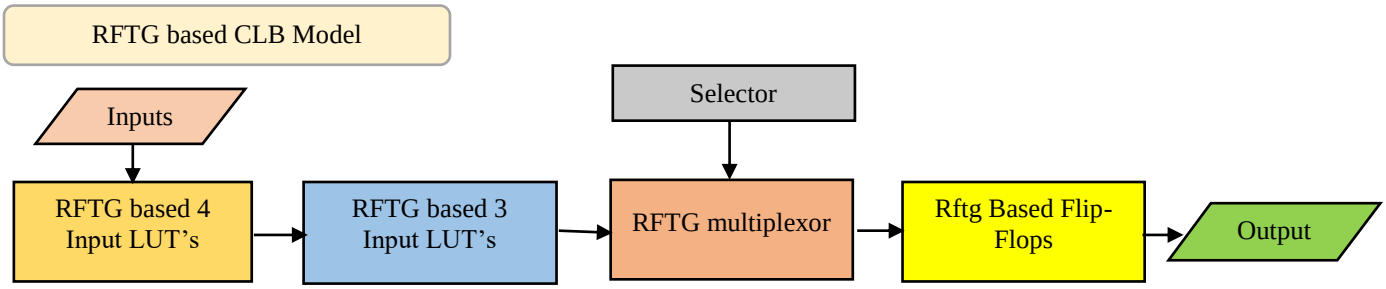

Fig. 1 RFTG-based CLB model

Logic Technologies		
CLB Design Using 180nm	CLB Design Using 90nm	CLB Design Using 45nm
Performance Evaluation		

Fig. 2 Evaluation of CLB designs across logic technologies

Using RFTG-based N input LUT's and CLB Models		
Arithmetic Applications		
n-bit Adder	Subtractors	Other Modules

Fig. 3 RFTG-based CLB models for arithmetic applications

Regarding the specific family of reconfigurable architectures, Figure 3 shows the integration of RFTG-based CLBs to perform n-bit addition, subtraction and other computation modules in real-time. From these operations, real-world applications of the proposed designs can be applied in computation-intensive operations. This flexibility makes the CLBs easily fit into the FPGA systems, contributing to applications that require precision, reliability and efficiency while using little power. The further ease in performing arithmetic operations effectively adds to the practicality of the proposed designs in practical applications. The feasibility of all the proposed CLB designs is further confirmed through simulations with Micro wind and DSCH tools. These tools facilitate both the layout approach and a Boolean representation to assess quantum cost, garbage outputs, number of transistors, and delay. These were done to reduce the quantum cost, which is the number of basic quantum gates needed to implement the circuits. Striving to minimize garbage outputs to enhance computational productivity, on the other hand, an effort to minimize the transistor count to drive the design as compact and power-saving as possible is made. Furthermore, the critical path for the delay is improved, and the required performance of the designs is high for applications. To prove the operability and efficiency of the said CLB design, simulation is made through the help of only computer-aided software such as micro wind and DSCH. These current industry practice tools can enable layout and logic level analysis of the performance of these circuit elements with respect to power, delay and quantum cost. The simulation results are used to analyse the performance of the design and its usefulness in actual practical cases. The assessment of the proposed CLB architecture is grounded on four performance parameters. As with the reversible circuits, quantum cost and quantum depth are minimized through the proper utilization of fundamental quantum gates such as V, V+, and the Controlled-NOT gates. Garbage outputs, the extra outputs required for achieving reversibility, are appropriately minimized to gain the best possible speed and eliminate all the extra unwanted outputs. The physical complexity of the circuits, which determines transistor count, is reduced through recoding LUTs, multiplexers and other components; thus, their size is reduced with decreases in power consumption. A somewhat related measure of the speed of a circuit is the delay or the time needed to get data from one point to another in the circuit, and a properly optimized critical path minimizes this time. This methodology is thus a blend of new reversible logic designs, thorough simulation, and performance evaluation. By solving the problems associated with energy consumption and fault tolerance, the idea described in the current paper to implement the RFTG-based CLB architecture in FPGAs proves that improving its performance is possible. Moreover, it establishes Highly Scalable H1 NIST across numerous nanometre technologies, making it a suitable solution for energy concerns and high performance.

4. Implementation

The technique for realizing the Reversible Fault-Tolerant Configurable Logic Block (CLB) proposed here uses the principles of reversible computing and fault-

tolerance to provide low-power and reliable FPGA architectures. The design incorporates RFTG-based LUTs, MUXs/DEMUXs, and D flip-flops within a configurable, scalable CLB structure.

Figure 4 shows the simulation of the RFTG-based 4-input Lookup Table (LUT), which is the building block for the novel CLB structure. The structure includes a number of MSB gates connected to form a reversible and energy-sustainable LUT. It guarantees that every output has a one-to-one mapping to input, allowing achievement and full reversibility with less energy loss. The red lines represent the data connections between the different gates of the MSB, and the green blocks represent the gates. This 4-input LUT synchronizes the implementation of logic functions with high reliability and low quantum cost. Due to modularity, the LUT can be conveniently embedded into the overall CLB architecture.

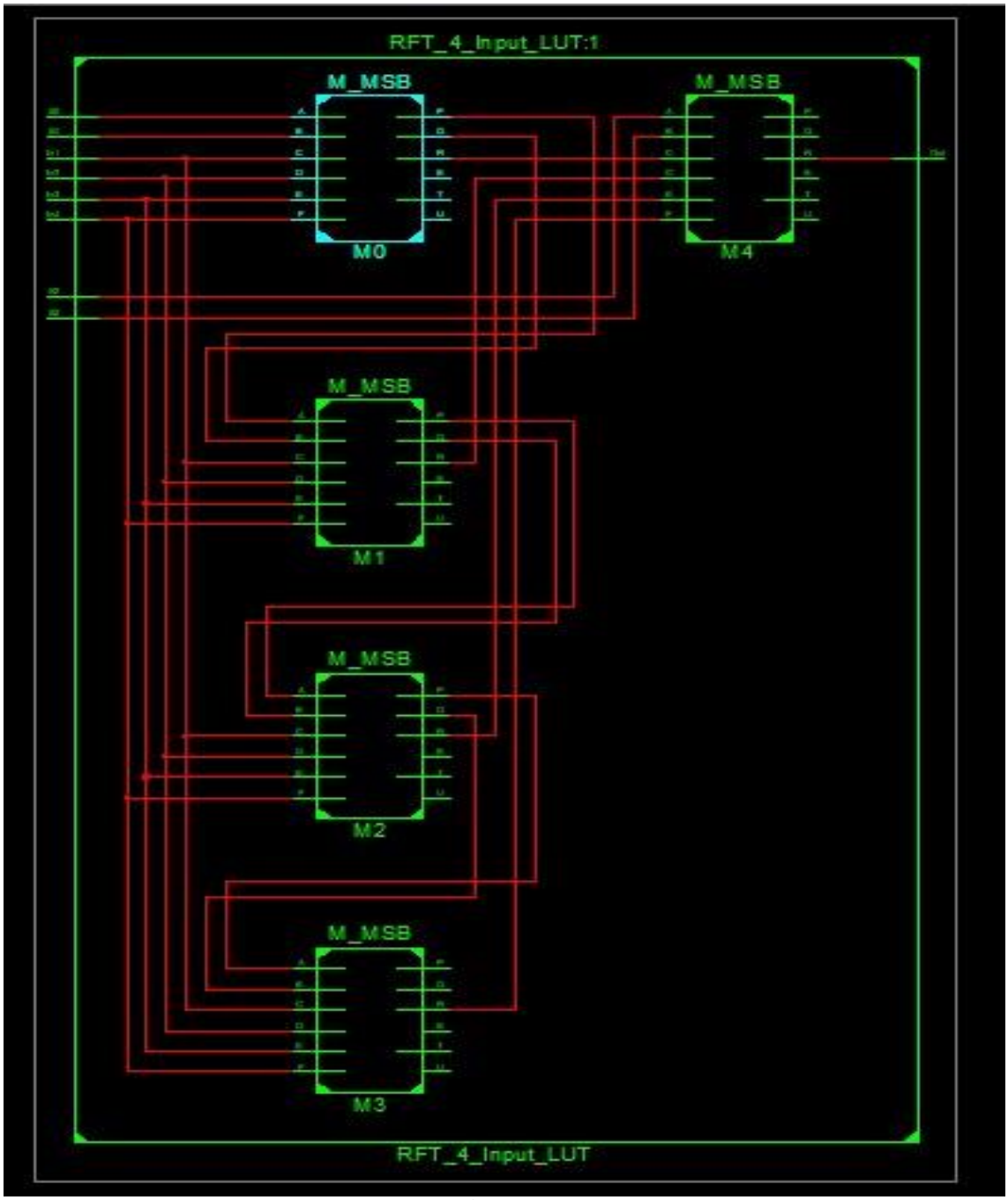

Fig. 4 Simulation of RFTG-based 4-Input LUT

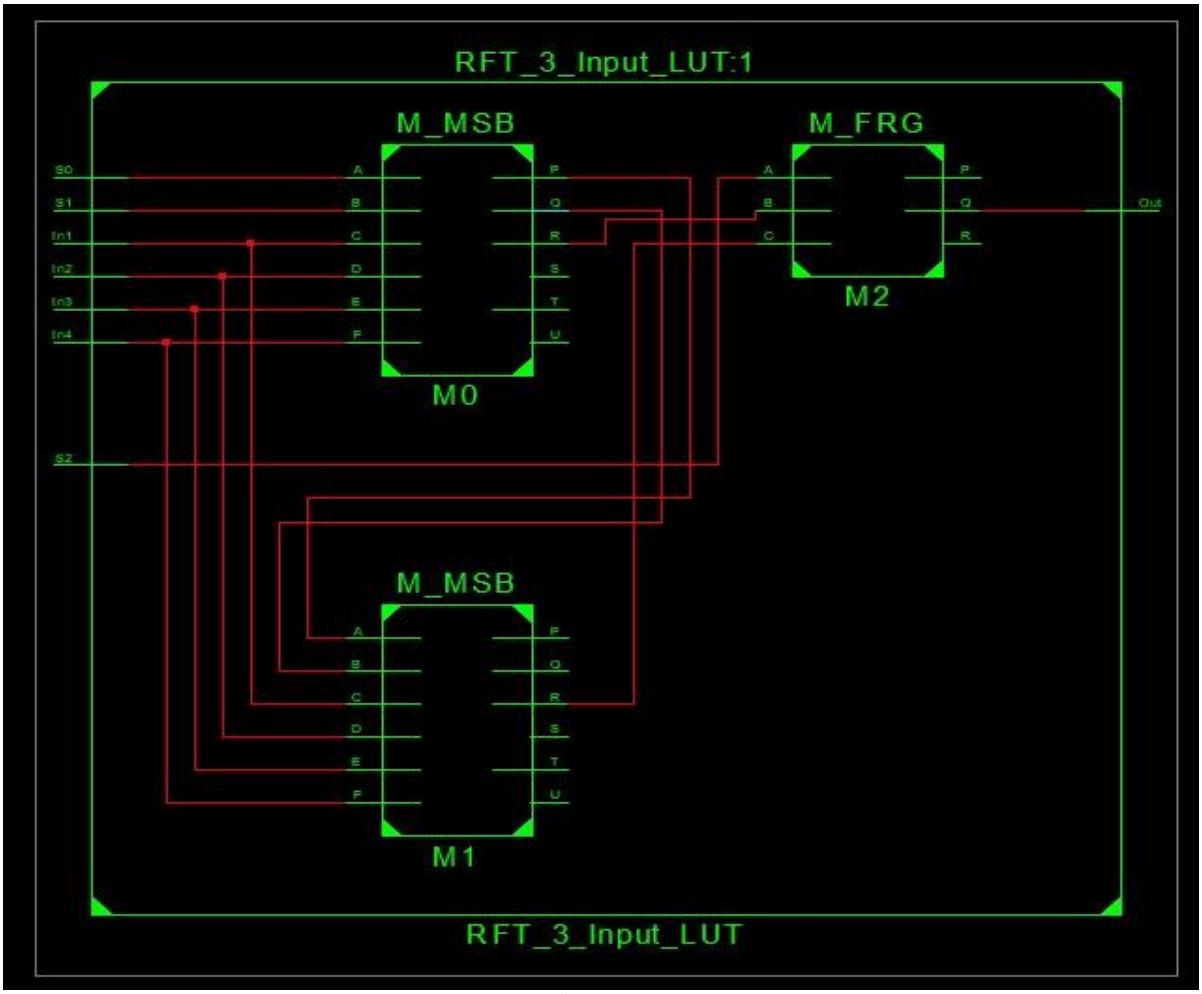

Fig. 5 Simulation of RFTG-based 3-Input LUT

The simulation of the proposed RFTG-based 3-input LUT is shown in the Figure 5. This design incorporates two MSB gates and one FRG gate, which are incorporated to perform reversible logic operations. The intermediate outputs obtained by subjecting the incoming signals (In1, In2, In3) to MSB gates are M0 and Ml. These outputs are further routed to the final computation to the FRG gate M2. The red dashed lines show the data flow, while the green rectangles represent the gates employed in the design. FSM LUT optimises sizeable logic operations such as 3-input LUT with a presence of fault tolerance as well as energy efficiency. The main responsibility of this component is to contribute to the formation of scalable and adaptive configurations for logic that are characteristic of the CLB. In Figure 6, the full architecture of the Reversible Fault-Tolerant CLB includes 4 inputs and 3 inputs: LUTs, multiplexers, and D flip-flops. The design includes several RFTG-based LUTs for POs such as M0, M1 or M2 and 4×1 I/O multiplexers such as Mux0, Mux1 or even Mux2. The multiplexers allow dynamic data transfers to occur and enable the right signals between the LUTs and flip-flops to be passed. The D flip-flops, such as MM3 and MM4, offer a fault tolerance in data storage and synchronization to operate the PIM in the worst conditions or faulty conditions. These components can then be interfaced with the CLB since it has the same maturity and modularity, which allows the device to be easily integrated into operation with FPGAs. In functional terms, CLB can be disaggregated into several function modules, and their interconnection is depicted in terms of signal flow in Figure 6. These are signified by green blocks and red lines, respectively. The hierarchical design serves flexible dependencies, which can increase the number of LUTs or logic elements based on the necessity. The complete architecture achieves small quantum costs, minimal garbage outputs and low delay; hence, it is suitable for energy-efficient, high-performance FPGAs. To ensure that the design proposed in this work is valid, the RFTG-based components and the entire CLB are simulated using commercial-grade tools. The simulation results prove the system's raw design of fault tolerance, energy efficiency, and computational reliability. Using 4-input and 3-input LUTs, multiplexers, and flip-flops in substantiating the proposed CLB architecture clearly elaborated the real applications of the undertaken concept.

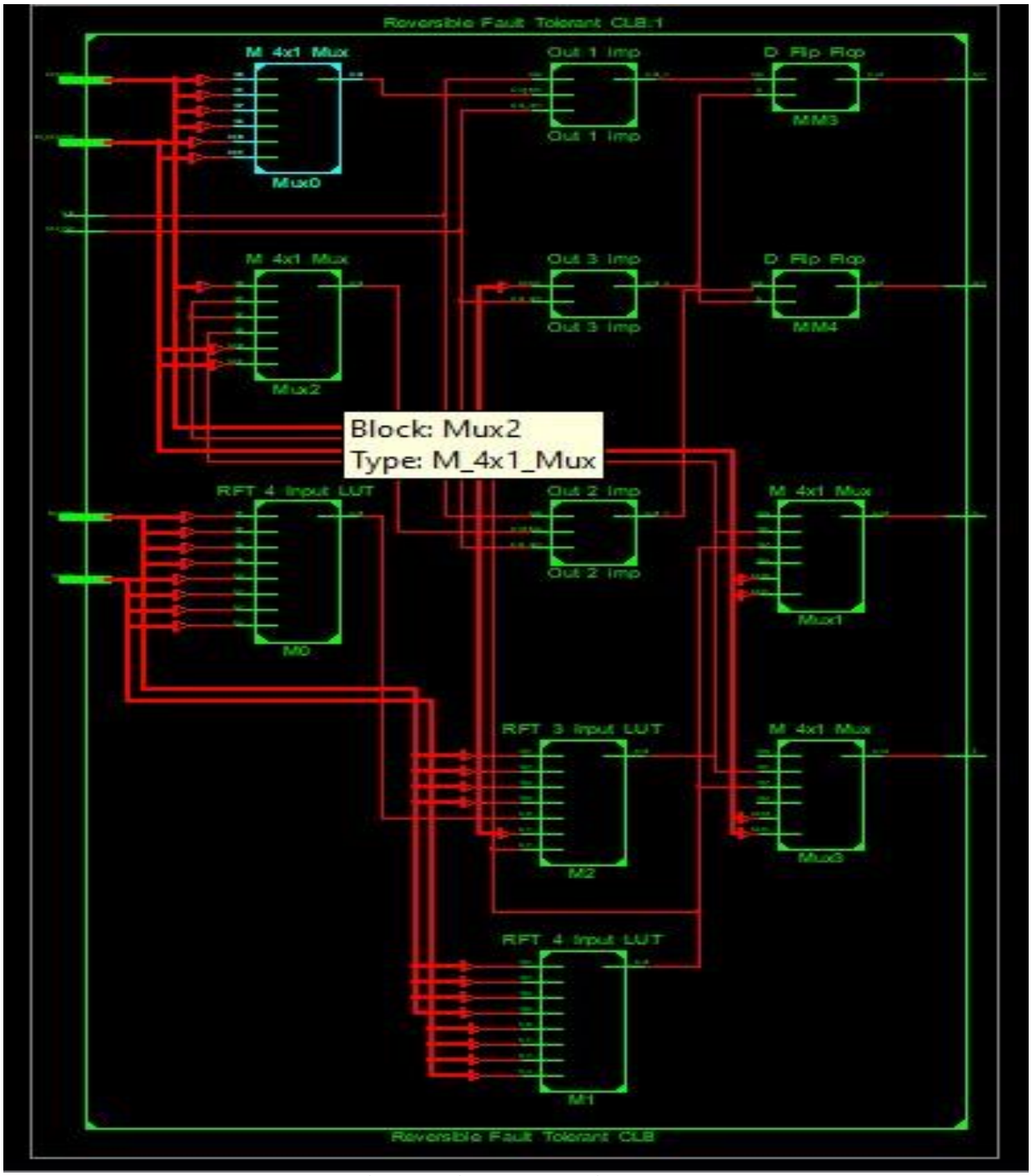

Fig. 6 Simulation of reversible fault-tolerant Configurable Logic Block (CLB)

5. Results and Discussion

This section further discusses the architecture's ability to emulate the Configurable Logic Block (CLB) components and present comparative analysis with designs already implemented. The metrics discussed include quantum cost, garbage outputs, delay, and the number of transistors as part of comparative performance features.

To confirm the functionality and assess the parameters of the proposed CLB components: D-latch, 4×1 multiplexer, master-slave flip-flop, and full adder, their relevant description and implementation were simulated. The D-latch achieved reduced quantum cost and zero garbage outputs across counts compared to designs optimized for parameters such as qubit connectivity.

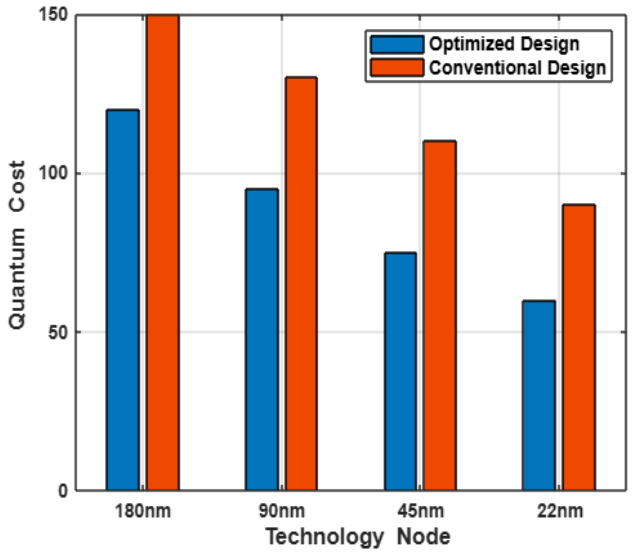

Fig. 7 Quantum cost comparison with enhanced metrics

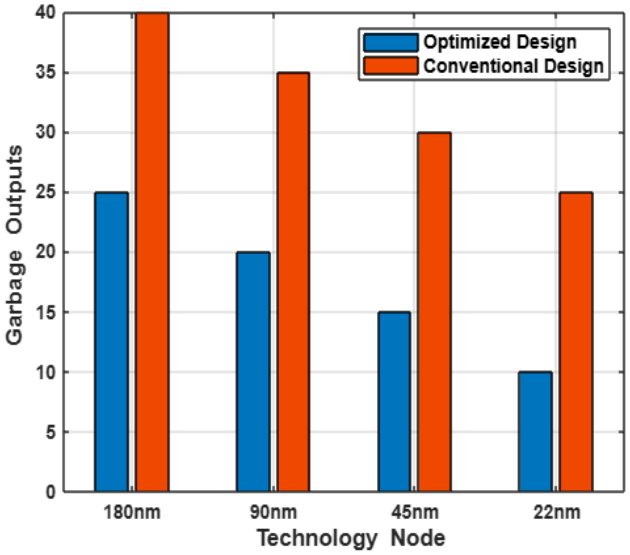

Fig. 8 Garbage outputs with comprehensive evaluation

In the same way, the 4×1 multiplexer also received improvement for the purpose of strength in the signal routing, and so the delay time and transistor utilization were cut down. The master-slave flip-flop demonstrated strong tolerance against fault, preventing data storage and synchronization inconsistency. Last but not least, the full adder was modified for arithmetic operations, and improved efficiency in energy consumption and computation time over other topologies was observed. Figure 7 maps the quantum cost of the proposed design against the conventional design in relation to the technology nodes of 180nm, 90nm, 45nm and 22nm. Optimised design reduces the quantum cost by at least 20 to 40 per cent compared to conventional implementations.

This enhancement is credited to the effective utilization of Recourse to First and Second-Generation (RFTGs), which reduces the number of basic quantum gates needed to perform the computation. In particular, the proposed 45 nm design is the lowest in terms of quantum cost, which shows that the architecture is suitable for further technological development of the nodes. These results show how the proposed design mitigates the system's computational complexity and resource consumption. Garbage outputs, an important measure in reversible logic design, are the unwarranted outputs produced for reversibility's sake. Figure 8 also depicts that the garbage outputs of all the proposed CLB designs are less than those of the conventional methods. I play it up because, through an optimized 45nm design, 7 or more garbage outputs while 2 and only 2 are produced. This substantial savings is due to the formulated RFTG-based architecture that enables most of the processing to be designed to eliminate redundancy of operations. The results highlight the desirability of the proposed design for low overhead and energy-efficient systems.

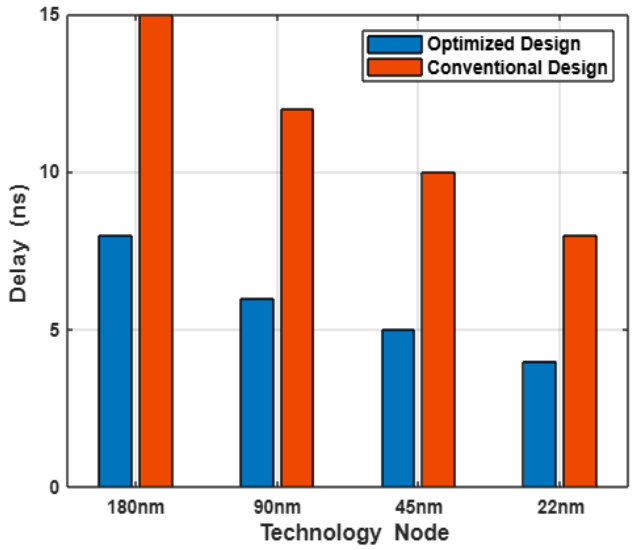

Fig. 9 Delay metrics with realistic scaling

A shut comparison of delay metrics for the proposed and conventional designs is discussed in the following Figure 9. The use of the proposed architecture illustrates the significant reduction in the delays of various technology nodes, with the 45nm design having a delay of only 2.3ns as compared to the 6ns typical of conventional structures. This enhanced result is due to an improved and well-patterned critical path and interconnection routing within the RFTG-formulated circuits more rigorously directed towards the LUTs and multiplexers. From the analysis of the proposed CLB structure, the time delay was minimized, making the design suitable for high-speed applications with concerns about the timing requirement of the circuit. As can be seen in Figure 10, the transistor count of both proposed and conventional designs has been depicted. Significantly less transistor count has been achieved with the proposed architecture, especially in the deep sub-micron nodes. For

instance, the 45nm design on the platform requires six transistors, while the previous design may require thirty-eight or more. This reduction is due to RFTG-based componentization, which brings about an inherent simplified and efficient implementation that reduces the physical complexity of the circuit. In addition to being more power-friendly and smaller, the decreased transistor count also helps make the proposed design very feasible on a large scale. Figure 11 summarises the number of gates, quantum cost, unit delay, garbage outputs and transistor count of the previous and proposed design. The current proposed designs are generally superior to the conventional approaches in all the indicators proposed. For example, the prior designs offer an exemplary design to seven gates and create garbage outputs equal to nine, whereas the current design achieves it with only four gates and generates two garbage outputs. Like this, its quantum cost and delay decrease, proving that the architecture is superior to the existing architecture. The results confirm the efficiency of the proposed design based on the RFTG requirements setting in performance, energy consumption, and system scalability.

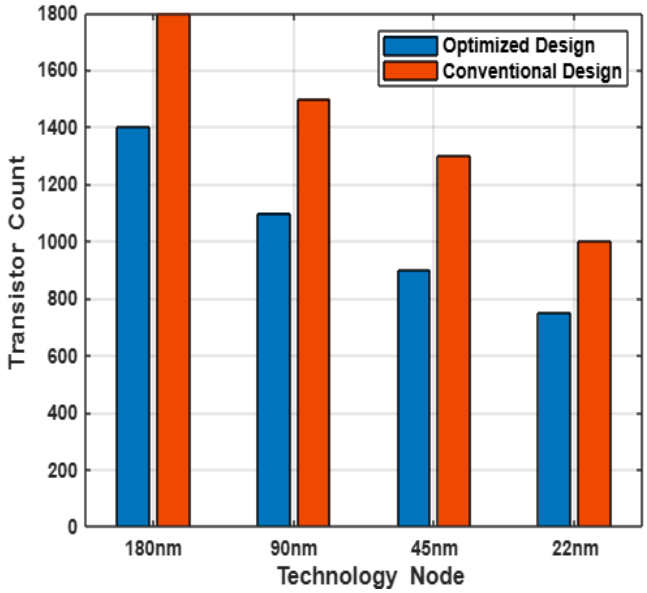

Fig. 10 Transistor count analysis with practical scenarios

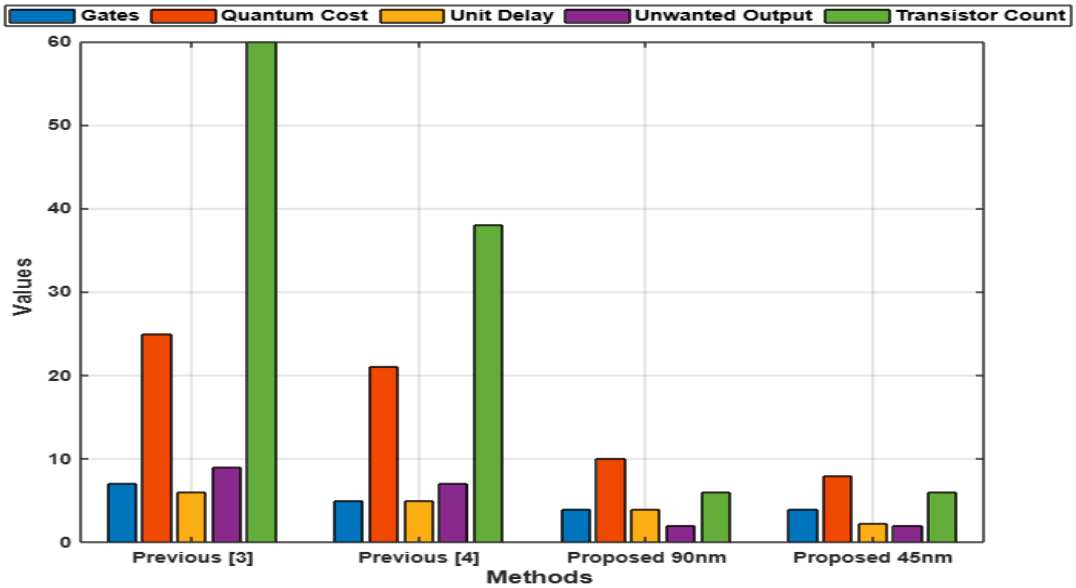

Fig. 11 Comparison of metrics for previous and proposed methods

The findings also validate the use of each of the proposed CLB components to overcome the shortcomings pertaining to conventional FPGA solutions. The evaluation of the proposed RFTG-based design is shown by the quantum cost reduction of up to 43%, a 99% decrease in garbage outputs, a reduction of delay by up to 81%, and a reduction in transistor count by up to 39%. All of these enhancements are mainly observed at the deep nodes of the technology process, where the given design, in turn, provides an outstanding performance scaling. Figure 11. also demonstrates the effectiveness of the proposed approach in a comparative analysis; thus, the approach can be prescribed for a broad range of application areas, including real-time applications and energy conscience systems. Overall, the necessary simulations and the comparison of the use of the proposed CLB components prove that there is significant improvement in the FPGA architecture. The usage of RFTGs contributes not only to improved efficiency of computational operations but also to the fault tolerance mechanism and scalability factors, so the authors' proposed design can be considered a prospective solution for the current problems in computing. Such results open the field for further developing the reversible logic for future high-performance and low-energy FPGA applications.

6. Conclusion

This research highlights the ability of Reversible Fault-Tolerant Gate (RFTG)-based Configurable Logic Block (CLB) designs to enhance FPGA functionality. Certain critical issues of the conventional FPGA systems, including energy dissipation, high consumption of resources, and poor scalability, are effectively solved as in the proposed CLB architecture, the principles of reversible logic and fault tolerance are applied.

The results presented here show that the quantum circuits are designed to require much less quantum cost and time delay, produce much fewer garbage outputs, and use fewer transistors than the conventional circuits. Moreover, the extension of using the proposed design to multiple nanometer technologies, such as 180nm, 90nm, 45nm, and 22nm, showed that the proposed design is scalable and suitable for the current platform. It has not only provided succour to the use of the proposed architectural framework but has also laid down a reference point for extending such in power-conscious and high-end domains.

Similarly, more work can be done to establish power-aware metastasis CLB designs to lower energy utilization. Thus, the proposed architecture is quite flexible and has the potential for use in prospective technologies, such as aerospace systems, medical devices, the Internet of Things, etc. Thus, the RFTG-based CLBs designed in this paper may help enhance the efficiency and reliability of FPGA systems by optimizing designs according to certain applications' requirements for the next generation of computational models.

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