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Original Article

Machine Learning-Based Design of a 2-Stack Gilbert Cell-Based Variable Gain Amplifier for Low-Noise Application

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Abstract *- In this paper, a Machine Learning (ML) based design methodology is presented for the cell-based Variable Gain Amplifier (VGA). The designed unit cell consists of the Gilbert Cell configuration, with two cells stacked over each other for the current reuse and multiple channels for recording. The design can be reused for multiple recording channels to successfully record a large number of low-frequency signals. Furthermore, the Gilbert Cell design includes the integration of g_m/I_d Transconductance Efficiency Factor (TEF) with the k-nearest neighbor (k-NN) based searching algorithm for obtaining the geometry of the cell. The k-NN algorithm analyzes a precomputed look-up table generated by the TEF methodology for the design. The k-NN algorithm, implemented to optimize the VGA's transistor width-to-length (W/L) ratios, demonstrates exceptional precision. With an accuracy of 0.96 in selecting optimal geometric configurations, the k-NN approach significantly enhances the VGA's performance under varied operational conditions, reflecting its robustness and efficacy in real-time design adaptation. The unit cell so configured using the integrated approach is stacked over one another to give two channels for signal acquisition. The VGA gives a gain ranging from -20 dB to 54 dB with 10mW of power consumption.*

Keywords *- Variable gain amplifier, Machine Learning, Gilbert Cell, Transconductance Efficiency Factor, K-nearest neighbor, Look-up Table, etc.,*

1. Introduction

In the evolving landscape of signal acquisition, the demand for highly adaptable and efficient electronic devices is ever-increasing [1, 2]. Among the pivotal components of signal acquisition systems are Variable Gain Amplifiers (VGA), which are integral in applications ranging from audio processing to sophisticated radar systems to bio-medical signal acquisition. In conditions where signal amplitudes vary and the amplifier must dynamically change the gain to ensure optimal performance of the system, VGAs are absolutely essential [3]. The conventional method uses either basic adaptive algorithms that change the gain depending on pre-defined criteria or manual tuning. These techniques are not without restrictions, though; usually, they call for sophisticated circuitry or fail to react fast to any rapid change in signal conditions. Furthermore, incorporating these VGAs into contemporary digital systems usually requires extra components, which might complicate the design and raise power consumption [4].

Traditionally, the VGAs are designed with a closed-loop configuration to provide a varied gain over a large range. However, these systems are limited by the bandwidth specifications, and further, a large number of ramp signals are required to provide continuous gain tuning. Again, the use of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) in the design of the VGA requires exponential approximation to get an accurate dB-linear characteristic. Many designs have been proposed to achieve linearity.

In [3], the VGA uses the folded cascode structure to achieve linearity but does not have good bandwidth and power consumption. Similarly, in [5], though the circuit provides an exponentially large gain, noise creeps into it, which affects the design process of the VGA. The VGA discussed in [6] works using the cell-based structure, and stacking the unit cell can lead to a design with multiple channels for signal acquisition. This work uses the Gilbert cell-based design for the VGA cell to provide a varied gain for multiple signal acquisitions [7-9]. The basic block diagram of the Gilbert cell is illustrated in Figure 1. Further, this work focuses on the design methodology of the VGA cell. Equation 1 shows the output produced by the VGA.

$$V_{out} = A_1 V_{in} + A_2 V_{in} \quad (1)$$

Where A_1 and A_2 are gains of the differential amplifiers and controlled by $V_{Control1}$ and $V_{Control2,}$ respectively.

The Gilbert-Cell, well-known for its balanced architecture and intrinsic linearity, forms the cornerstone of the cell-based VGA design. [10] uses the Gilbert-cell configuration as a mixer with the source degeneration technique. [11] uses the Gilbert structure as a VGA with a double heterojunction bipolar transistor. The VGA design boasts a gain control range of 44 dB, a noise figure of 6.2 dB, an output third-order intercept point of 17 dBm, and a total power consumption of 350 mW from a single power supply. In [12], the VGA's development is described, featuring a 4-stage fully differential cascaded amplifier architecture in a 180 nm CMOS process, achieving a current-controlled gain from -39.4 dB to +20.2. Despite its advantages, traditional Gilbert Cell configurations struggle with scalability and power efficiency under varying operational conditions. Further, all the literature so discussed above utilizes either a conventional methodology for the design of the VGA cell or a hit-and-trial method for the design. Again, with the reduction in the technology node, an overdependence on human expertise may lead to failure in the Integrated Circuit (IC) design [13]. This work focuses on using Machine Learning (ML) at the design level. With its robust data-driven decision-making capabilities, ML not only complements Gilbert-Cell's architecture but dynamically optimizes it, ensuring efficiency and adaptability across a broad spectrum of conditions. Also, the utilization of ML in the design can help in using automation at the schematic level for any analog design.

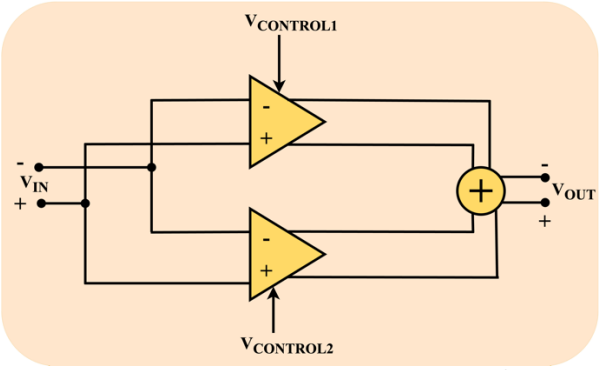


Fig. 1 Block diagram representing the variable gain amplifier using the gilbert cell configuration blocks

The advent of ML in hardware design presents a unique opportunity to overcome these challenges. By incorporating ML algorithms directly into the design process, unprecedented levels of precision and flexibility can be achieved. This paper introduces ML-based methodology along with the g_m/I_d technique popularly known as the transconductance efficiency factor (TEF) for designing a Gilbert cell-based VGA. A look-up table is constructed using the TEF data collection method in the design. Later, using the K-nearest neighbour (k-NN) search algorithm along with the spline interpolation to find the appropriate geometry of the Gilbert cell is obtained. Using the k-NN leads to the optimum values of cell geometry, leading to better circuitry performances. The design is particularly notable for its ability to efficiently handle low-frequency signals, which is common in medical imaging, audio technology, and seismic data analysis.

The preliminary results show that ML-enhanced Gilbert Cell-based VGA not only satisfies but surpasses conventional performance criteria, providing significant gains in gain range and power economy, which is discussed in the following sections. Section 2 of the document reviews various VGA architectures and the design methodologies of the amplifiers. Section 3 explains the method of the work, stressing an integrated approach to improve the design process by combining the TEF approaches with the k-NN search algorithm. Spice simulations show how this ML-enhanced approach enables more exact geometry of performance measures and design parameter optimisation. In section 4, data analysis is carried out, illustrating that k-NN techniques integrated with the TEF significantly enhance traditional techniques. Section 5 contains a brief conclusion highlighting the benefits obtained in VGA design through the proposed approach, marking a progressive step away from traditional analog circuit design practices.

2. Literature Review

VGAs are instrumental in systems requiring dynamic range adjustments, particularly in environments where signal strengths are unpredictable and vary widely. Automatic Gain Control (AGC) circuits are integral functions of VGAs to ensure the optimal signal amplitude, enhancing the overall system performance and efficiency. This functionality is crucial in applications ranging from audio processing in hearing aids to signal management in communication satellites or auto gain controlling in bio-medical signals, highlighting their broad applicability and necessity in modern technology. Recent studies have emphasized the importance of sophisticated VGA designs that cater to both open-loop and closed-loop configurations, each serving distinct purposes across various applications. In [14], the gain of the CMOS open-loop VGA is regulated by a variable g_m or load resistance (R_L). Regarding GM, the primary techniques for its adjustment include calibrating the bias current, partitioning the output current, optimising the source degeneration resistor, and employing a weighted switched MOS array to get a tuneable aspect ratio. Although the design exhibits commendable linearity, fluctuations in its output current adversely impact its performance. An open-loop architecture is favoured for high-frequency applications due to its low power consumption and minimal noise; however, it suffers from inferior linearity compared to closed-loop amplifiers operating at the same frequency [14, 15]. The gain in an open-loop VGA can be regulated, for instance, by variable transconductance or output-load impedance. Further, in [16], Song et al. use resistor arrays to generate the control signals,

where the performance is affected by the high resistive load. [17] uses the Gilbert-cell configuration to control voltage generated by changing the tail current. Again, in [3], this Gilbert-cell design is used in designing a 4-stack VGA. The Gilbert cell is used in a wide range of applications due to its high linearity output in varied gain. The gain-control mechanism of Gilbert-cell is a popular choice due to its simpler design and high-speed merits.

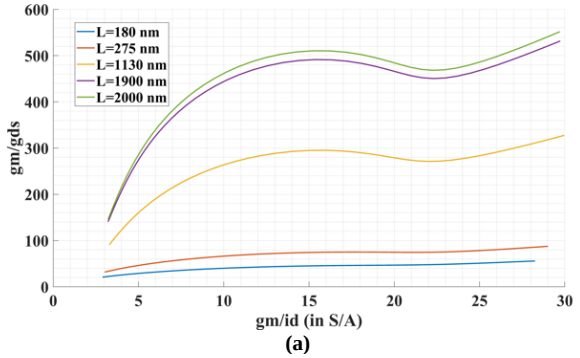
Even though VGAs have different configurations with wider capabilities, the design mechanism is still widely based on traditional approaches. The main part of the VGA is the design methodology of the operational transconductance amplifier (OTA), which is based on conventional methods like square law [18], bias point simulation approach [19], iterative simulation, etc. These methods do not properly adapt to the newer technology nodes; hence, the designer goes for the hit trial methods. This causes the design time to increase. In [20], Silveria et al. introduced the gm/Id or TEF methodology, which is quite capable of using different technology nodes. The TEF method basically uses the characteristics graph of the transistors and utilizes it for the design. This method has been properly discussed in [21, 22]. But still the method lacks a data-driven approach for completely making the design process robust. With the advent of ML, the optimization and design of the OTA have seen a shift. In [23], the author employed precomputed tables to design a Bandgap voltage reference circuit. Subsequent to this research, Wolfe et al. [24] and Lberni et al. [1] employed machine learning approaches in two-stage OTA design, demonstrating the efficacy of machine learning in managing the nonlinearities intrinsic to transistor models. In this work, VGA is designed by combining the TEF method with the k-NN algorithm. The detailed method is discussed in the following sections.

3. Materials and Methods

This section delineates the systematic approach undertaken to design and optimize the VGA using 180nm Semiconductor Lab (SCL) CMOS technology. The methodology is characterized by meticulous transistor-level analysis and the integration of machine learning techniques for parameter optimization. The details of the methodology are described in the following subsections.

3.1. Transistor Characterization

The design process starts with an extensive characterization of NMOS and PMOS transistors, meticulously capturing the different device parameters across transistor channel lengths ranging from 180nm to 10.8 µm. Critical parameters such as transconductance (g_m), output conductance (g_{ds}), drain current per unit width (I_d/W or J), gate-source voltage (V_{gs}), drain-source voltage (Vds), threshold voltage (V_{th}), and drain current (I_d) were collected through SPICE simulation. This detailed collection of data lays the groundwork for understanding the varied behaviors of transistors at different dimensions, proving invaluable for the detailed transistor-level analysis required in subsequent phases of the circuit design [7-9]. As the data collected during transistors are large numbers, proper visualization and very few values of channel lengths were chosen for the transistors. The plots for NMPOS and PMOS are shown in Figures 2 and 3, respectively.



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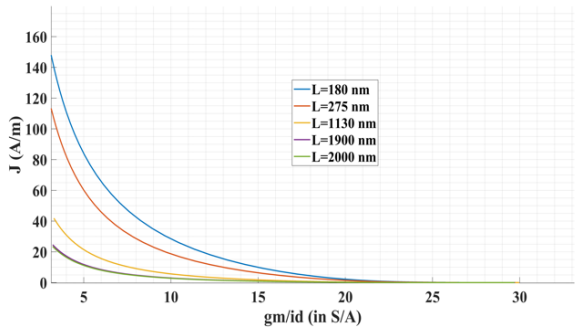

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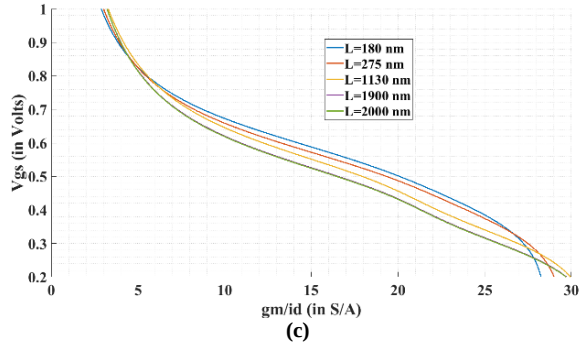

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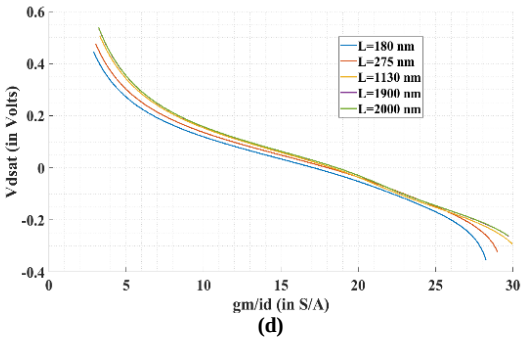

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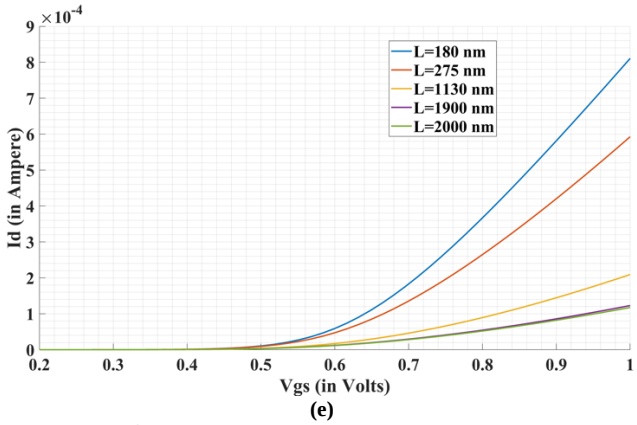
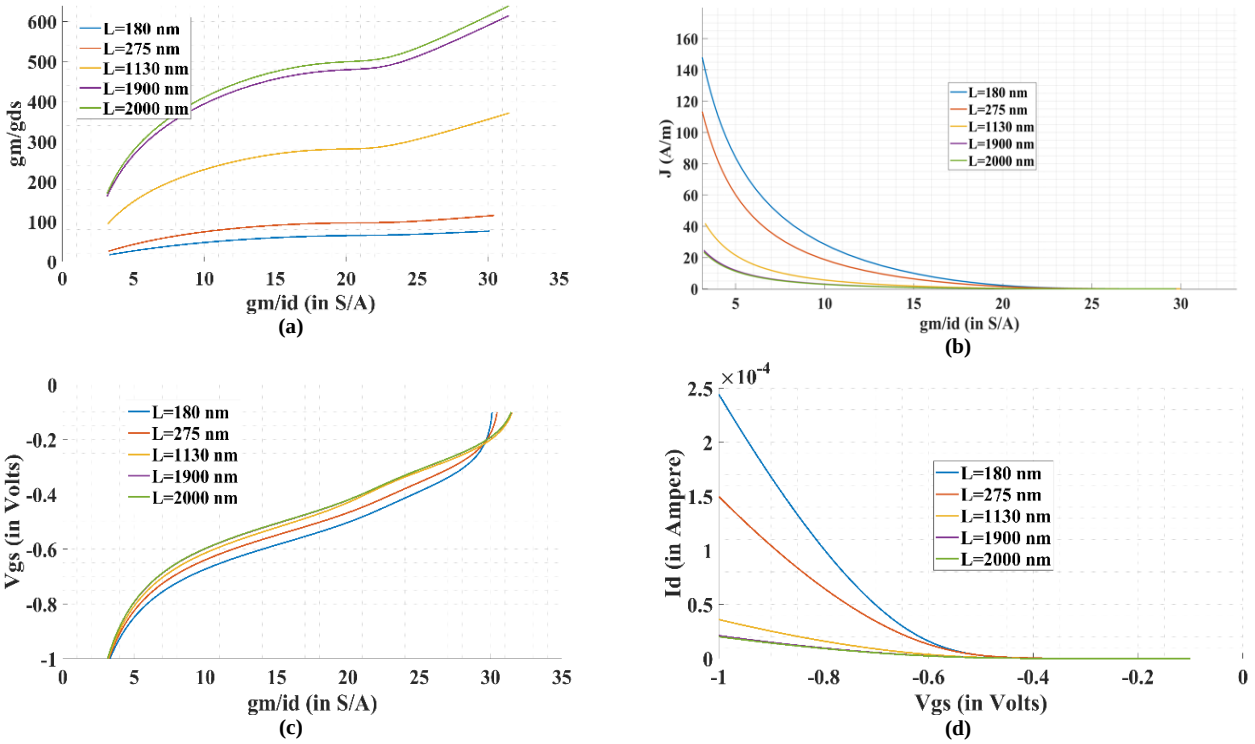


(e)

Fig. 2 Different plots plotted with respect to g_m/I_d for NMOS transistor (a) g_m/I_d Vs g_m/g_{ds}, (b) g_m/I_d Vs J, (c) g_m/I_d Vs V_{gs}, (d) g_m/I_d Vs V_{dsat}, and (e)V_{gs} Vs I_d.



(a) (b) (c) (d)

Fig. 3 Different plots plotted with respect to g_m/I_d for PMOS transistor (a) g_m/I_d Vs g_m/g_{ds}, (b) g_m/I_d Vs J, (c) g_m/I_d Vs V_{gs}, and (d)V_{gs} Vs I_d.

3.2. Creation of Lookup Table for Transistor Characterization

Using the extensive data gathered from the detailed characterization of NMOS and PMOS transistors, a comprehensive lookup table (LUT) is created. This LUT consists of critical transistor parameters such as g_m/I_d, g_m/g_{ds}, I_d/W, V_{gs}, V_{ds}, and V_{th} for varying channel lengths (L). The LUT serves as an important resource, enabling swift and precise parameter selection that adapts flexibly to different operational needs, thus streamlining the design iterations and enhancing the optimization process for OTA designs [21, 22]. The LUT so obtained is created using a Python 3.11 environment. The different plots for the data obtained are shown in Figures 2 and 3 for NMOS and PMOS, respectively. Around 92k data were collected, and LUT was created with the transistor characterization data.

3.3. k-NN Algorithm Application on LUT

In the design process, the k-NN algorithm is used precisely to determine the suitable values of 'L' that meet the design criteria. This ML algorithm effectively uses the LUT to identify the 'L' value that aligns closely with the targeted parameters, such as desired g_m/g_{ds} ratios for a given TEF value. By analyzing proximity within the feature space, the k-NN algorithm predicts appropriate 'L' values, ensuring high accuracy in component selection even in scenarios where an

exact match is unavailable in the LUT. The LUT is later used to design the differential pair, current mirror, and tail current source, which is later used in the design of the Gilbert cell.

The k-NN algorithm is a flexible and efficient method for both classification and regression tasks in supervised ML [25]. In this work, the k-NN technique is utilized to search for tasks. It determines outcomes based on the mean values from the nearest data points in the training dataset. Notably, the k-NN algorithm demands no preliminary training phase, making it swift as it relies solely on the incorporation of data. The process begins by measuring the Euclidean distances (ED) between data points, a crucial step for employing the k-NN algorithm in regression models, as depicted in equation 2. *d(x,y),* is the ED [26].

$$(x, y) = \sqrt{\sum_{i=1}^{n} (x_i - y_i)^2} \tag{2}$$

$$\hat{y}(x_{new}) = \frac{\sum_{i=1}^{k} f_i y_i}{\sum_{i=1}^{k} f_i} \tag{3}$$

On determining the distance metrics, the k-NN process searches for the *k* closest neighbours to the fresh data point, referred to as x_{new} within the training dataset. Typically, x_{new} is calculated as the mean of the dependent variable *y* from these nearest neighbours. The anticipated value is presented in Equation (3) with $f_i = \frac{1}{d(x_{new}, x_i)^p}$ and *p=2* [27]. The Scikit-learn [28] toolkit in Python is utilized to provide various functionalities for the k-NN prediction tasks. The following sections detail the data collection, preprocessing, and training procedures, all aimed at accurately predicting the aspect ratio for the Gilbert-cell configuration.

3.3.1. Searching the Data from the LUT

The requisite data is produced for the SCL 180 nm CMOS technology node utilising the SPICE simulator. The simulations were conducted within a Python framework, with results confirmed through Cadence's SPICE or Spectre simulator for accuracy. The data handling and training processes were executed on a system powered by an AMD Ryzen 3 3200G processor at 3.20 GHz, integrated with Radeon Vega Graphics and equipped with 16GB of RAM, using Python version 3.11. The scikit-learn library is utilized in this work, and it is highly regarded for its extensive set of tools that support data normalization, model training, and detailed evaluation. This library is selected due to its proficiency with a range of machine learning algorithms, which is crucial for achieving the objectives of the analog design. The performance of the models is thoroughly assessed using established metrics like Mean Absolute Percentage Error (MAPE) and R-squared (R^2), which are given in equations 4 and 5. These metrics are vital as they offer a robust quantitative basis for assessing the models' accuracy and predictive power, thereby confirming the reliability and efficacy of the analytical methods used in this design process.

$$MAPE = \left(\frac{1}{n} \sum_{i=1}^{n} \left| \frac{y_i - \hat{y}_i}{y_i} \right| \right) \times 100 \tag{4}$$

$$R^2 = 1 - \frac{\sum_{i=1}^{n} (y_i - \hat{y}_i)^2}{\sum_{i=1}^{n} (y_i - \bar{y})^2} \tag{5}$$

3.3.2. Spline Interpolation in the Data Search

In the methodology, when the k-NN algorithm sweeps the LUT and encounters absent data points, it generally yields a null value. This can derail any analog design process. To effectively manage these gaps, spline interpolation is incorporated into the data retrieval process from the LUT. The method can significantly improve the accuracy of the k-NN algorithm. The missing data points are obtained by integrating interpolated values encountered during the design. Within the framework of this design methodology, cubic spline interpolation is utilized. This technique constructs a smooth curve through existing data points, ensuring each query produces a meaningful and precise outcome. Such enhancements strengthen the robustness of the analytical models and also broaden their practical applications, making the datasets more effective for addressing real-world design challenges [29]. The curve is formed by combining a sequence of cubic polynomial segments between each pair of consecutive data points. Mathematically, for a set of data points (x_i, y_i) where $i = 1, 2,..n$, the cubic spline $C(x)$ on the interval $[x_i, x_{i+1}]$ is given in equation 6:

$$C_i(x) = p_i + q_i(x - x_i) + r_i(x - x_i)^2 + s_i(x - x_i)^3 \tag{6}$$

Where $p_i, q_i, r_i,$ and s_i are coefficients that are determined for each sub-interval based on the boundary conditions. The capability of cubic splines to construct a smooth curve through any sequence of data points ensures that each interpolation not only bridges the gaps in sparse data but also maintains the natural flow of the dataset's underlying trends. As a result, the application of cubic spline interpolation in k-NN-based systems broadens their utility in searching the OTA's geometry, which is later used in designing the 2-stack Gilbert-cell for the VGA application.

3.4. Gilbert Cell Design

The design of the Gilbert cell unit, as illustrated in Figure 4, depends on the 'L' values fine-tuned using the k-NN algorithm. This configuration lays the groundwork for designing the subsequent VGA configuration. The unit cell design integrates key components such as a differential pair, a current mirror, and a tail current source. The Gilbert cell meets

the required specifications by applying these optimized parameters obtained. The detailed geometry of the Gilbert cell is presented in Table 1.

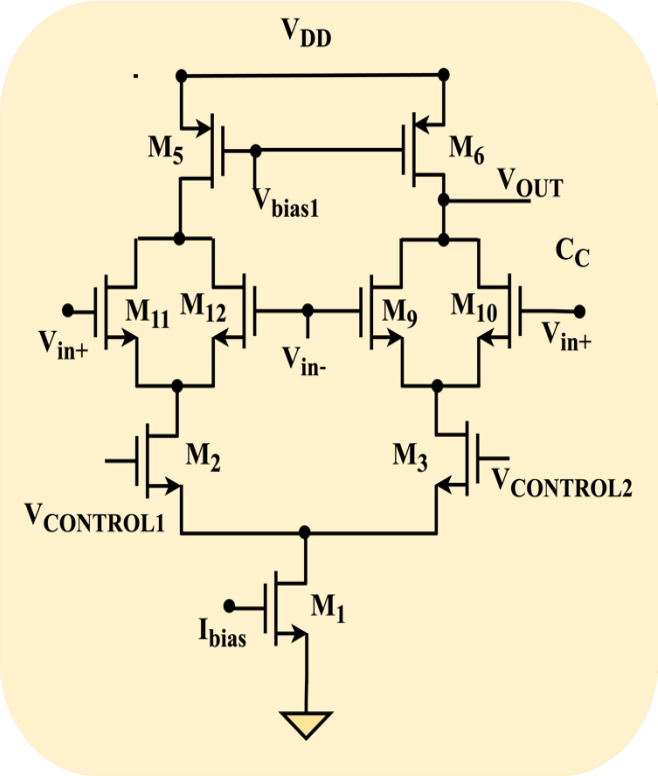


Fig. 4 Schematic of VGA using the gilbert cell configuration

Algorithm: Gilbert Cell Design Utilizing Integrated Method of KNN Search and TEF Technique

1. Design of Differential Pair (M_{11}, $M1_2$ and M_9, M_{10}):
   - Input Specifications: Retrieve essential parameters such as TEF, g_m/g_{ds}, and drain current (I_d) from the dataset.
   - Length Prediction:
     - Use the k-NN search to determine the 'L' of the transistors. Input the TEF and g_m/g_{ds} values into the k-NN algorithm to find the nearest set of data points in the dataset that match these specifications.
     - The algorithm should return the 'L' values from the dataset closest to the desired TEF and g_m/g_{ds} ratios.
   - Width Calculation:
     - Calculate the width (W) for transistors using the formula $W=I_d/(I_d/W)$, where I_d/W is retrieved from the nearest neighbours found by the k-NN search.
2. Current Mirror Load Design (M_5, M_6):
   - Conductance Parameters: Determine the g_m/g_{ds} values required for M_5 and M_6 from the design specifications.
   - Transconductance Prediction: Use the retrieved g_m/g_{ds} ratio for both M_5 and M_6.
   - Geometric Estimation:
     - Apply the k-NN algorithm to a PMOS dataset to predict the lengths of M_5 and M_6. Input the g_m/g_{ds} and 'L' values to find the nearest matches.
     - Calculate their widths based on the geometric parameters (like $W=I_d/(I_d/W)$ obtained from the nearest neighbour results in the dataset.
3. Tail Current Source Optimization (M_2, M_3 and M_1):
   - CMRR Alignment: Based on the desired Common Mode Rejection Ratio (CMRR) values, calculate the g_m/g_{ds} values for the transistors.
   - Geometry Determination:
     - Employ the k-NN search to estimate the geometric dimensions (length and width) for the transistors. This step involves inputting g_m/g_{ds} values into the k-NN algorithm and retrieving the closest matching geometric parameters from the dataset.

3.5. VGA Simulation

The final phase involved simulating the VGA under varying control voltage conditions to validate and refine the design. In the VGA, apart from the Gilbert cell, it has the common source amplifier (CSA) (M_7 and M_8) in the complete schematic.

The design steps for the CSA used the same steps as used for the cell design. This resulted in the increase of the maximum gain from 30 dB to 54 dB. Figure 5 shows the flow chart for the design of the CSA.

These simulations are crucial for verifying that the VGA meets the desired performance metrics across different operational states and identifying potential areas for further optimization. Figure 6 shows the complete VGA structure along with the common source amplifier.

Table 1. Summary of the transistor properties derived for the VGA cell through k-NN analysis

Transistors	W/L	Channel Width (in μm) with L_{min}=0.18μm
Input Pair Differential Amplifier	3	0.54
Current Mirror	15	2.7
Tail Current Source	4.5	0.81
CSA(M_8)	36	15
CSA(M_7)	36	5

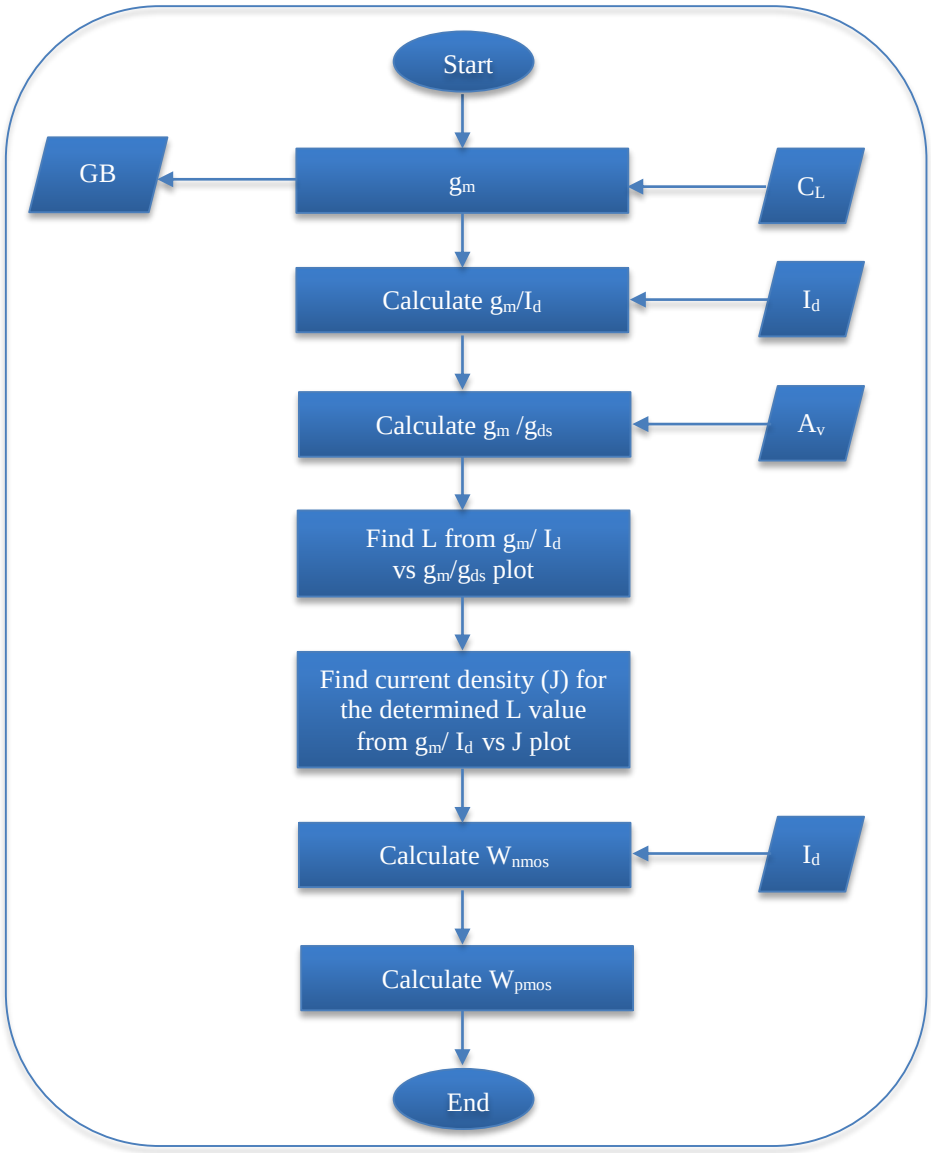


Fig. 5 The flow diagram illustrates the various stages of the k-NN methodology in designing the common source amplifier circuit

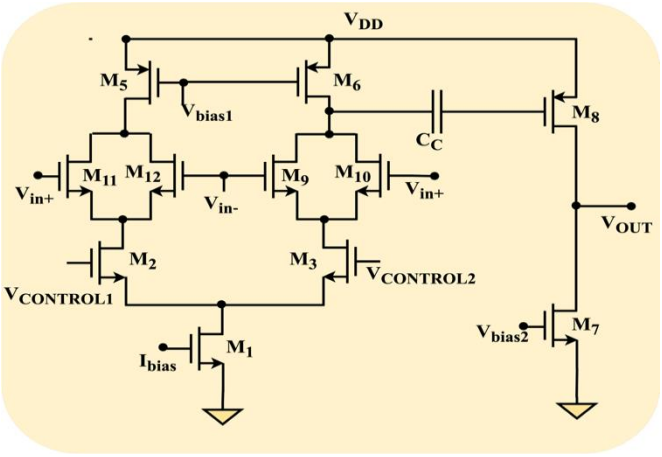


Fig. 6 Schematic of VGA using the gilbert cell configuration and common source amplifier

4. Results and Discussion

The LUT obtained from the SPICE simulations for both NMOS and PMOS transistors plays a crucial role in aiding the k-NN models in accurately determining the precise dimensions of the transistors. After extensive training and evaluation, the k-NN model displayed impressive accuracy. For the NMOS transistor data, the model demonstrated a remarkable R^2 score of 0.9603 and a Mean MAPE of 4.7%, showing its robustness and reliability in closely approximating the true data points. Meanwhile, for PMOS transistors, the model achieves an R^2 score of 0.9617 and a MAPE of 7.8%, which, although slightly higher, still demonstrates a reliable level of accuracy in predictions.

Figure 7 shows the AC analysis performed on the VGA. The gain varies from -20 dB to 54 dB. This variance is

controlled by adjusting the voltage from 0.1V to 0.9V, demonstrating the VGA's responsiveness to control voltage adjustments. The k-NN approach resulted in a power consumption of 10 mW. Figure 8 shows the Fast Fourier Transform (FFT) simulation results for the k-NN-based method, which achieves a third-order Harmonic Distortion (HD_3) of -78.79 dB. These simulation outcomes were recorded at 298K under typical corner conditions. Table 1 shows all the parameters of the VGA compared against the previous literature.

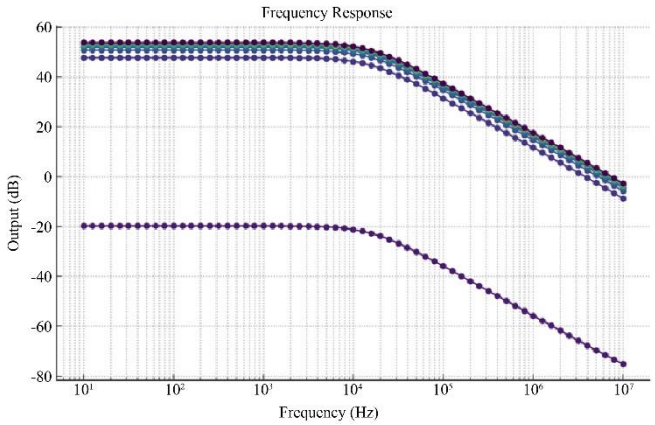


Fig. 7 Schematic of VGA using the gilbert cell configuration

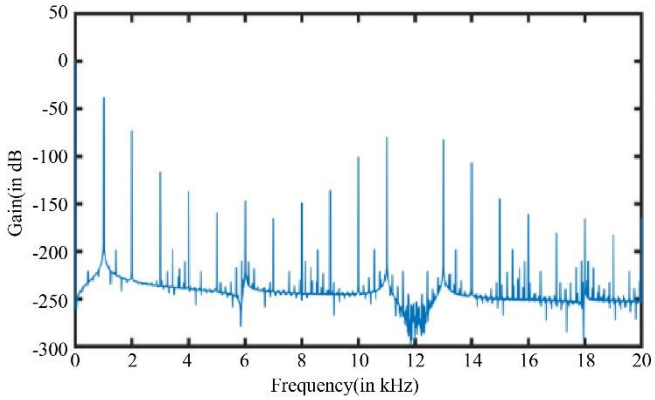


Fig. 8 Fast fourier transform analysis of the VGA in k-NN-based design approach

The integration of the k-NN algorithm, along with cubic spline interpolation, into the design of a VGA using a Gilbert Cell configuration marks a notable evolution in the field of analog circuit design. This research highlights how machine learning can enhance the process of selecting transistor dimensions, greatly improving the functionality and efficiency of VGAs designed for low-noise environments. Using k-NN to search through the precomputed LUT to select the transistor dimensions proves effective against the traditional methods. Further, this method utilizes the TEF calculations to satisfy the specification, which stands out as particularly effective. This method greatly simplifies the design process, cutting down on the need for repetitive manual tuning and the usual hit-and-trial method in analog circuit design, thus making the design process more data-centric. The initial results, which show high R^2 scores and MAPE for both NMOS and PMOS datasets, verify the k-NN model's effectiveness in making precise predictions that closely mirror the real data points.

Table 2. Comparative analysis between k-NN based design of gilbert cell with respect to literature

Parameters	This Work	[10]	[11]	[12]
Technology (in nm)	180	180	250	65
Range of Gain (in dB)	-20 to 54	13.2	31	-39.4 to 20.2
Power Consumption (in W)	10m	700µ	350m	26m
Phase Margin (in degrees)	70	NA	NA	NA
Bandwidth (in Hz)	1M	2.4G	40G	4G
HD_3 (in dB)	-78.79	NA	NA	27

Moreover, by interpolating missing data points, this technique ensures the continuity and integrity of the ML model's output, thereby enhancing the utility and applicability of the k-NN algorithm in real-world design scenarios. This method ensures that the model's utility is not compromised by the lack of direct matches in the LUT, thus maintaining the integrity and continuity of the data analysis process.

5. Conclusion

This work presents the process of integrating ML and TEF into the design and fine-tuning of Gilbert Cell-based VGAs. By utilizing the k-NN algorithm together with cubic spline interpolation, significant improvements have been made in the precision and adaptability of VGA designs. This enhancement has streamlined the design process considerably. The introduction of ML techniques has also advanced automation in analog circuit design, leading to workflows that are both more efficient and more cohesive. Finally, this method can offer designers the tools to achieve precision and efficiency. It paves the way for creating more intelligent, adaptable, and energy-efficient electronic systems, which are both robust and driven by data.

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