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Original Article

Control and Analysis of a Power System From a Dual IPC_240 System Controlled by FPGA in High Contingencies Situations

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Abstract *- This work presents automatic management methods for handling single-phase or two-phase faults on an electrical power transmission line, enabling the redirection of power flow from the defective phase to the normal phases. When one or more phases are disconnected, the automated system provides a portion of the rated power on the receiving side while maintaining the three-phase balance of the load supply. In the event of a fault, alerts are sent in real-time to operators via SMS on their phones or by email, accompanied by an audible alarm and the activation of the relevant indicator lights. This type of work is particularly crucial for both developing countries and developed nations facing frequent short circuits in power transmission networks, as it improves system flexibility and reliability. The Field Programmable Gate Array (FPGA), combined with a communication module and programmed in VHDL, generates a series of logic gates. It was integrated into the QUARTUS II environment for real-time monitoring of its operation.* The outcomes of the simulations *confirm* the possibility of implementation *and effectiveness of the two 240 interphase power controller technologies in managing energy flow,* both in standard situations and in times of emergency. *Overall, the results demonstrate that using two interphase power regulators, one on the source side and the other on the load side, ensures 98% stability in the transmission of electrical energy*.

Keywords *- Control, System from a dual, IPC, FPGA, High contingency.*

1. Introduction

The FACTS (Flexible Alternating Current Transmission Systems) system was developed and is part of a wide range of advanced electronic technologies designed to compensate for symmetrical energy in electrical networks, whether they are subjected to normal or unforeseen operating conditions. For instance, if a short circuit happens on one phase of a transmission line, the remaining unaffected phases are shut down; however, unlike FACTS, the Interphase Power Controller (IPC) technology was developed to passively compensate for asymmetric energy in unforeseen situations using standard reactive devices. It has been demonstrated that when a fault happens on one or two phases, a network fitted with an IPC can continuously supply less energy to a load terminal, proportionally to the number of active phases remaining [1-3], for example, 2/3 of the rated power if a pair of phases are unaffected, and one-third of the rated power is available if only a single phase stays active. Interphase power controller technology has attracted growing interest among researchers and power system professionals following its adoption. As a result, several innovative IPC topologies are available in the literature, and each is adapted to the internal control parameters used to provide passive compensated energy to electrical networks. The most widely used control parameters are usually the phase angle of a transformer's phase shift.(e.g., interphase power controller 60 and 20), or the susceptances of reactive elements (e.g., interphase power controller 120 and 240) [4]. A typical interphase power controller 240 topology consists of two parallel branches of reactive elements with conjugate impedance values at the fundamental frequency level. The automatic management of one-phase-phase or two-phase faults on a power transmission line, usually characterized by high short-circuit levels, is performed using a Programmable Logic Controller (PLC) associated with a communication module, which uses standard logic gates such as NOT, AND, and OR.

The authors' work highlights the reliability of 240-type IPCs in managing power flows and signalling systems with various types of faults, including symmetrical and asymmetrical short circuits, current dips, symmetrical and asymmetrical overloads, as well as voltage fluctuations or flicker effects, affect power transmission networks [4].

Some researchers evaluate the impact of short circuits and other disturbances, such as non-periodic distortions affecting network currents and voltages, leading to phase losses in a power transmission network. To address this, IPCs at the source and load are used to suppress these irregular distortions, thus improving network stability [5].

The stability of the power transmission system is then analysed using the UPFC FACTS system, employing the Newton-Raphson method and power flow continuation techniques. A comparative study between the Static VAR Compensator (SVC) and UPFCs is also conducted, including stability margin analysis for these compensators [6].

In most applications, one interphase power controller 240 is positioned between the source and the receiver. However, a significant drawback of this system is that, if power transmission is impaired due to a phase failure, unbalanced AC current is continuously supplied to the receiver. As a result, most three-phase receivers cannot operate correctly during contingency situations. One application of the interphase power controller 240. A three-branch FACTS system has been examined. Where a double IPC is applied on both the source and load sides for unbalanced power compensation in an AC electrical grid [1, 7].

Nevertheless, while simulations yield high-quality results, an FPGA board for energy system compensation within a dual configuration interphase power controller 240 setup, it is essential to note that the handling of required or excess reactive components prior to and during unforeseen periods has been performed manually, an automated control mechanism, as typically anticipated in the practice of energy flow automation.

The key contributions of this paper are: Advanced stochastic FPGA control, integrating multiple RPIs, ensuring the continuity of electrical networks with multi-source management;

- Automatic control of dynamic networks, aimed at improving the compensation of electrical energy in transmission networks during contingency events or significant disturbances such as short circuits or phase loss;
- Automatic opening and closing of circuit breakers in case of faults, with automation of energy flow control on the network.

The rest of this article, in Section 2 (Materials and Methods), describes two 240 interphase power regulators and intelligent circuit breakers placed upstream and downstream of the transmission line, controlled by a PLC associated with a communication module. Analytical and numerical methods will be used to conduct our research alongside the Matlab tool, version 2019. Section 3 presents several simulation results with the FPGA module, integrating various operating scenarios. A detailed analysis of each scenario is provided. Finally, Section 4 concludes with a summary of the main contributions of this work, their impact, and their support for development in various countries, including emerging ones, with future research prospects.

2. Literature Review

Improving electric power quality has long been a subject of extensive research. Among these efforts, L. Zahedi, Mehdi S. Naderi, and others proposed in 2011. The issue highlighted by these authors was the elevated short-circuit levels within the power transmission grid. In order to tackle this, they focused on designing IPC components using a multi-step algorithm.

In 2015, Jean Jacques Mandeng and Jean Mbihi conducted research and made another proposal. They also tackled the issue of high short-circuit levels in the transmission network. Their solution involved using two IPCs on the source and load sides, manually simulating a short circuit to test whether the IPCs could ensure asymmetric compensation of the line [8]. A year later, in 2016, Mohammad Amin Chitsazan and colleagues made another proposal [9].

This study addressed the issue of harmonic disturbances in the transmission network and proposed using a passive filter coupled with the IPC to reduce harmonic effects. In the same year, Harsha Nagarajan and colleagues made another proposal. The main issue highlighted by the authors was natural disturbances (e.g., wind, tornadoes, storms) affecting the power transmission network. They proposed using FACTS devices and transformers to mitigate these issues to enhance grid resilience [10].

In 2017, Jean Jacques Mandeng, Jean Mbihi, and Charles Hubert Kom made another scientific contribution. The problem they addressed was again the high short-circuit levels in the transmission network. Their proposed solution involved using two IPCs on the source and load sides connected to the line via circuit breakers controlled by wired logic [13].

Several years later, in 2023, Mougnol Assala conducted research made another scientific contribution. This study used a three-branch interphase power controller 240 for unequal compensation coupled with a solar photovoltaic system to offset the loss of transmitted power.
[7].

3. Matérials and Methods

3.1. Materials

The advancement of Interphase Power Controller technology has primarily been driven by the necessity to develop new power flow designs and control devices capable of overcoming the operational limitations of electrical networks, often related to excessively elevated fault current levels. Indeed, these elevated fault current levels represent a commonly used issue, but one that has undergone largely neglected in the design of FACTS systems [1, 8, 12].

However, the adaptability and dependability of transmission and distribution networks may be significantly improved by integrating circuits or interconnection points that do not contribute to increasing short-circuit power [13]. Despite global advancements in developing fault-current limitation devices, IPCs remain an effective and cost-efficient solution. Given that power transmission lines are frequently subjected to one-phase or dual-phase faults, deploying an automated dual interphase power controller system becomes essential to ensure the continuous operation of the network, even in the presence of such disturbances. In this context, we present in this section an architecture featuring two 240-type IPCs, along with smart circuit breakers installed upstream and downstream of the transmission line. This is controlled by a Programmable Logic Controller (PLC) coupled with a communication module. For this study, we employ both analytical and numerical analysis methods, using MATLAB 2019 as the environment.

Table 1. Topological characteristics of IPCs [18, 19]

Topology		Quantity of Branches	Type of Branches	Phase Displacement Method	Angle δ_{sr} (in Degrees)	Setting Process
Synchrone	240	2	Simple (C or L)	Connection	240	Susceptance
	180			Transformation	180	
	120				120	
	30P15 30M15				30	
	60 with 90° injection			Injection	0 à 60	Phase shift
	20 with variable injection				Zero to twenty	Phase shift and conversion ratio
Asynchrono	3 branches	3	Double (C and L	Transformation	120	Susceptance
	4 branches	4			90	
	4 branches and points	4				

3.1.1. Interphase Power Regulator

The Interphase Power Controller (IPC) comprises three-phase inductors and capacitors installed in series between two networks or sub-networks. Compared to other series compensation devices, its distinctive feature lies in its specific connection configuration to the network. For example, the inductor associated with phase A of one network might be connected to phases B and C of the other network. Once all components are energized, the current's amplitude and phase angle (δ) are determined at one of the regulator's two connection points (buses). Current regulation thus allows for adjusting the active power passing through the regulator, along with the reactive power either absorbed or injected at one of the buses. Within this model, the inductors and capacitors are assumed to be ideal, meaning they have no losses. The impedances of the series components are reduced to their imaginary component or, more specifically, to their reactance. In the operation of the regulator, where the series components are connected in parallel, the term susceptance applies is more commonly used than *reactance*, for convenience (B = -1 / X).

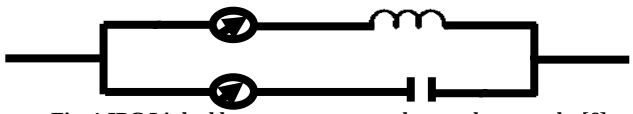

Fig. 1 IPC Linked between two networks or sub-networks [6]

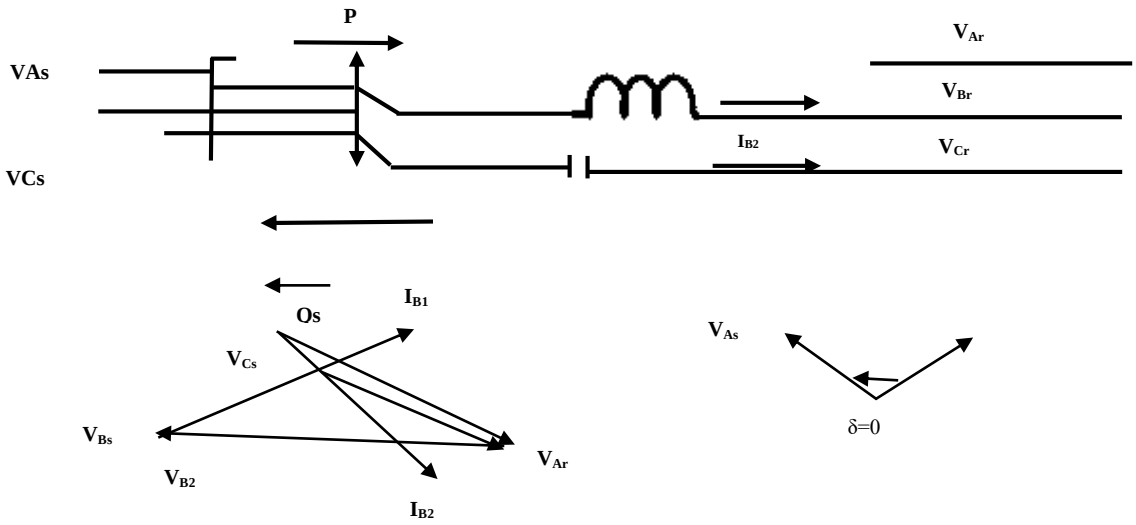

Fig. 2 IPC 240 fitted with switches for reversing the angle of +60° and -60° to voltage

IPC innovation has enabled the development of various devices with configurations that can vary depending on specific applications. Before delving into the details of Interphase Power Controllers (IPCs), it is essential to examine a few examples illustrating the flexibility of this technology, along with the significance of the analytical tools that will be presented later. Table 1 highlights the key characteristics of different IPC topologies. One of the key factors in an IPC is the number of branches it contains. Typically, a one-phase IPC circuit can have parallel branches, but in practice, this number is kept to a minimum to reduce the device's size and cost. The number of branches needed is determined by the range of the angle δsr across the IPC terminals [1].

Depending on the type of busbar used, there are two categories interphase power controllers can be categorized into synchronous and asynchronous types. The chart below presents a summary of the different IPC topologies. Since our study focuses on IPC 240, the rest of our analysis will be dedicated to this specific configuration. The figure below illustrates two-phase susceptances connected to a set of switches that allow for reversing the direction of active power flow, P. This active power P is considered positive when energy transfer occurs from the source side to the load side. Reactive powers Qs and Qr are positive when the IPC injects reactive power into the buses it is connected to. The susceptances B1 and B2 are connected to the voltage points V_{CS} and V_{BS}, respectively. The inversion of the energy flow is achieved simply by changing the connection of the susceptances on the s terminal and swapping the positions of B1 and B2. This technique of reversing the energy flow direction is applied to all interphase power controllers (IPCs). The name IPC 240 comes from the fact that the susceptances B1 and B2 are linked to the voltage points VCS and VBS, which have a phase shift of 240°.

$$\begin{cases} \varphi_1 = -120° \\ \varphi_2 = 120° \end{cases} \qquad \gamma = \varphi_2 - \varphi_1 \qquad (1)$$

The Equation (1) presented earlier highlights the value of the angle γ = 240°, which justifies the name IPC 240. The phase current IAr corresponds to the total of the currents IB1 and IB2, flowing through the susceptances in the direction of active power flow. The diagram illustrates a simplified equivalent circuit for IPCs employing conjugate susceptances.

Influence of different IPC Parameters

This paragraph demonstrates that the IPC provides reliable and predictable control of active power through the use of fixed-value susceptances provided that the angle δ across that interphase power controller terminals remains within a ±25° range; there is no need to subdivide or switch the susceptances to regulate the power flow. Switching, however, becomes necessary when adjusting the power level or generating/absorbing a specific amount of reactive power. Initially, the regulator is analysed in a network consisting of two buses considered infinite to observe its impact on power characteristics, leakage impedance, terminal voltage, and the behaviour of switching susceptances. It is then connected between two buses with equivalent Thevenin impedances, demonstrating that its characteristics remain virtually unchanged, regardless of the short-circuit levels of the networks. The calculations are carried out considering a nominal voltage on each side and a transformation ratio m = 1.

Transformer Leakage Impedance

The angular offset between the sources is now shared between the series impedances and the leakage impedance of the transformer. With power flowing from the S side to the R side, the angle across the susceptances decreases, resulting in

an increase in the reactive power generated by them [2]. This rise is particularly noticeable on the R side, where no transformer is present, leading to a shift of the reactive power Qr to the right. The leakage impedance of the transformer then absorbs a portion of the reactive power produced by the susceptances.

Subnetwork Short-Circuit Impedance

The two sub-networks are modelled according to the Thevenin equivalent to analyse the impact of their short-circuit impedances on the behaviour of the IPC. The nominal power of the regulator, for an angle $\delta = 0°$, is set to 1 p.u., while the short-circuit power of the relevant sub-network is 15 p.u., corresponding to a typical value for an urban network. The susceptances used by the regulator are identical to those used in the previous cases. In this context, the inductive and capacitive components of the interphase power controller have a reactance about 25 times higher than the short-circuit impedance Zth of the sub-network, viewed from each side of the device.

Even though the thevenin equivalent impedance on the s side increases by 98%, the real and imaginary power characteristics are only slightly modified. This situation, however, represents a critical scenario, as it implies a halving of the short-circuit level [2]. Thus, daily or seasonal load fluctuations and variations due to maintenance operations or unforeseen situations have only a limited impact on the performance of the IPC. It is important to highlight that in the case of such disturbances, the interphase power controller can contribute to stabilizing the voltage by injecting or absorbing reactive power while limiting the transfer of active power between the two sub-networks.

3.2. Methods

The approaches adopted in this study rely on both analytical and numerical methods. For the analytical part, starting from the functional diagram representing the implementation of a dual IPC 240 three-branch system connected in interphase to an electrical power transmission line, we develop mathematical models that represent the control laws. These models are used to structure the FPGA access control list, from which a flowchart is then designed. In parallel, the numerical method involves simulating the VHDL code in the QUARTUS II environment to compare the obtained results with the theoretical predictions and assess their consistency and performance.

3.2.1. Operation of the IPC 240 Dual System

Operation of the IPC 240 dual system linked to a power transmission line through three branches. Think about the case of an alternating current transmission line, integrating a system consisting of a 240 IPC on the source side (S-IPC), a transmission line, a 240 IPC on the receiver side (R-IPC), and a series of smart circuit breakers positioned both upstream and downstream (d1 and d4 for phase a, d2 and d5 for phase b, d3 and d6 for phase c). This system is controlled by a programmable FPGA. The individual reactances of the source interphase power controller are modulated using switches labelled S1 to S9, while an equivalent set of switches S1' to S9' manages the reactances of the R-IPC. Thus, a total of eighteen switching reactances must be controlled, both in normal operation and during disturbances, while ensuring synchronization between the two IPC 240s. If a phase of the line is exposed to a critical risk, such as a short circuit, the corresponding circuit breakers deactivate that phase. The FPGA then intervenes to redirect the energy flow to the still operational phases. Through the integrated communication module, technicians can receive real-time alerts for any anomalies affecting the line, enabling them to react quickly if the failure persists.

The added value of this double IPC 240 architecture lies in its ability to maintain a three-phase electrical supply to the receiver terminal, even in the presence of significant faults such as a short circuit in a single-phase or two-phase system. The three-branch charge interphase power controller ensures an efficient redistribution of power from the still-active phases. The FPGA, at the heart of the system, thus represents an innovative and effective solution for optimizing power flow management in alternating current networks using a dual IPC topology. In the initial phase, it becomes crucial to determine the input and output parameters that the access control list of the dual interphase power controller 240 setups will manage and examine the collected data.

The main variables involved in this context, whether input or output, are summarized in the table below. It is also essential to fully understand the main operations and commands related to the functioning of the studied system. Under normal conditions (i.e., in the absence of any disturbance), all switching commands for the peripheral elements must initially be activated. In these conditions, the two-interphase power controller 240 system operates as an ideal power transmission system.

In the event of a significant fault in phase A (such as a single-phase short circuit), the smart circuit breakers D1 and D4 will automatically deactivate this phase. The states of these circuit breakers will be detected by the access control list, which will then order the activation of the necessary reactances (Xaas, Xbas, Xcas, Xbbs, Xccs) and (Xaar, Xbbr, Xacr, Xccr) while excluding those that have become unnecessary in the dual IPC 240 system. A similar reasoning can be applied to all single-phase or two-phase fault cases. The structure of the envisioned access control list is presented in the table below [8, 17].

Truth Table to be Coded in VHDL

Table 3 provides a truth table intended for implementation in VHDL according to several determining parameters for the in-depth analysis of the system.

Table 2. PLC truth table

Combined Contingency Detection Marginal State Inputs d1, d2, d3, d4, d5, d6			**Output Variable and Reactance to be Switched**									**Transmission Line Power Flow Mode**	**Signalisation**
d36= d3.d6	d25= d2.d5	d14= d1.d4	S1 S1'	S2' S2	S3' S3	S4' S4	S5' S5	S6' S6	S7' S7	S8' S8	S9' S9		
Phase C	Phase B	Phase A	Xaas Xaar	Xbas Xbar	Xcas Xcar	Xabs Xabr	Xbbs Xbbr	Xcbs Xcbr	Xacs Xacr	Xbcs Xbcr	Xccs Xccr		
0	0	0	0	0	0	0	0	0	0	0	0	3-phase fault	L1 = L2 = L3 = A= 1.
0	0	1	1	1	1	0	0	0	0	0	0	C and B fault	L1 = 0 ; L2= L3 = A = 1
0	1	0	0	0	0	1	1	1	0	0	0	A and C fault	L1= L3 = A=1 ; L2=0
0	1	1	1	0	0	0	1	0	1	1	1	C fault	L1=L2=0 L3= 1=A
1	0	0	0	0	0	0	0	0	1	1	1	Fault in A and B	L1=L2=1 ; A=1 ; L3=0
1	0	1	1	0	0	1	1	1	1	1	1	B fault	L2= 1=A ; L1=L3=0
1	1	0	1	1	1	0	1	0	0	0	1	A fault	L1=1=A ; L2=L3= 0
1	1	1	1	1	1	1	1	1	1	1	1	No defects	L1 =L2=0 ; L3 = A = 0

3.2.2. Control Logic Equations

From the previous truth table, it is straightforward to represent each output variable sjs_j (where j=1, 2,9j = 1, 2, ..., 9) as a direct function of the combined input variables, according to the following relation:

$$S_1 = \bar{d}_{36}d_{25}d_{14} + d_{36}\bar{d}_{25}d_{14} + d_{36}d_{25}\bar{d}_{14} + d_{36}d_{25}d_{14} + \bar{d}_{36}\bar{d}_{25}d_{14} \quad (2)$$

$$S_2 = \bar{d}_{36}\bar{d}_{25}d_{14} + d_{36}d_{25}\bar{d}_{14} + d_{36}d_{25}d_{14} \quad (3)$$

$$S_3 = \bar{d}_{36}\bar{d}_{25}d_{14} + d_{36}d_{25}\bar{d}_{14} + d_{36}d_{25}d_{14} \quad (4)$$

$$S_4 = \bar{d}_{36}d_{25}\bar{d}_{14} + d_{36}\bar{d}_{25}d_{14} + d_{36}d_{25}d_{14} \quad (5)$$

$$S_5 = d_{36}d_{25}\bar{d}_{14}\bar{d}_{36}d_{25}d_{14} + d_{36}\bar{d}_{25}d_{14} + d_{36}d_{25}d_{14} + (6)$$

$$S_6 = d_{36}\bar{d}_{25}d_{14} + d_{36}d_{25}d_{14} + \bar{d}_{36}d_{25}\bar{d}_{14} \quad (7)$$

$$S_7 = d_{36}\bar{d}_{25}\bar{d}_{14} + \bar{d}_{36}d_{25}d_{14} + d_{36}d_{25}d_{14} \quad (8)$$

$$S_8 = d_{36}\bar{d}_{25}\bar{d}_{14} + \bar{d}_{36}d_{25}d_{14} + d_{36}d_{25}d_{14} \quad (9)$$

$$S_9 = \bar{d}_{36} d_{25} d_{14} + d_{36} \bar{d}_{25} d_{14} + d_{36} d_{25} \bar{d}_{14} + + d_{36} \bar{d}_{25} \bar{d}_{14} \quad (10)$$

A new combined variable is introduced, allowing the can be expressed as follows:

$$S_{10} = d_{36} \bar{d}_{25} d_{14} + d_{36} + \bar{d}_{36} d_{25} d_{14} + d_{25} \bar{d}_{14} + d_{36} d_{25} d_{14} \quad (11)$$

The previous equations, once simplified, can be reformulated as follows:

$$S_1 = \bar{d}_{36} \bar{d}_{25} d_{14} + S_{10} \quad (12)$$

$$S_2 = \bar{d}_{36} \bar{d}_{25} d_{14} + d_{36} d_{25} \quad (13)$$

$$S_3 = S_2 \quad (14)$$

$$S_4 = \bar{d}_{36} d_{25} \bar{d}_{14} + d_{36} d_{14} + d_{36} d_{14} \quad (15)$$

$$S_5 = \bar{d}_{36} d_{25} \bar{d}_{14} + S_{10} \quad (16)$$

$$S_6 = S_4 \quad (17)$$

$$S_7 = d_{36} \bar{d}_{25} \bar{d}_{14} + d_{25} d_{14} \quad (18)$$

$$S_8 = s_7 \quad (19)$$

$$S_9 = d_{36} \bar{d}_{25} \bar{d}_{14} + S_{10} \quad (20)$$

$$L2 = \bar{d}_{25} \quad (21)$$

$$L3 = \bar{d}_{36} \quad (22)$$

$$A = \bar{d}_{25} + \bar{d}_{36} + \bar{d}_{14} \quad (23)$$

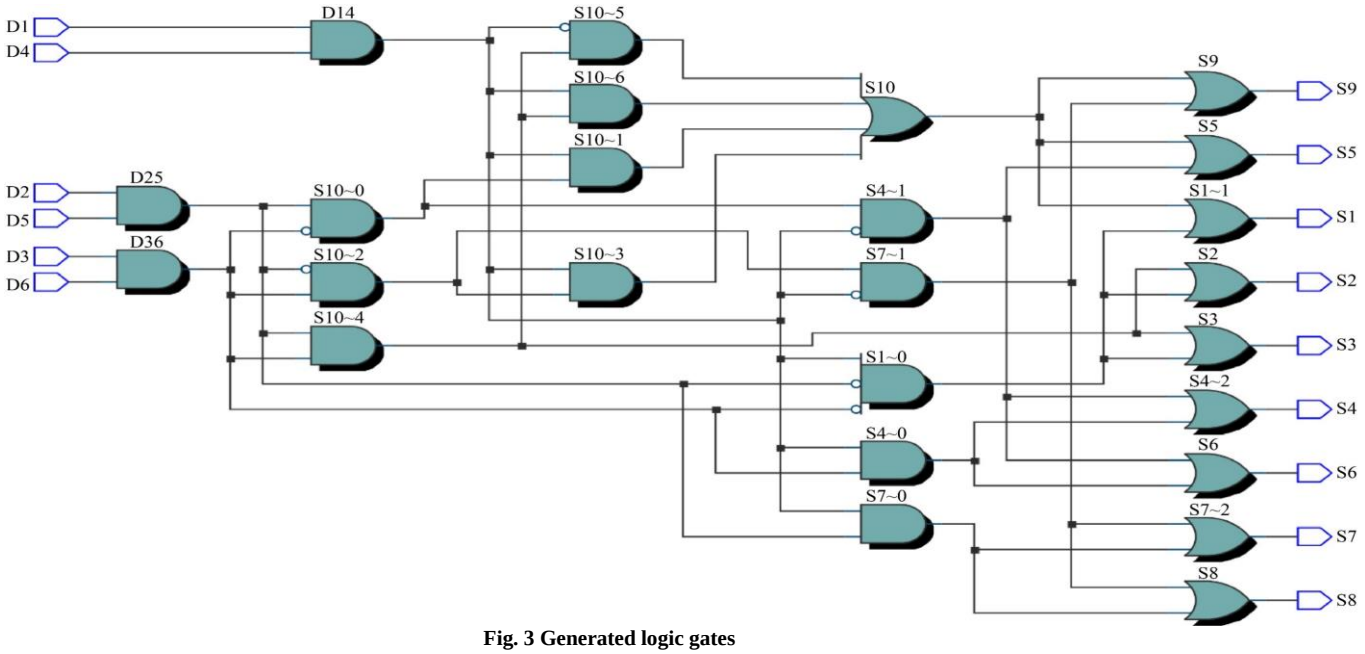

Fig. 3 Generated logic gates

Table 1. Table of input and outputs variables [16]

Symbols	Naturals	Descriptions
a',b' et c' ; a, b,c	Input	Data on load angle
d3, d1, d2	Input	Status of circuit breakers open or closed (D2, D1, D3 respectively)
d6, d4, d5,	Input	Status of circuit breakers open or closed (D6, D2, D5 respectively)
i9, i1, i5, i2, i8, i3, i4, i6, i7	Input	Switching status open or closed (S9, S1, S4, S2, S3, S5, S6, S8, S7 respectively)
S9, S1, S4, S2, S3, S5, S6, S8, S7	Output	The switching conditions of the line reactions linked to the source interphase power controller 240
L2, L1, L3, A	Output	Status of indicator lights and audible alarm
S9', S1', S4', S2', S3', S5', S6', S8', S7'	Output	That switching states from the line reactions associated with the charge interphase power controller 240

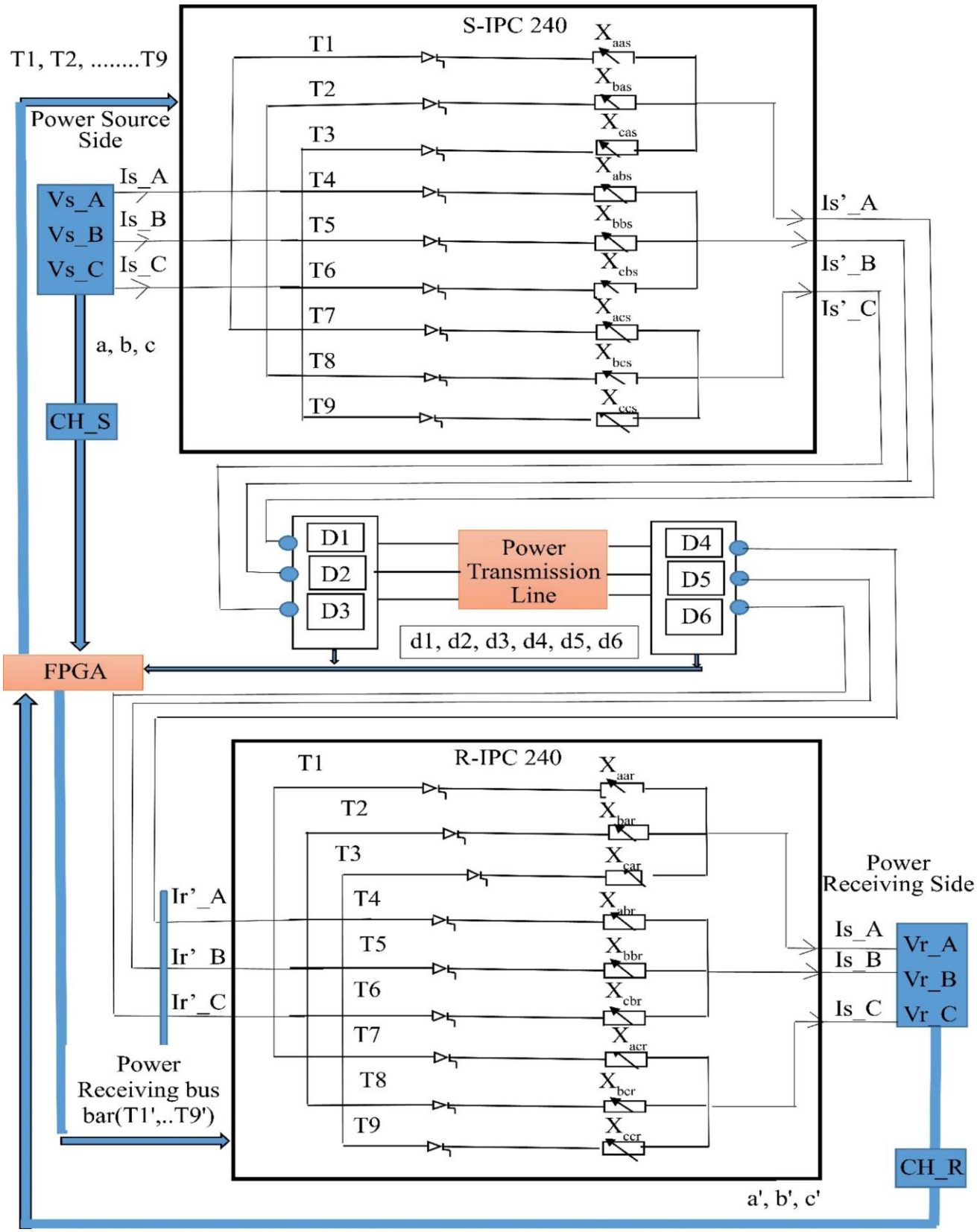

Fig. 4 Power transmission lines featuring an automated dual IPC 240 system integrated with an FPGA module

The set of these equations analytically represents the fundamental principles of PLC for a dual IPC 240 system. The entire set of these equations analytically translates the basic principles of a Programmable Logic Controller (PLC) applied to a dual IPC 240 system. From the compilation of the VHDL program, the flowchart corresponding to the operation of the dual IPC 240 system is generated.

4. Results and Discussion

4.1. Simulation of FPGA without Line Fault

All the input signals d1, d2, d3, d4, d5, and d6 are in logical state 1, indicating that all the circuit breakers are in the "ON" position. This means that no error is present in the transmission line. The figure below illustrates the simulation result under these conditions. Variables for different circuit breaker states

```
D1 <= '0' after 0 ns, '1' after 10 ns, '1' after 20 ns, '1' after 30 ns,
    '0' after 40 ns, '1' after 50 ns, '1' after 60 ns, '1' after 70 ns,
    '0' after 80 ns, '1' after 90 ns, '1' after 100 ns, '1' after 110 ns,
    '0' after 120 ns, '1' after 130 ns, '1' after 140 ns, '1' after 150 ns,
    '0' after 160 ns, '1' after 170 ns, '1' after 180 ns, '1' after 190 ns,
    '0' after 200 ns, '1' after 210 ns, '1' after 220 ns, '1' after 230 ns;
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(a)

(b)

Fig. 5(a-b): Signal with no faults on the line

When no anomaly is detected across all phases, the signals remain at a high logical level during the time interval from 0 to 240 ms.

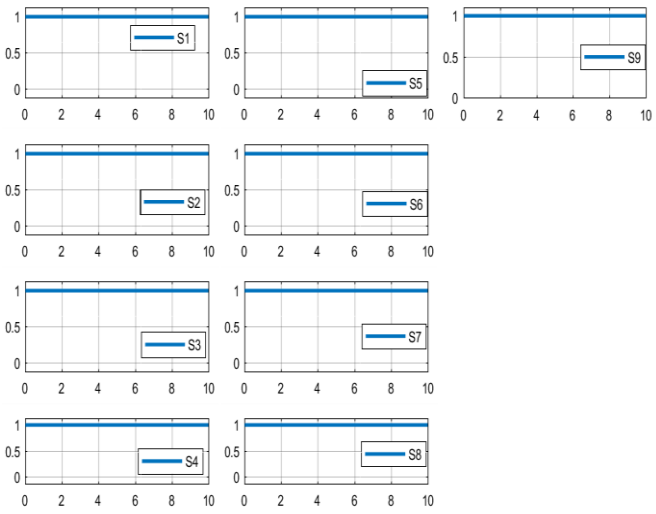


Fig. 6 Reactance states without line faults

Figure 7 above illustrates the states of the reactances when there is no fault on the transmission line. In fact, if there is no fault on the line, all input signals are at a high logical level (state 1), which results in the activation of all reactances S1 to S9, represented by the output signals also in state 1, confirming that the line operates without any contingency. Furthermore, the input signals d14, d25, and d36 also equal 1.

Fig. 7 LED status and audible alarm without line fault

Figure 7 above clearly indicates that none of the L1, L2, or L3 indicators or the A alarm is triggered to signal any anomaly on the line, which is explained by the fact that all these indicators are in the low state (0). As a result, no alert message will be sent to the operators, neither by SMS nor by email.

4.2. Simulation of the FPGA with a Fault in Phase A

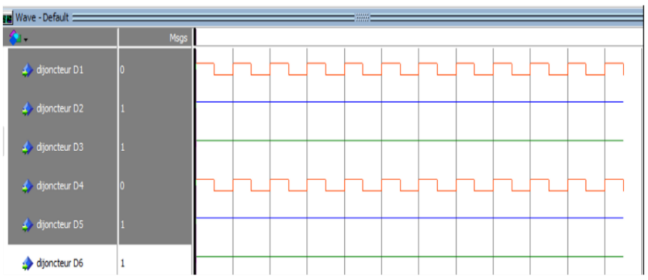
Figure 8 below illustrates the input signals configured to simulate a fault on phase A for ten-time units. In this case, the signals d1 and d4 switch to the low state (0), indicating that an incident has occurred in phase A and that circuit breakers D1 and D4 have automatically isolated this phase. On the other hand, the input signals d2, d3, d5, and d6 remain in the high state (1), meaning that phases B and C are operating normally, with d25 = d36 = 1 and d14 = 0. At the end of the simulation, the output signals S1 to S9 corresponding to the states of the reactances, as well as the indicators L1, L2, L3, and the alarm A, which provide real-time information on the conditions for phases A, B, and C of the line, are shown in Figures 9 and 10.

```
D1 <= '0' after 0 ns, '1' after 10 ns, '1' after 20 ns, '1' after 30 ns,
    '0' after 40 ns, '1' after 50 ns, '1' after 60 ns, '1' after 70 ns,
    '0' after 80 ns, '1' after 90 ns, '1' after 100 ns, '1' after 110 ns,
    '0' after 120 ns, '1' after 130 ns, '1' after 140 ns, '1' after 150 ns,
    '0' after 160 ns, '1' after 170 ns, '1' after 180 ns, '1' after 190 ns,
    '0' after 200 ns, '1' after 210 ns, '1' after 220 ns, '1' after 230 ns;
```

(a)

```
D4 <= '0' after 0 ns, '1' after 10 ns, '1' after 20 ns, '1' after 30 ns,
    '0' after 40 ns, '1' after 50 ns, '1' after 60 ns, '1' after 70 ns,
    '0' after 80 ns, '1' after 90 ns, '1' after 100 ns, '1' after 110 ns,
    '0' after 120 ns, '1' after 130 ns, '1' after 140 ns, '1' after 150 ns,
    '0' after 160 ns, '1' after 170 ns, '1' after 180 ns, '1' after 190 ns,
    '0' after 200 ns, '1' after 210 ns, '1' after 220 ns, '1' after 230 ns;
```

(b)



(c)

Fig. 8(a-c): Signal set with fault on phase A

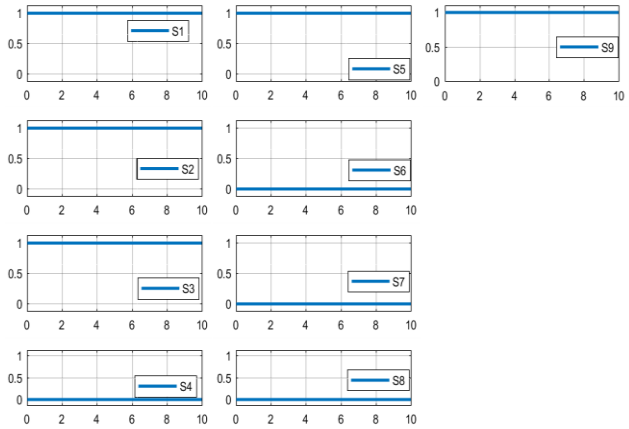


Fig. 9 Reactance states with phase A fault

Fig. 10 LED Status and audible alarm

Figure 9 above illustrates the states of reactances S1 to S9 in the presence of a fault in phase A. When an anomaly occurs on this phase for ten-time units, circuit breakers D1 and D4 open, automatically isolating the faulty line. In response, the FPGA activates reactances S1, S2, S3, S5, and S9 (ON position) to redirect the power flow initially affected towards phases B and C, which remain functional on the source side, and to maintain a three-phase supply on the receiver side. At the same time, reactances deemed unnecessary in this context, namely S4, S6, S7, and S8, are deactivated (OFF position). Figure 10 shows the states of indicators L1, L2, and L3, as well as alarm A, which reflect the operational status of phases A, B, and C. It can be seen that L1 and A are in the high state (1), while L2 and L3 remain at 0. This means that only the L1 indicator and the audible alarm are activated to signal a fault in phase A. Consequently, an alert message such as "Alert: Fault on phase A, d1d4 = 0" will be automatically sent to the designated operators, either by SMS or email, to inform them in real time of the incident on phase A.

4.3. Simulation of the FPGA with Simultaneous Two-Phase Faults Affecting Phases B and C

Figure 11 shows the input signals configured for a simultaneous biphasic fault on phases B and C over a period of 4-to-6-time units. During this disturbance phase, input signals d1 and d4 remain at state 1, meaning that d14 = 1, indicating that phase A is unaffected and circuit breakers D1 and D4 remain in operation. Meanwhile, input signals d2, d3, d5, and d6 are at state 0, indicating that phases B and C are affected. The results of this simulation are illustrated in Figures 12 and 13.

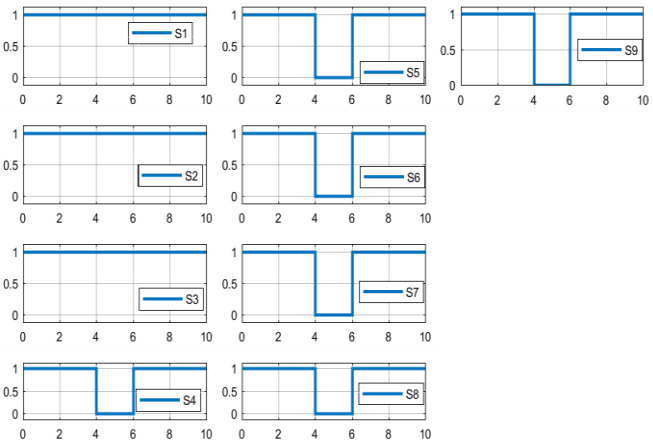


Fig. 11 Parameterised signal with simultaneous two-phase faults affecting phases B and C

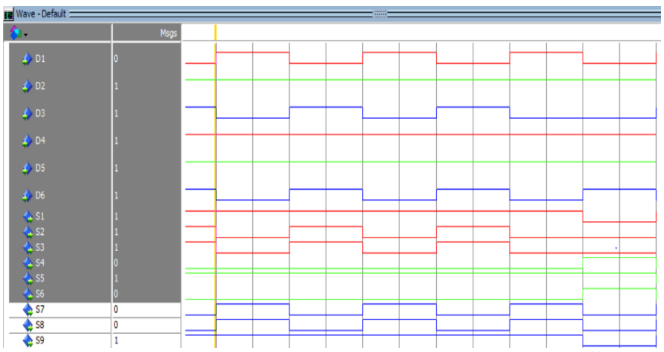


Fig. 12 Reactance states with simultaneous two-phase error affecting the B and C phases

Figure 11 shows the states of reactances S1, S2, S3, S4, S5, S6, S7, S8, and S9 when a fault simultaneously affects phases B and C. During a time interval of 4-to-6-time units, circuit breakers D2, D5, and D3, D6 are triggered, disconnecting the affected phases B and C. The FPGA automatically adjusts reactances S1, S2, and S3 to the ON

position during the fault period to redirect energy flows from the affected phases to phase A, which remains unaffected on the source side, and redistributes this energy across all three phases on the receiver side. Reactances S4, S5, S6, S7, S8, and S9, deemed unnecessary, are set to the OFF position.

Fig. 13 LED Status and audible alarm

Figure 13 illustrates the states of indicators L1, L2, L3, and alarm A, reflecting the condition of phases A, B, and C, along with L1 = 0 and L2 = L3 = A = 1, this indicates that indicators L2, L3, and the alarm are activated to signal the fault affecting phases B and C. Consequently, a message such as "Phase B fault alert, d2d5 = 0; Phase C fault alert, d3d6 = 0" will be sent to the designated operators, either via mobile phone or email, to inform them in real-time of the failure on phases B and C.

4.4. Simulation with Non-Simultaneous Two-Phase Faults Impacting Phases A and B

Figure 14 shows the parameterised input signals with non-simultaneous two-phase error affecting lines A and B over an interval of 2 to 8 time units and 7 to 8 time units. During a period of 2 to 8 time units, the contingency has affected phase A, and input signals d1 and d4 are in state 0, i.e. d14 = 0, proving that this phase is affected and circuit-breakers D1 and D4 open to de-energise it. As for phase B, it is affected over a period of 7 to 8 time units, which causes circuit-breakers D2 and D5 to open. Input signals d2, d5, d1, and d4 are at state 0, which means that phases A and B are affected. The results of the simulation are displayed in Figures 14 and 15.

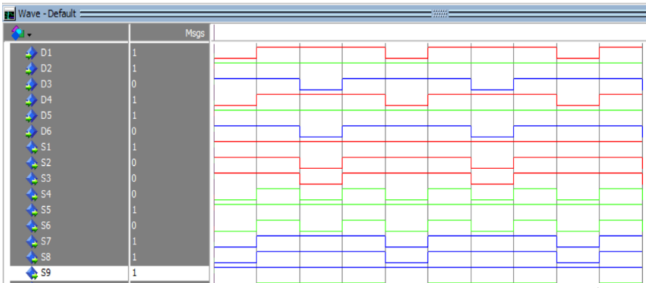


Fig. 14 Parameterised signal with non-simultaneous two-phase faults affecting phases A and B

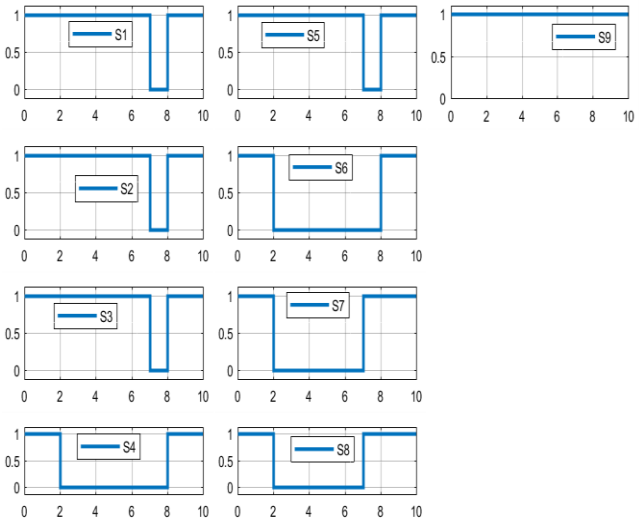


Fig. 15 Reactor states with non-simultaneous two-phase faults affecting phases A and B

Figure 15 illustrates the states of reactances S1 to S9 in response to faults affecting phases A and B successively. When these biphasic faults occur, with a disturbance on phase A between 2- and 8-time units and on phase B between 7- and 8-time units, the switches D1 and D4 for phase A and D2 and D5 (for phase B) trip to isolate these phases during the anomalies.

The FPGA automatically adjusts the reactances accordingly: S1, S2, S3, and S5 are activated from 2 to 7 time units; S7 and S8 are activated between 7- and 8 time units; and S9 remains active throughout the disturbance. These adjustments redirect energy flows from the faulty phases to phase C, which remains functional on the source side while ensuring balanced energy distribution across all three phases on the receiver side. Reactances S4 and S6, deemed unnecessary, are deactivated (set to OFF).

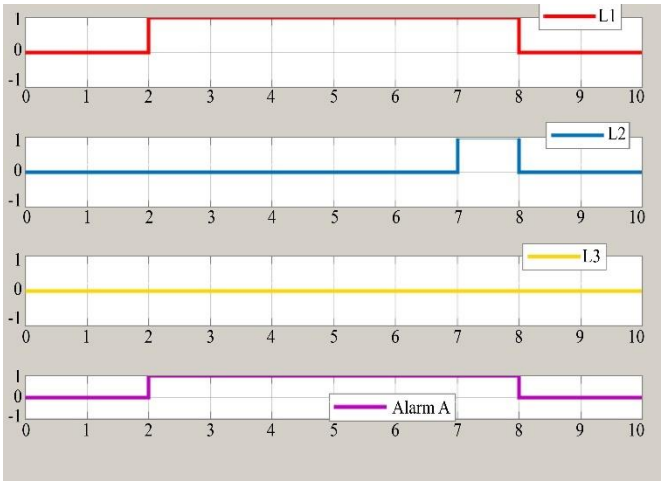


Fig. 16 LED and alarm status

Figure 16 illustrates the states of indicators L1, L2, L3, and alarm A, reflecting the conditions of phases A, B, and C. During the contingency period, L1 = 1, L2 = 1, and A = 1, while L3 remains at 0. This indicates that indicators L1, L2, and the alarm are active to signal faults in phases A and B. A notification stating, "Phase A fault alert, d1d4 = 0; Phase B fault alert, d2d5 = 0," will be dispatched to the assigned operators via mobile phone or email, providing real-time updates on the faults affecting phases A and B.

4.5. Discussion

In this article, we carry out a comparative study of our results obtained with other works in the literature to highlight the points of similarity and the innovative points of our work. The problem of fault management in an electrical power transmission network has been addressed by several authors. Contingency management criteria, evolutionary factors, and technological resources allow us to distinguish between authors and highlight our contribution to these works. Indeed, regarding the criterion of automatic contingency management, our work allows for the regulation of single-phase, simultaneous and non-simultaneous two-phase, and three-phase faults on the power transmission line. In addition, this can be supplemented by the stabilization of power flow between two sub-networks, the attenuation of short-circuit current, regulating the active and reactive power under pre-fault and after the fault has occurred, and a 100% compensation time of the transmitted power.

Regarding the criterion of scalability and technological resources (FPGA card, VHDL language), our solution uses programmable logic, which means that, in case of modification of the network parameters, it is sufficient to declare the parameters of the new line in the source code of the program. The update is done, unlike wired logic, which requires tedious work and a representation of new truth tables, algebraic equations, logic diagrams, etc [13, 15, 18]. The results obtained in our work are of major importance, namely on the criterion of flexibility and customization. It ensures a rapid configuration because FPGAs allow for the dynamic reconfiguration of the hardware, which facilitates adaptation to network evolutions and new standards and customization in the sense that FPGAs allow for the design of tailored solutions adapted to each network's specific needs. Regarding the criterion of performance and response time, FPGAs offer very high execution speeds, which is crucial for protection applications where response time is critical. FPGAs allow for the execution of several operations in parallel, which improves the overall performance of the system.

Regarding the criterion of robustness and reliability, FPGAs can quickly and accurately detect different types of faults (short circuit, overcurrent, etc.), thus allowing the isolation of the faulty area and limiting damage. The processing speed of FPGAs reduces the response time to faults, which limits network disturbances. FPGAs can be designed with redundancy mechanisms to improve system reliability. Regarding the integration and energy consumption criterion, FPGAs can be integrated into compact and modular systems, which facilitates their installation in electrical substations. Modern FPGAs are becoming increasingly energy-efficient, which reduces operating costs. Finally, regarding the cost criterion, although initial acquisition costs may be higher than traditional solutions, FPGAs can reduce maintenance and operating costs over the long term thanks to their flexibility and reliability. FPGA boards offer a powerful and flexible solution for automatically regulating faults in electrical power transmission networks. Their high performance, flexibility, and robustness make them an increasingly popular choice for critical applications.

Table 4. Comparison of work with other authors

Authors / Criteria		Our proposals	Mougnol Assala [7]	Essama et al[17]	KOM Charles [19]	Mandeng Jean Jacques [13]
Structure		☑	☒	☒	☒	☒
flexibility		☑	☒	☒	☒	☒
Complexibility		☑	☒	☒	☒	☒
Contingency category management	Single-phase fault regulation	☑	☑	☑	☑	☑
	Biphasic fault regulation	☑	☑	☑	☑	☑
	Three-phase fault regulation and more	☑	☒	☒	☒	☒
	Simultaneous biphasic fault regulation	☑	☑	☒	☒	☑
	Non-simultaneous biphasic fault regulation	☑	☑	☒	☒	☑
	Use programmed logic	☑	☒	☒	☒	☒

	Use wired logic	☒	☑	☒	☑	☑
	Power flow stabilization between two subnetworks	☑	☑	☑	☑	☑
	Short-circuit current limitation	☑	☑	☑	☑	☑
	Control of active and reactive power during pre-contingency as well as after contingency scenarios	☑	☑	☑	☑	☑
	Compensation rate of transmitted power (100%)	☑	☒	☑	☑	☑
Scalability	Contingency management automation (Programmed logic)	☑	☑	☒		☒
	Wired logic	☒	☑	☒	☑	☑
Technological resources	IPC-Source and load	☑	☑	☑	☑	☑
	VHDL	☑	☒	☒	☒	☒
	Matlab	☑	☑	☑	☑	☑
	FPGA board	☑	☒	☒	☒	☒
Adaptability	Quick configuration	☑	☒	☒	☒	☒
	Complex algorithms	☑	☒	☒	☒	☒
	Customization	☑	☒	☒	☒	☒
Performance and latency	Processing speed	☑	☒	☒	☒	☒
	Parallelism	☑	☒	☒	☒	☒
Durability and Reliability	Fault detection	☑	☒	☒	☒	☒
	Quick response time and fault tolerance	☑	☒	☒	☒	☒
Integration and compactness	Integration	☑	☒	☒	☒	☒
	Power consumption	☑	☒	☒	☒	☒
Costs	Total cost of acquisition	☑	☒	☒	☒	☒

Note: Legend: The symbol ☑ indicates the presence of a criterion. The symbol ☒, on the other hand, indicates the absence of a criterion.

5. Conclusion

The primary aim of this article was to demonstrate how this automated dual IPC system improves the management of electric power compensation in a transmission network, particularly in response to challenges posed by short circuits or phase losses. To achieve this, we began by analysing the causes of failures in electrical networks, followed by the presentation of FACTS devices, which serve a crucial function in enhancing the transient stability of systems.

This analysis allowed us to provide an overview of compensators, both traditional and advanced, highlighting their advantages and limitations. The study also emphasized the importance of system automation in production chains, notably through the review of the access control list for a system incorporating two IPCs 240. Based on this, we developed the logical model of the controller, which was then tested through simulations. The simulations were carried out on an FPGA board, simulating various scenarios: no faults on phases A, B, and C; a one-phase fault affecting phase A; simultaneous dual-phase faults occurring on phases B and C; and finally, non-simultaneous dual-phase error on phases A and B. We also conducted a comparative study with the manual management of reactances to demonstrate the advantages of using FPGA to manage faults and enhance the flexibility of power transmission.

Despite some unforeseen issues, such as persistent single-phase or dual-phase faults, the suggested automated system manages to maintain a balance in the three-phase power supply to the load, providing part of the nominal power on the receiver side. Thanks to the FPGA board, remote operators can receive real-time fault notifications via SMS or email, specifying the faulty phases. The real-time results showed that the system is effective and that using two RPIs is essential to ensure the stability of electric power transmission. In the future, an interphase power regulator controlled by fuzzy logic is being considered to address overload issues during peak hours.

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