SSRG International Journal of Electronics and Communication Engineering
ISSN: 2348-8549/ https://doi.org/10.14445/23488549/IJECE-V12I8P121

Volume 12 Issue 8, 234-243, August 2025
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Original Article

Halo-Implanted Partially Depleted Silicon-on-Insulator MOSFET with Optimized Buried Oxide Substrate for Short Channel Effects Mitigation

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Received: 11 June 2025 Revised: 12 July 2025 Accepted: 13 August 2025 Published: 30 August 2025

Abstract *- In traditional bulk MOSFETs, the MOSFET dimensions shrink below the 90 nm barrier, and Short-Channel Effects (SCE) emerge, which weaken gate control. These include threshold voltage roll-off, increased leakage currents, and Drain-Induced Barrier Lowering (DIBL). While offering better electrostatic control, Fully Depleted Silicon-on-Insulator MOSFETs (FD-SOI) and Partially Depleted Silicon-on-Insulator (PD-SOI) MOSFETs still have inherent drawbacks in ultra-scaled nodes. Since FD-SOI MOSFET needs silicon thickness to be controlled precisely, along with exact doping, it is harder and more expensive to manufacture. Although it reduces some SCEs and increases gate-to-body coupling, it has some leakage current and electrostatic limitations. To overcome these limitations, a proposed PD-SOI MOSFET design uses source-side halo implantation with a tunnel diode within the Buried Oxide (BOX) layer. Halo implantation reduces channel electrostatics by the depletion region effects originating from both sides of the source and drain implants, while an integrated tunnel diode provides another current path to balance leakage currents and improve electrostatic control. The proposed device combines these two approaches to suppress SCE and further improve the performance of the device, with the potential for higher SCE suppression as well as higher performance of the devices in next-generation MOSFETs. The simulated results achieve the low threshold voltage and low DIBL, reducing the SCE in the proposed device.*

Keywords *- Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), Short-Channel Effects (SCE), Fully Depleted Silicon-On-Insulator (FD-SOI) MOSFET, Partially Depleted Silicon-On-Insulator (PD-SOI) MOSFET, Buried Oxide (BOX) layer.*

1. Introduction

For low-power, high-performance applications, the SOI MOSFET technology is currently believed to be a great solution to the scaling problems of the bulk equivalent. [1]. A MOSFET's high efficiency and low power consumption in electronic signal amplification and switching make it a crucial component of many electronic systems and devices. The Source, drain, gate and body are the parts of a MOSFET. Technology development, which leads to more functions and improved performance, has been fueled by the achievement of scaling MOSFETs [2]. On the other hand, rapid technological growth causes SCE and might result in reliability problems. SCEs are explained by the restriction placed on electron drift in a channel and the shift in a device's threshold voltage brought by the channel's decreased length [3]. Surface scattering, impact ionization, Ioff, Ion, velocity saturation, DIBL, Subthreshold Slope (SS), and hot carrier effect are all included in the SCEs [4]. SOI technology can reduce SCEs by placing an insulating layer known as a BOX layer just beneath the transistor's channel. Also, the SOI MOSFET enables the device to function at greater speeds and tolerate higher voltages and temperatures by reducing the parasitic capacitance impact [5].

Researchers with different architectures have been interested in investigating the shrinking of the SOI MOSFET. The front-gate-to-channel controllability and SCEs have been further enhanced by the development of ultra-thin body and BOX (UtBB) on SOI MOSFETs [6]. Additionally, the majority of the MOSFET's bulk volume merely produces parasitic effects, whereas the top layer is helpful for transporting electrons [7]. When compared to traditional bulk MOSFETs, the SOI MOSFET offers a higher packing density. The lack of wells and the presence of a BOX layer are the causes of the decrease in latch-up and parasitic drain/source to substrate capacitance. Better speed and less power dissipation are the outcomes of the SOI device. In comparison to bulk MOSFETs, a steep subthreshold slope and lower leakage

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current are also attained, improving device performance [8]. Mostly, the SOI MOSFET offers low junction capacitance, low leakage current, enhanced sub-threshold characteristics, and better gate control over the device.

There are two types of SOI MOSFETs, for instance, devices that are PD and devices that are FD [9]. The device is known as PD-SOI when the silicon layer is thicker than the depletion width because the channel is partially depleted during normal operation. Conversely, FD-SOI is the channel region beneath the inverting layer, and the silicon film is thinner than the depletion width. However, like other physical and semi-empirical models, its modelling procedure requires a lot of technological data and the extraction of rather complex parameters [10]. PD-SOI transistors, unlike FD-SOI transistors, possess a nonlinear drain current model and a gate capacitance model. [11]. While the drain current model considers the current-induced body effect, self-heating effect, and channel length modulation effect, the designed capacitance enhances modeling precision in the triode region using charge conservation. [12].

The halo implantation is used by channel engineering [13]. The high leakage current and SCEs that may deteriorate the device output characteristics when the dimensions are deeply scaled down into the deep-submicrometer regime are mitigated by traditional drain engineering, another widely used technique. Halo pocket implants have already been studied and modelled for their effects on electrical properties such as threshold voltage, Drain-Induced Threshold Shift (DITS), capacitance, current mismatch, output resistance, and transconductance [14]. Usually, sub-threshold slope and SCEs are achieved using halo implants on the source side and homogenous doping on the drain side. Furthermore, a zone of increased doping concentration will be created next to the Source using the Source-side halo implant [15]. This helps to lessen the electric field that results in SCEs such as threshold voltage roll-off and DIBL. So, in this research, the SCE can be mitigated by combining both source-side halo and tunnel diode insertion in the BOX of PD-SOI MOSFET. This work mainly aims to reduce the short channel effects of SOI MOSFET using Halo Implantation and optimized BOX Substrate. The main contributions of this research work are listed as follows:

- To mitigate SCEs of PD-SOI MOSFET by fitting a source-side halo implantation.
- To reduce the SCEs of PD-SOI MOSFET by inserting the tunnel diode in the BOX, which is made up of N+ and P+ doping areas.
- To analyze the SCE of the proposed model using Threshold voltage roll-off, transfer characteristic simulation and DIBL.
    - The next section of the research article is structured as follows: A review of recent research that is important to the proposed device is given in Section 2. The specific ideas and principles of the suggested design are explained in detail under Section 3. Section 4 presents a study of the simulation result research and improvement. Using various performance measures. Finally, Section 5 concludes the paper by summarizing the findings and offering recommendations for future research.

There are a number of traditional MOSFET technologies, the dimensions of the MOSFETs are large, which causes high SCE and increases the leakage current, and some more limitations are the Large-scale circuit simulation speed, impacted by increased computational complexity resulting from integrating components of the BSIM-SOI models. In RNAFET, the small channels raise the possibility of direct source-to-drain tunnelling, resulting in leakage currents and affecting detection accuracy. The metal Source/Drain contacts are essential for preventing ion penetration into the BOX layer. Then, the PDSOI MOSFET has increased fabrication complexity and too much tunnelling current, which causes increased SCE. Even though PD-SOI MOSFETs have many advantages over bulk MOSFETs, including better electrostatic control and fewer substrate effects, many issues still require further investigation.

The PD-SOI MOSFETs have numerous advantages over bulk MOSFETs, such as improved electrostatic control and fewer substrate effects. However, there are a number of issues in the PD-SOI MOSFET. To overcome these, to integrate both source-side halo and a tunnel diode insertion in the BOX of PD-SOI MOSFET for SCE mitigation

2. Literature Review

Chetan Kumar Dabhi et al. [16] introduced a charge-symmetric compact model of PDSOI technology. The industry-standard Berkeley Short-Channel IGFET Model (BSIM)-BULK platform is a foundation for the device core charge computations, which fully use its symmetry, speed, and durability. Moreover, the industry-standard legacy BSIM-SOI model is used to integrate the SOI-specific. The model may faithfully represent a Floating Body Effect (FBE), which is essential to PDSOI technology. For BC PDSOI devices, the linear and nonlinear Body Contact (BC) models have also been used. For both DC and small-signal simulations, a model passes source-drain symmetry tests, producing outstanding harmonic balancing properties that are essential for radio frequency applications. The industry's most recent PDSOI device data is used to validate the model.

An ORF1ab RNA gene detection Ribonucleic Acid (RNA) Field-Effect Transistor (RNAFET) using a planar FDSOI p-channel Schottky Barrier (SB) MOSFET was recently reported by Haihua Wang et al. [17]. A high-K hafnium dioxide/gold nanoparticle/FDSOI SB-PMOSFET biosensor with ultrahigh voltage sensitivity is shown. The

built-in back gate measures it without the use of a liquid-gate electrode. A good back-gate RNAFET biosensor is necessary to achieve high voltage sensitivity, and the very thin top-Si channel of FDSOI requires metal source/drain (S/D) contact instead of ion implantation doping to prevent ion penetration in the BOX layer. Without the need for extra amplifying circuitry, the back-gate measurement operation can greatly increase the detection sensitivity by amplifying the voltage readout response through the double-gate device's strong capacitive coupling effect. The hybridization of the complementary probe Deoxyribonucleic Acid (DNA) and the charged RNA analyte can change the threshold voltage of the RNAFET biosensor. ORF1ab gene detection demonstrates that the back-gate Vth sensitivity can reach 1.765 V/log[RNA], which is approximately 100 times better than a traditional liquid-gate Si MOSFET DNA biosensor.

Mohammad and Zeinab describe a new modified construction based on PDSOI MOSFETs with integrated tunnelling diodes inside the BOX [18]. The Electric field will shift, and a new path for an accumulation of holes to be evacuated will be created. Therefore, these integrated diodes effectively control the FBE, a highly detrimental phenomenon. N+ and P+ doping areas will be inserted into the BOX to create the diodes. These additions will create lateral and vertical holes for current to tunnel via the channel region.

Additionally, by adding a tunnelling diode inside the BOX, the suggested device's effective thermal conduction rises, thus reducing the self-heating effect. The suggested framework had a strong potential to improve its figure of merit by changing two parameters in the cases of reduced self-healing effect and FBE. The parameters are subthreshold Swing, leakage current, ION/IOFF, DIBL, power gains, drain-source conductance, cut-off frequency, and minimum noise figure. An ATLAS tool from the SILVACO family has been used to simulate the device and compare it to the traditional structure. The advantages of the suggested device over the standard equipment were evident in every result that was achieved.

Haihua Wang et al. [19] introduced a novel sensing structure based on Au nanoparticles/HfO2/FD SOI (AuNPs/HfO2/FDSOI) MOSFET. For a quick and ultrasensitive detection of the coronavirus disease 2019 (COVID-19) ORF1ab gene, the electrostatic enrichment (ESE) is used. When a testing liquid analyte comes into indirect contact with a top-Si layer, a Back-Gate (BG) bias can create a necessary electric field to facilitate an ESE process. It has been discovered that ORF1ab genes may efficiently and quickly accumulate near the HfO2 surface through the ESE process, which can drastically alter the MOSFET threshold voltage. Even in a high ionic-strength solution, a suggested MOSFET effectively exhibits the detection of the zeptomole (zM) COVID-19 ORF1ab gene with an ultralow detection limit down to 67 zM (~0.04 copy) during the test duration of less than 15 minutes. Additionally, the TCAD simulation confirms the quantitative dependency of variation on COVID-19 ORF1ab gene concentration, which ranges from 200 zM to 100 femtomoles.

Zhanpeng Yan et al. [20] have examined the deterioration mechanism of the Radio Frequency (RF) performance of 22 nm FD-SOI nMOSFETs at various levels of Total ionizing Dose (TID). The maximum oscillation frequency (fmax) and cut-off frequency (fT), RF figures of merit, exhibit notable degradation of roughly 6.8% and 14.1%, respectively. It has been discussed how the small-signal parameters, capacitance (C_{gg}), reflection coefficient, output conductance (g_{ds}), and transconductance (g_m) vary at various TID levels. The vertical channel field is increased by gate oxide because of its TID-induced trapped charges and BOX, resulting in a more intricate deterioration of small-signal characteristics throughout a broad frequency range.

From the above article, there are a number of traditional MOSFET technologies. The dimensions of the MOSFET are large, which causes high SCE and increases the leakage current, and some other limitations are the Large-scale circuit simulation speed, impacted by increased computational complexity resulting from integrating components of the BSIM-SOI [16] models. In RNAFET [17], the small channels raise the possibility of direct source-to-drain tunnelling, which can result in leakage currents and affect detection accuracy; the metal Source/Drain contacts are essential for preventing ion penetration into the BOX layer. Then, the PDSOI MOSFET [18] has increased fabrication complexity, and there is too much tunnelling current, which causes increased SCE. Even though PD-SOI MOSFETs have many advantages over bulk MOSFETs, including better electrostatic control and fewer substrate effects, many issues still require further research and improvement. The PD-SOI MOSFETs have numerous advantages over bulk MOSFETs, such as improved electrostatic control and fewer substrate effects. However, there are a number of issues in the PD-SOI MOSFET. Both source-side halo and a tunnel diode insertion in the BOX of PD-SOI MOSFET for SCE mitigation must be integrated to overcome these.

2.1. Problem Statement and Motivation

Thin-film thickness, BOX thickness, and DIBL all affect SCE in SOI MOSFETs. When device dimensions are reduced below the 90 nm limit, SCEs and leakage currents increase, but the effect of gate control on the channel is reduced. SCE and electrical properties differ between FD and PD-SOI MOSFETs. Compared to conventional PD-SOI MOSFETs, FD-SOI MOSFETs have a lower leakage current. However, more exact control over doping levels and silicon layer thicknesses is necessary to accomplish full depletion of the silicon channel, where all carriers are removed from the channel region. This adds more phases to the process, like etching, ion implantation, and thin-film deposition, which

might raise manufacturing costs. The PD-SOI MOSFET is a type of SOI MOSFET that was developed to reduce some of the SCEs experienced by traditional bulk MOSFETs as their channel length decreases. It can enhance gate-to-body coupling, body effect, and junction area capacitance, all of which increase the driving current during switching.

Even though PD-SOI MOSFETs have many advantages over bulk MOSFETs, including better electrostatic control and fewer substrate effects, many issues still require further research and improvement. As MOSFETs continue to shrink in size (to nodes smaller than 10 nm), the partially depleted arrangement becomes less effective. SCEs are more common in smaller devices because the depletion zone from the Source and drain begins to overlap more. The semiconductor industry makes extensive use of halo pocket-implanted devices to reduce the SCE. The efficacy in ultra-scaled devices is limited by the halo regions, which can still lead to elevated leakage currents and inadequate electrostatic regulation of the channel. However, the integrated tunnelling diodes in BOX can help enhance electrostatic control and lower SCE by offering an extra current path that can help with some of the leakage current problems. Tunnel diodes may find it difficult to maintain a constant threshold voltage at small nodes under certain conditions. Both built-in tunneling diodes and halo pocket implantation have their own drawbacks when it comes to controlling short-channel effects and enhancing device performance at smaller technology nodes. A more comprehensive solution to controlling short-channel effects may be possible by combining the two approaches. These points motivate us to integrate both source-side halo and a tunnel diode insertion in the BOX of PD-SOI MOSFET for SCE mitigation.

3. Background of SOI MOSFET

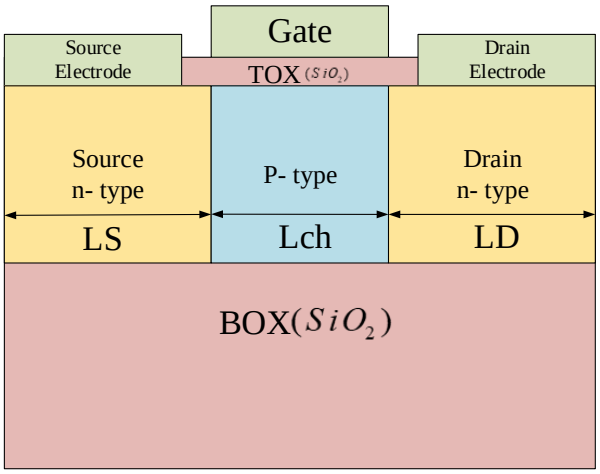

Fig. 1 Model device of conventional SOI MOSFET

The above Figure 1 shows the Conventional SOI (C-SOI) MOSFET. It has already passed the 45 nm transistor fabrication limit. As silicon reaches its physical and electrical limits, creating a functional transistor becomes increasingly challenging and complex. The main problem is to create a transistor with a nominal threshold voltage (VTH), low gate leakage current (IOFF), and low DIBL. SOI MOSFETs minimize the SCE by inserting BOX in the silicon substrate. FD- SOI MOSFET and PD-SOI MOSFET are two types of SOI MOSFET.

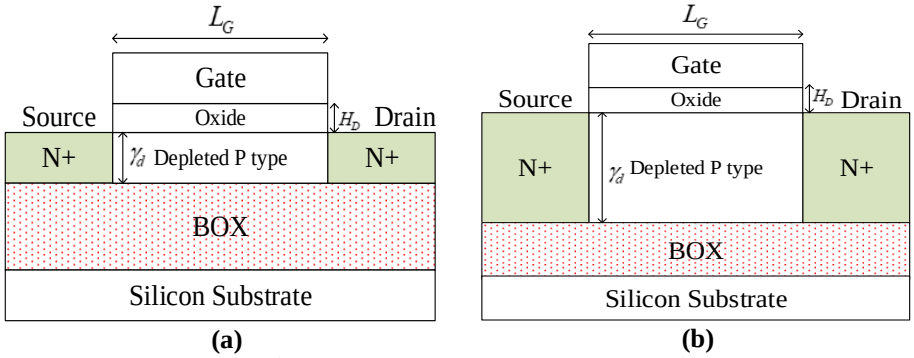

Fig. 2 (a) Model device of FD- SOI MOSFET, and (b) Model device of PD- SOI MOSFET.

An FD-SOI MOSFET is a type of SOI MOSFET in which the silicon layer is thin enough to become fully depleted of charge carriers during its operation. Such a design improves electrostatic control over a channel and reduces SCE, thus improving a transistor's performance. PD-SOI MOSFETs are often preferred over FD-SOI MOSFETs because they are simpler to manufacture and design, as they can utilize design features from bulk silicon devices with only modest changes.

In a PD-SOI MOSFET, the silicon layer is depleted to some extent on top of an insulator layer. In PD-SOI devices, the silicon film thickness is rather large, so the depletion region extends only part of the silicon. PD-SOI MOSFETs help reduce SCE by minimizing charge-sharing between the drain and Source, leading to better control of the channel and improved device performance. Therefore, PD-SOI MOSFETs show properties similar to bulk MOSFETs with some advantages. They have lesser parasitic capacitance and better performance as well.

4. Proposed Device Model and Numerical Procedure

A SOI technology is presented as a dependable and effective way to reduce SCE in VLSI circuits because of its superior insulation and low parasitic capacitances. FD-SOI and PD-SOI MOSFETs are the two types of SOI-MOSFETs. The PD-SOI MOSFETs are simpler and less expensive to build than the SOI MOSFETs.

This research introduces an improved structure for PD-SOI MOSFETs for short-channel effects mitigation. This model consists of a Top Silicon Layer for conducting current and operating as the active region, while the gate electrode regulates the channel's conductivity. Also, current carriers can be provided and collected using Source and Drain. BOX is used to insulate the silicon channel from the underlying substrate. The best location to add SiGe is in the channel region (between the Source and drain) since this would immediately affect carrier mobility in the channel and enhance device performance. In addition to improving device performance, this increases current driving capability and lessens the impact of short-channel effects.

In addition, the Source-side halo implant is used to create a region with a higher doping concentration near the Source, which helps reduce the electric field that causes SCE effects like DIBL and threshold voltage roll-off. Also, the BOX substrate optimized for the carrier distribution correction by employing a tunnel diode at the bottom of the Source and the channel regions. In order to create a diode, N+ and P+ doping areas are inserted into the BOX. This provides lateral and vertical holes for current to tunnel via the channel region. The integration of both source-side halo implantation and the insertion of a tunnel diode at the BOX in a PD-SOI MOSFET can help mitigate SCEs efficiently. The effectiveness of this model was also analyzed by considering the halo doping in the source, drain, and both sides.

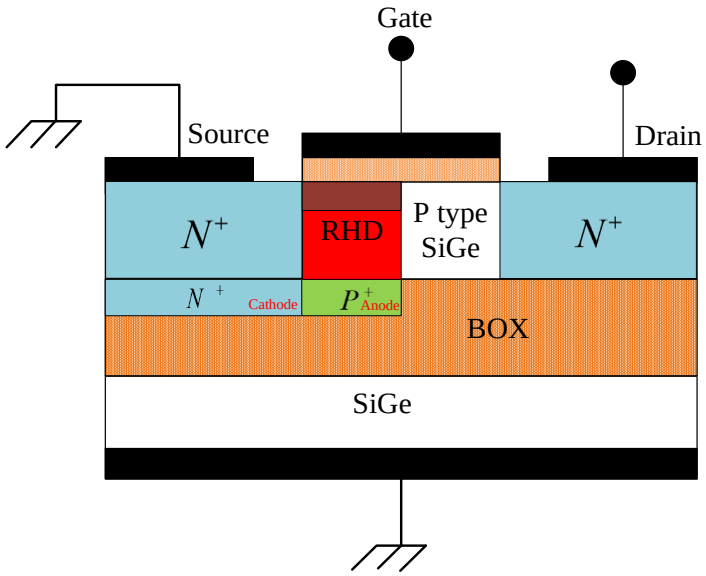

Fig. 3 Proposed device model of the PD- SOI MOSFET

Figure 3 represents the proposed device model of the PD-SOI MOSFET. The tunnel diode is implemented at the BOX layer, increasing the SCE and present under the Retrograde Halo Doping (RHD) and the Source region. SiGe reduces SCE by enabling more precise doping through substrate growth rather than conventional ion implantation. This approach allows for the placement of dopant at the Source edges with greater accuracy, which enhances halo formation and reduces off-state leakage.

In addition, the RHD is placed between the N+ cathode and the SiGe of PD-SOI MOSFET, which is used to minimize SCE, leakage current, and DIBL, and it degrades the device's performance. The RHD off current and sub-threshold slope are less than those of the C-SOI MOSFETs. Unlike uniform halo doping, where dopants are uniformly distributed across the area, RHD places more dopants near the bottom of the channel, thus reducing excessive leakage but not carrier mobility.

This selective doping technique increases the sub-threshold slope, decreases the off-state current, reduces hot carrier injection, and improves the transistor's overall dependability.

Boron (B) is a p-type dopant used for halo doping. Dopants are driven deeper into the substrate by higher-energy boron implantation, creating the retrograde profile that helps in the suppression of SCEs. By producing a shallow doping profile, lower-energy boron implantation enhances threshold voltage (Vt) control and lowers leakage currents.

The fundamental disadvantage of uniform halo doping is that it increases impurity dispersion, which reduces carrier mobility and leads to larger changes in threshold voltage. RHD is favored because it optimizes the trade-off between lowering leakage current and maintaining carrier mobility.

4.1. Analytical Model

Identify the equations for drain current relevant to scenarios I, II, and III. Examine Case I, where the device is bulk-Si-like regardless of the channel length V_{DS}. Therefore, the equation of bulk–Si is used. In case II, throughout the channel length, the device is bulk-Si-like $V_{DS} \le V_f$. But, over the early portion of the channel, the device is bulk-Si (V_{CS}: 0 toV_f). FD-SOI-like over the latter part (V_{CS}: $V_f$toV_{DS}). Therefore, the bulk-Si equation is used for$V_{DS} \le V_f$. And for$V_{DS} > V_f$the derivation is modified, yielding

$$I_D = \frac{W}{L}\frac{1}{\left(1+\frac{1}{L}\left[\frac{V_f}{E_c}+\frac{V_{DS}-V_f}{E_{cfd}}\right]\right)}\left\{\mu_{eff}\int_o^{V_f}(-Q_I)dV_{CS} + \mu_{fdeff}\int_{V_f}^{V_{DS}}(-Q_{Ifd})dV_{CS}\right\} \quad (1)$$

Whereμ_{fdeff}mobility is concerned, the channel charge per unit area and critical field are in the latter part of the channel.

$E_{cfd} = 2|V_{sat}|/\mu_{fdeff}$, where $V_{sat}$is the saturation velocity of channel electrons.

Similar definitions apply toμ_{eff}, $Q_I$andE_c: although these characteristics are related to the channel's earlier portion.

Case II is the same as Case I and has been replacedV_{fd}. The equations for Case III are comparable to those for Cases I and II; however, because Case III involves three scenarios rather than simply two, it is more complex than Cases I and II.

The generation current due to impact ionization at the drain,I_{gii}, is given by

$$I_{gii} = (m-1)I_{ch} \quad (2)$$

Where $I_{ch}$the channel current and multiplication factor are$m$.

$$(M-1) \cong \frac{X_i}{Y_i}(V_{DS}-V_{DSat})\,exp\left(\frac{-B_i\lambda}{V_{DS}-V_{DSat}}\right) \quad (3)$$

The electrical parameters X_i and Y_i the physical device parameters , such as doping density and gate oxide thickness, are in the model.

$$I_{gth} = A_{BD}C_oV_{DB} \quad (4)$$

Where the drain body voltage is V_{DB}, the electrical parameters are C_o and τ.

Then$A_{BD} = Wt_{si}$.

$$I_{BS} = A_{BS}J_s\left[exp\left(\frac{qV_{BS}}{n_1kT}\right)-1\right] + A_{BS}J_r\left[exp\left(\frac{qV_{BS}}{n_2kT}\right)-1\right] \quad (5)$$

Where the electrical parameters are J_s,J_r and$n$ A_{BS} is the area of the body/source diode.

4.2. Halo Doping

In short-channel devices, an electrostatic regulation of the channel is affected by source-side halo doping. In order to punch through and suppress DIBL, it modifies the electric field close to the Source. Usually, with a peak close to the Source, the halo doping profile follows an exponential or Gaussian distribution.

$$N_{halo}(x) = N_{halo,0\,exp}\left(-\frac{x}{\lambda_{halo}}\right) \quad (6)$$

Where $N_{halo,0}$is the peak doping concentration, and λ_{halo}what is the characteristic length scale of the halo doping?

5. Simulation Results

This section deeply explains the results obtained from the proposed device compared to the existing device. The proposed PD-SOI MOSFET was simulated using Silvaco TCAD. Also, the performance of a proposed design will be

validated in terms of DIBL, threshold Voltage Roll-Off and DC sweep simulation for different values of channel length.

Table 1. Comparison between the proposed device and the existing device

Device	DIBL	Sub-threshold Swing (mV/dec)
Proposed Device	200	123.52
PD-SOI MOSFET [18]	220	187
Conventional PD- SOI MOSFET	330	307

The DIBL of the proposed device is 9.09% better than the existing PD-SOI MOSFET model because the tunneling diode reduces the drain voltage-induced threshold voltage fluctuation. The proposed sub threshold swing is 51.39% better than the existing device of the PD-SOI-MOSFET.

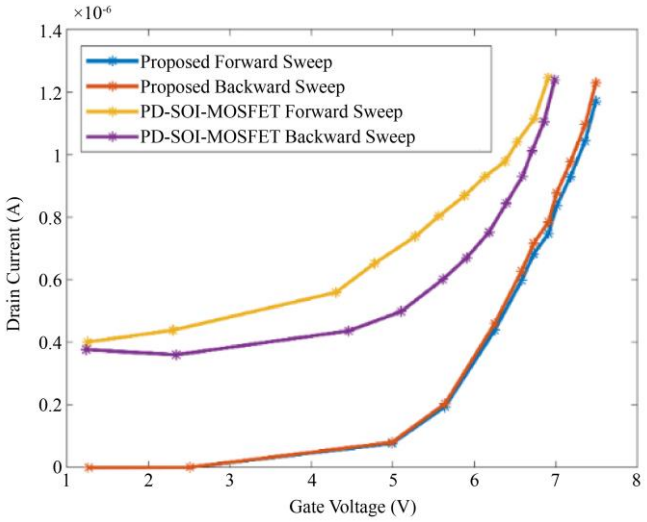

Fig. 4 Hysteresis effect illustration for the proposed and existing devices

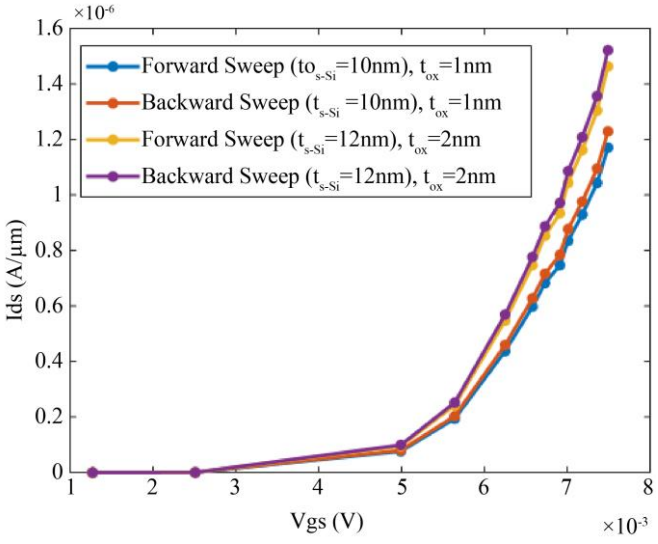

Fig. 5 The effects of t_{ox} and $t_{s\text{-}Si}$ on the proposed model's transfer characteristics and gm value

The above Figure 4 demonstrates this by applying a transient gate voltage to the gate electrode in both forward and backwards directions, extracting the drain current, and plotting it against the gate voltage. The FBE is dominant for the device; the drain currents are different for both directions, releasing the same gate voltage. The above Figure 5 shows the effects of hysteresis on the proposed and existing devices. The SOI technology isolates the active portion of the transistor from the substrate. This reduces the effects of hysteresis; as a result, the switching speed and system efficiency are increased.

Above Figure 5 illustrates how the s-Si and oxide (tox) thicknesses affect the g_m value and transfer properties of the suggested model. Higher g_m, enhanced transfer characteristics, and increased t_{ox} and ts-Si were caused by the proposed model's sub-threshold region decrement. The transfer characteristics and greater gm are also observed in the proposed model when the tox and s-Si are dropped.

The temperature of an atomic lattice in a semiconductor is known as the lattice temperature. When a transistor operates at high voltages or currents, energy is released as heat, which raises the lattice temperature. Then the lattice temperature should stay as constant and low as possible; high lattice temperatures may reduce device performance by decreasing mobility and increasing carrier scattering. Therefore, the proposed model has a low latency temperature, which is shown in Figure 6 below.

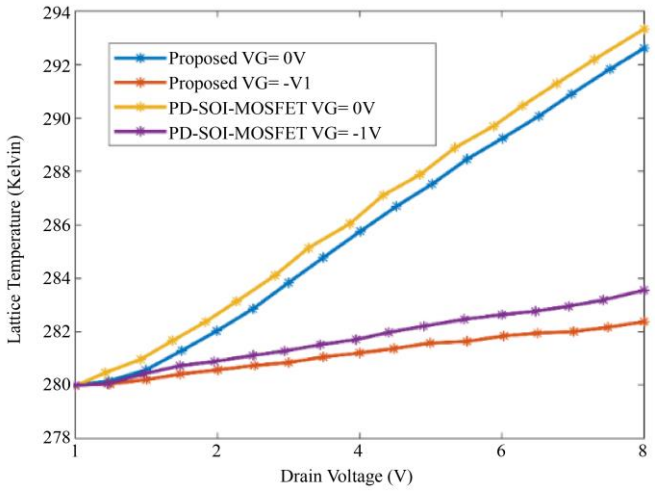

Fig. 6 Maximum lattice temperature versus drain voltage for the proposed model, the existing model of PD- SOI MOSFET

The above Figure 6 shows that the maximum lattice temperature versus drain voltage for the proposed model and the existing model of PD-SOI MOSFET. The proposed model is compared with the existing method; it achieves a low lattice temperature because it integrates a tunnel diode in the Buried Oxide (BOX) layer and uses source-side halo implantation. This combination reduces Short-Channel Effects (SCE) and

lowers the electric field intensity, which reduces the heat generated during transistor operation. Due to low lattice temperature, it reduced leakage currents, improved carrier mobility and enhanced reliability.

The proposed structure's Maximum Available Gain (MAG) and Unilateral Power Gain (UPG) are investigated and compared with the PD-SOI MOSFET. Figure 8 shows that the UPG and MAG values have been enhanced. The following are the f_{max} and UPG equations.

$$f\frac{fr}{2}\sqrt{\frac{R_{DS}}{R_G}}_{max} \quad (7)$$

$$UPG = \left(\frac{f_{max}}{f}()^2\right) \quad (8)$$

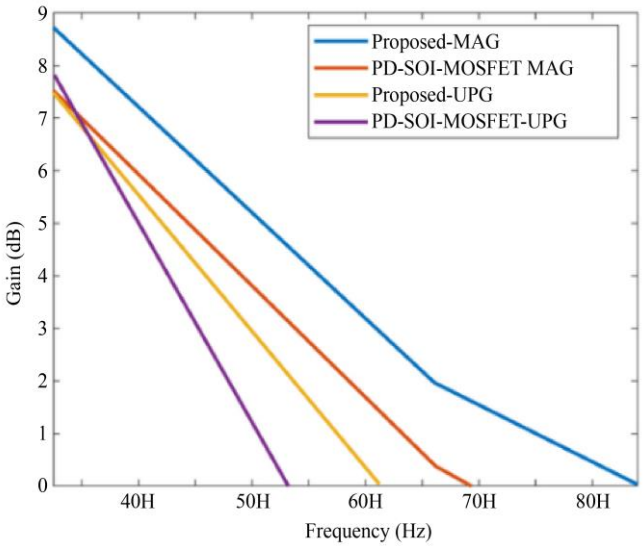

Fig. 7 UPG and MAG of proposed device and PD- SOI- MOSFET

Equation (8) shows that the proposed structure's UPG is enhanced when the cut-off frequency is increased in accordance with equation (7), which also causes the fmax to increase. Additionally, the proposed structures' improved conductivity results in a greater f_T and lower drain-source resistance, which raises the maximum oscillation frequency and enhances UPG.

In high-frequency applications, the minimum Noise Figure (NF_{min}) is a crucial component in the amplifier system. Then the noise is one of the elements that affects how well an amplifier performs. There are two types of noise in amplifiers: noise that the amplifier makes and noise that it receives at its input. An effective system is one in which the signal/noise ratio achieves the noise figure, and the noise produced by the amplifier itself is less than the noise from the input source. The NFmin for a device is obtained by the following equation,

$$NFgs\sqrt{\frac{R_S+R_G}{g_m}}_{min} \quad (9)$$

Where source resistance is R_S and gate resistance is R_G.

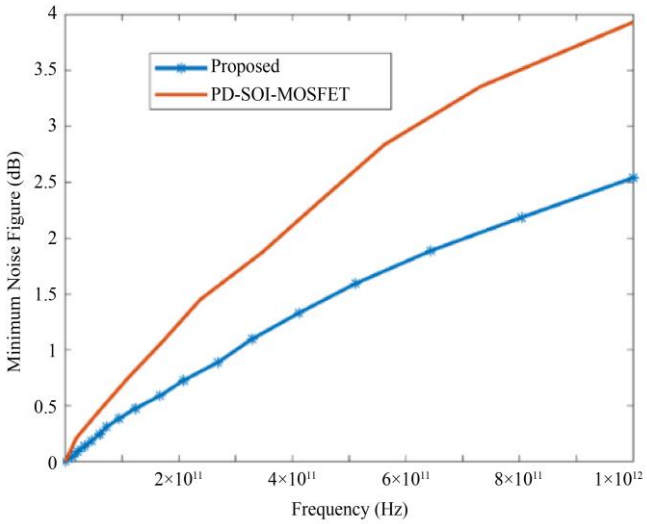

Fig. 8 Minimum noise figure (NF_{min}) as a function of frequency

The above Figure 8 shows that the NFmin versus frequency function of frequency. If the capacitance of a gate source decreases, the minimum noise figure also decreases. Minimum noise will be reduced due to the lower R_S and C_{GS}, so the proposed method produced less NFmin, which is desirable.

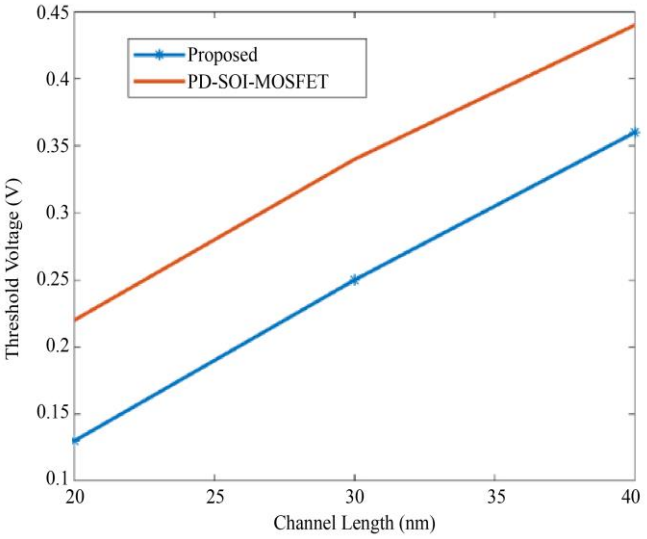

Fig. 9 Threshold voltage versus channel length for the Proposed and PD-SOI MOSFET.

The above Figure 9 shows a threshold voltage versus channel length for the proposed and PD SOI MOSFET, which is highly desirable. Another significant finding is that, regarding scaling concerns, the proposed device gives less

threshold voltage than PD-SOI MOSFET because of better gate control and reduced SCE and the Performance is improved by doping profile optimization and material improvements.

6. Conclusion

This research proposed an improved structure of PD-SOI MOSFET for reducing the short channel effects, and this model consists of a Top Silicon layer for conducting current and operating as the active region. The SiGe was located between the RHD and drain region and was used to produce a strain in the silicon channel to boost the performance and reduce the SCE in the proposed structure. In addition, the Source-side halo implant was used to create a region of higher doping concentration near the Source, which helps to reduce the electric field. Also, the carrier distribution correction is optimized by inserting the tunnel diode into the BOX layer, which helps to reduce the SCE effectively. However, the reduction of SCE decreases threshold voltage; this problem leads to scaling limitations on the PD-SOI MOSFET. Use an Ultra Large Scale Integration (ULSI) device for better scaling. The proposed PD-SOI MOSFET was implemented using the Silvaco TCAD tool. Also, the performance of a proposed model was validated in terms of DIBL, threshold Voltage Roll-Off and DC sweep simulation for different values of channel length.

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