SSRG International Journal of Electronics and Communication Engineering
ISSN: 2348-8549/ https://doi.org/10.14445/23488549/IJECE-V13I1P113

Volume 13 Issue 1, 148-156, January 2026

Original Article

Design of an Efficient Forward Error Correction Transceiver for Advanced Communication System on Hardware Platform

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Received: 08 November 2025 Revised: 09 December 2025 Accepted: 08 January 2026 Published: 14 January 2026

Abstract *- The serial concatenation of Bose-Chaudhuri-Hocquenghen (BCH) and Low-Density-Parity-Check (LDPC) codes results in an efficient channel coding framework which is used in the next generation of advanced communication, such as video broadcasting and satellite applications, for transmitting data on non-ideal communication channels with constrained bandwidth. The Next Generation Communication System's high-speed necessities and adaptive coding approach create significant design issues for an effective codec hardware implementation. This manuscript proposes an efficient Forward Error Correction (FEC) Transceiver (TR) architecture by concatenating the BCH and LDPC codes on the hardware platform to overcome the design issues in the next-generation communication system. The FEC TR system utilizes <1 % chip area, operates at 343.5 MHz, and obtains a Throughput of 1.202 Gbps with a Bit Error Rate (BER) of 10-8 on the Artix-7 chip. The FEC transmitter and receiver use only 22.5 and 18 Clock Cycles (CC), obtaining the Throughput of 1.44 Gbps and 1.202 Gbps, respectively. Lastly, the FEC TR, BCH, and LDPC modules are compared with existing approaches, with enhanced improvement in the performance parameters.*

Keywords *- Forward Error Correction (FEC), BCH and LDPC Codes, FPGA, 5G and Beyond, FEC Transceiver, Serial concatenation.*

1. Introduction

Communication of data between origins and consumers is difficult in wireless networks because there is no wired connection. The wireless channel is prone to several disruptions, which could result in receiving the error code at the target location. Channel coding is employed to identify and fix transmission errors. The information sent can have errors found by the channel coding, which can then fix the flaws and recover the original information. The transmission channel in a wireless connection is noisier and requires effective channel Coding [1, 2].

In order to reduce Amplified Spontaneous Emission (ASE), a type of noise that naturally occurs in optical amplifiers and in which bit mistakes happen haphazardly, Forward Error Correction (FEC) codes were first applied to optical connection networks. FECs, however, had to operate within burst error conditions and deal with additional optical imperfections at the transmission rate progressively increased.

Furthermore, economics mandated the creation of robust digital end-to-end processing approaches, which typically depend on strong FECs, to improve visibility along with the expansion of optical connections. One of the primary technologies that allows for the subsequent development of optical networks is the FEC [3, 4].

FEC is a popular substitute for retransmission in which redundant information is created utilizing coding theory approaches from the original information. The actual time communication protocol features for noninteractive streaming applications from the Worldwide Internet Infrastructure Working Group suggest error-correcting codes, including Low-Density Parity-Check (LDPC) and digital fountain codes [5]. The effective FEC code used by the 2nd generation Terrestrial and satellite-based Digital Video Broadcast (DVB-T2 and DVB-S2) standard is built on the sequential combination of BCH and LDPC codes for High-Definition Television (HDTV) and Satellite Communications [6]. The combination of LDPC and BCH codes is used further in storage (non-volatile memory) [7],

green communication [8], Partial-band jamming [9], and image compression [10] applications.

The FEC transceiver architecture is designed by concatenating the BCH and LDPC codes on a hardware platform for the advanced communication system. The main contribution and the significance of this research work are described as follows: The BCH decoder is designed with Double Error Correction (DEC) capability using a 2-step mechanism, including a syndrome generator and Chien search approach, which improves the chip area and throughput of the system. The LDPC decoder is designed using a simple Minimum-Sum Algorithm (MSA) approach using a Tanner graph, which improves data rate with minimal resources on hardware.

The concatenation of BCH with LDPC-based FEC TR offers a lower chip area and higher data rate with reduced Bit Error Rate (BER). The overall organization of the manuscript is described in the following order: The current FEC-related research work is reviewed and listed in Section 2. The hardware architecture of the proposed FEC transceiver is described in detail with BCH and LDPC codes in Section 3. The implementation results and outcome of the proposed design are evaluated in Section 4 with a comparative analysis. Finally, the conclusion of the work and future scope of the research work are highlighted in Section 5.

2. Related Work

This section discusses the current works of the LDCP, BCH, and concatenated coding approaches to realize their performance metrics. Gupta et al. [11] present the concatenated LDPC with BCH codes for the Digital Video Broadcast Satellite (DVB-S2) system. The system uses the Eight-Phase-Shifting Keying (PSK) as a modulation approach under a Rician fading channel. The system obtains the Bit Error Rate (BER) of 0.026 for a Signal-To-Noise Ratio (SNR) of 5 dB with 50 iterations by incorrectly reducing the decoding of 1938 bits. Gagan et al. [12] describe the Orthogonal Frequency Division Multiplexing (OFDM) system using Concatenated codes. The system uses the Quadrature Amplitude Modulation (QAM) technique in conjunction with an AWGN channel.

The LDPC decoder uses the Sum-Product Algorithm (SPA), and the BCH decoder uses the Berlekamp-Massey Algorithm (BMA). The system obtains the BER of 10^{-5} at an SNR of 24 dB and 10^{-6} at an SNR of 28 dB. Mathur et al. [13] explain the LDPC decoding mechanism using the bit-flipping approach for DVB-S2 applications. The system uses two modulation approaches, QAM and Quadrature Phase-Shifting Keying (QPSK), for performance realization under the AWGN channel. The work uses the MATLAB Simulink tool to realize the performance metrics. The LDPC system obtains a BER of 0.5 for both QAM and QPSK approaches by detecting 8105 errors.

Cai et al. [14] discuss the concatenated codes (LDPC and BCH) for optical communications on the FPGA platform. The work analyzes the BER and error probability at different code lengths. The system obtains the BER of 10^{-2} within 0.79 dB. Digdarsini et al. [15] describe the FEC-based Encoder implementation using BCH and LDPC codes for DVB-S2 applications. The system uses the QPSK modulation approach and works at a code rate of ½ with a code length of 64800 bits. The work realizes only the simulation results of the FEC encoder as part of the functional verification process. Mahdy et al. [16] present the parallel branches-based concatenated codes on an FPGA. This work uses two/four BCH branches concatenated with one LDPC on Encoder/decoder architectures. The system obtains a throughput of 200 Mbps for the encoder and 50 Mbps for the decoder. Mahdy et al. [17] explain the parallel concatenated codes for flash memories. The work realizes the BER by considering different SNRs and obtains the BER of 10^{-5} at an SNR of 1.5 dB. Kang et al. [18] discuss the FEC encoder core for satellite ground communications. The FEC encoder uses BCH, LDPC, and bit interleaver units. The work analyzes the simulation and performance results of the Kintex-7 FPGA. The FEC encoder core works at 1.19 Gbps for Variable Coding Modulation (VCO) approaches.

Kalya and Kumar [19] describe the Modified Anderson-based Physically Unclonable Functionality (PUF) key generation using LDPC codes. The LDPC codes use the bit-flipping approaches to detect and correct the errors in key generation. The work analyzes the simulation and synthesis results, improving uniformity. Qiu et al. [20] present the concatenated coding approaches using Reed-Solomon (RS) and Spatially Coupled (SC) LDPC. The work is carried out on the MATLAB tool and tests the performance results of BER v/s SNR at different code lengths. Huang et al. [21] explain the Deep Neural Network-based SPA decoders using auto-adaptive SNR algorithms for BCH and LDPC codes. The work reduces the convergence rate to 28 % and 35 % for BCH and LDPC codes, respectively. Rohit and Ramesha [22] discuss reviewing the FEC coding approaches on FPGA platforms. The work discusses the working operations of the BCH and LDPC codes. The different hardware architectures of both BCH and LDPC codes are discussed. The performance comparison of BCH, LDPC, and concatenated codes and their applications is discussed in detail.

3. Proposed FEC Transceiver

The FEC Transceiver core system is represented in Figure 1. The FEC core mainly contains the FEC Transmitter (TX), AWGN Channel, and FEC receiver modules. The FEC TX contains a BCH encoder, Serial-To-Parallel (S2P) converter, LDPC encoder, Interleaver, and Quadrature Amplitude Modulation (QAM) modules. The FEC RX has QAM demodulation, followed by a

deinterleaver, LDPC decoder, Parallel To Serial (P2S) converter, and BCH decoder. The BCH encoder receives the user's 7-bit data in a sequence and produces the 1-bit encoded data. The S2P converter converts the serial data to 8-bit parallel data using a shift register. The LDPC Encoder receives the 8-bit parallel data and performs the encoding operation using the generator matrix. The encoded data is stored row-wise and read out column-wise once the matrix is filled by the matrix interleaver. The QAM performs the constellation mapping based on interleaved data and generates the In-phase (I) and Quadrature-Phase (Q) data bits. The FEC-Transmitter produces the IQ-data values and inputs to the AWGN channel. The FEC receiver receives the corrupted IQ data values from the channel and performs the QAM demodulation. The deinterleaver receives the 4-bit demodulated data column-by-column and reads row-by-row till the matrix is complete. The LDPC decodes the deinterleaved error burst data using the Minimum Sum Algorithm (MSA). The MSA approach contains a parity check matrix and Tanner graph with majority logic. The 8-bit decoded data is converted back to serial data using a P2S converter. The BCH decoder performs the decoder operation to generate the final 7-bit output data using syndrome calculation and error location finding operations. The individual operation of the BCH and LDPC sub-modules of the FEC TR is explained as follows:

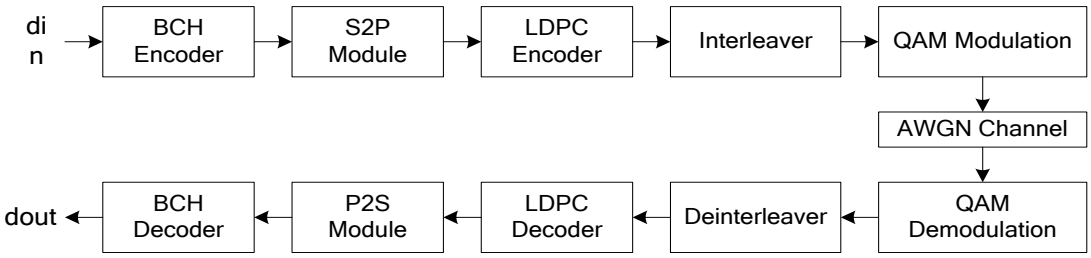

Fig. 1 Proposed FEC-TR core system

3.1. BCH Encoder

The codeword is obtained by using data bits (d) and the Generator Polynomial (g) in BCH codes (n, k, t). Where 'n' is the length of each codeword, 'k' is the data bits used in the codeword, and 't' is the number of errors to be corrected. This work considers the BCH (15, 7, 2) code format to detect and correct two-bit errors. The codeword polynomial is represented as $c(x) = d(x) + g(x)$. The Generator Polynomial g(x) defines the Error Correcting Codes (ECC). The BCH encoder uses the generator polynomial for 2-bit error correction, and it is described in Equation (1).

$$g(x) = 1 + x^4 + x^6 + x^7 + x^8\,; \quad (1)$$

The initialization of the Linear Feedback Shift Register (LFSR) is set to zero. The parity bits are generated using an LFSR, while the data bits d(x) are sent over 1 to k clock cycles. During k+1 to 'n' clock cycles, the generated parity bits in the LFSR are transmitted in parallel. The data bits (k) are added to the (n-k) parity bits to produce the encoded information. For DEC, the encoding technique generates the eight parity bits. Figure 2 shows the Linear Feedback Shift Register (LFSR) generation for the DEC-based BCH (15, 7, 2) encoder block.

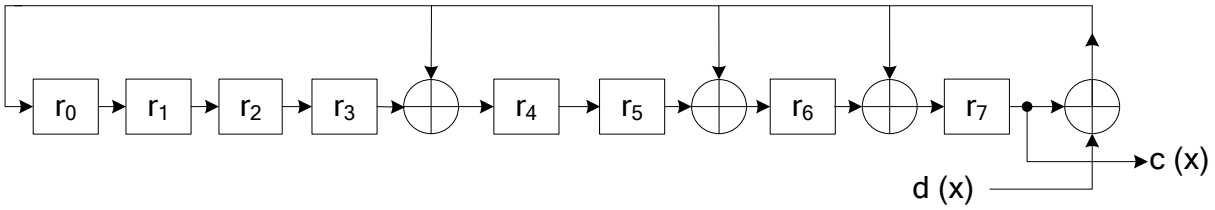

Fig. 2 Linear feedback shift register (LFSR) generation for BCH (15, 7, 2) encoder

3.2. LDPC Encoder

The LDPC codes are a type of linear block code and are designed with the help of a Generator Matrix (G) and Parity Check Matrix (M). The LDPC codes provide error correction features and are used in most applications. The LDPC encoder is constructed using a Generator Matrix (G), as shown in Figure 3. The G = [I P]. The 'I' denotes information bits and 'P' denotes parity bits. The sixteen code words (c_0 to c_{15}) are generated in this LDPC encoder with code rate 1/2. The first eight code words (c_0 to c_7) represent 8-bit information bits, and the following eight code words (c_8 to c_{15}) represent 8-bit parity bits. The LDPC Encoder generates the 16-bit encoded output, which contains the code word information.

3.3. LDPC Decoder

The LDPC decoder is constructed using a Multi-Source Agreement (MSA) approach by considering the Parity Check Matrix (M). The 'M' contains 'X' rows and 'Y' columns. The 'X' denotes check nodes and 'Y' denotes variable nodes. The check nodes contain the information bits, whereas the variable nodes contain bits of the

codewords. The matrix 'M' has many zeros and a few ones, and it is constructed using a random distribution. The Parity Check Matrix Generation is rearranged M = [P^T I], and it is illustrated in Figure 4 for the LDPC Decoder implementation, where P^T represents the transpose of parity bits.

G = [I P] =

	c_0	c_1	c_2	c_3	c_4	c_5	c_6	c_7	c_8	c_9	c_{10}	c_{11}	c_{12}	c_{13}	c_{14}	c_{15}
i_0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
i_1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	1
i_2	0	0	1	0	0	0	0	0	0	1	1	1	0	1	0	0
i_3	0	0	0	1	0	0	0	0	0	1	1	0	0	1	1	1
i_4	0	0	0	0	1	0	0	0	0	1	1	1	0	1	1	1
i_5	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0
i_6	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	1
i_7	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0

I P

Fig. 3 Generator matrix for LDPC encoder

M = [P^T I] =

1	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0
1	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0
0	0	1	0	1	0	0	0	1	0	0	1	0	0	0	0
0	0	0	1	0	0	0	1	0	0	1	1	0	0	0	0
0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1	0	0	0

Fig. 4 Parity check matrix generation for LDPC decoder

The proposed hardware architecture of the LDPC-based decoder is described in Figure 5. The proposed architecture contains a parity check matrix generator, a check, and variable nodes. The parity check matrix generator generates eight check nodes (CN_0 to CN_7) row-wise and sixteen variable nodes. Each Check Node (CN) receives 4-bit Data (m) from 'M' and generates the 4-bit Output (s). The check node generation is represented using Equation (2).

$$[s_3, s_2, s_1, s_0] = [(m_1 \oplus m_2 \oplus m_3), (m_0 \oplus m_2 \oplus m_3), (m_0 \oplus m_1 \oplus m_3), (m_0 \oplus m_1 \oplus m_2)] \quad (2)$$

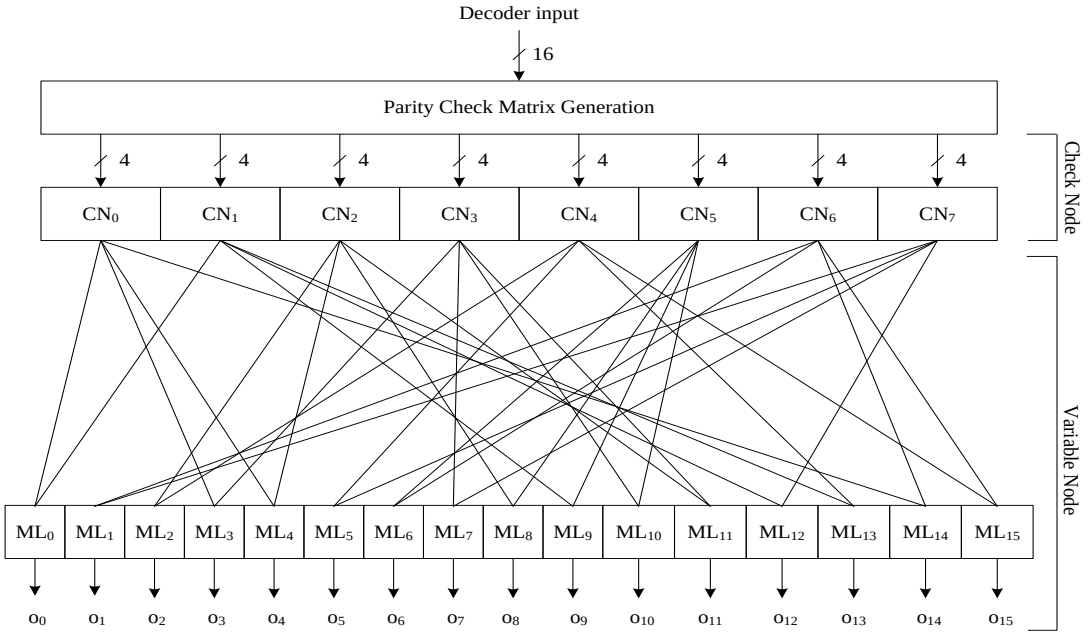

Fig. 5 Hardware architecture of the LDPC decoder

The output of each CN is connected to a Variable Node (VN) based on the Parity Check Matrix (M) using the Tanner graph. Each variable node receives a 1-bit codeword followed by a 2-bit check node output. The received 3-bit Data (t) in VN performs the Majority Logic (ML) operation to generate the decoded output. The output (O) of the ML operation is represented using Equation (3).

$$O = (t_0\, t_1 + t_0\, t_2 + t_1\, t_2) \quad (3)$$

The same ML process applies to all sixteen VN to generate the 16-bit decoded output. Out of the 16-bit decoded output, the first 8 bits are considered the LDPC decoder output.

3.4. BCH Decoder

Three steps comprise the BCH decoding process: calculating the syndrome, solving the key Equation, and locating the error. The syndrome calculation step yields the error location polynomial coefficient and is the only step to decode the DEC-based BEC codes. Therefore, solving key Equations is not used in DEC operations. Figure 6 shows the implemented hardware design of the BCH decoder for DEC. It primarily consists of a control unit, a Serial-Input-Serial-Output (SISO) register, an error detection unit, a Chien search module, and a Syndrome Generation Module (SGM). The syndromes were created using the SGM, which was also utilized to identify the coefficients of each error location polynomial. The Codeword c(x) was input to the BCH decoder, which was then utilized to calculate the syndrome. The Error-Input e(x) is corrupted with Codeword c(x); its outcome is input to the SGM. The next step in the BCH decoding operation is to identify the error location values, which are reciprocals of the error location polynomial roots. When employing CSM, the relevant primitive element of GF (2^4) is added into the error location polynomial place to determine the error location values. The detection module finds the error bits, and the CSM identifies the error locations. Based on the output of the control signal, the Serial input -Serial output register shifts the corresponding input data bits, and the outcomes are XORed with the erroneous bits to form the updated output bits. The control unit acts as a counter to the decoding logic circuit.

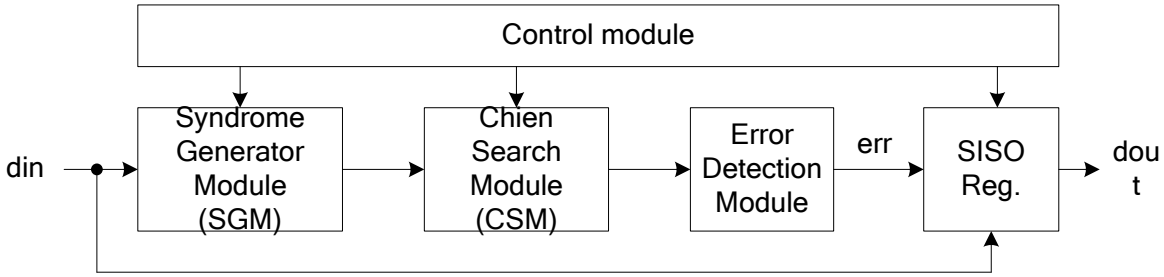

Fig. 6 Proposed hardware architecture of the BCH decoder for SEC and DEC

4. Results and Discussion

In this section, the performance and comparative analysis of the proposed FEC TR system are discussed. The Proposed FEC TR and sub-modules are designed using Verilog-Hardware Description Language on the Xilinx ISE environment. The simulation result is realized using the ModelSim simulator tool, and it provides functional verification of the design work for different test cases. The FEC TR system is implemented and prototyped on Artix-7. (XC7A100T-3CSG324) Device. The FEC TR system's simulation results are illustrated in Figure 7. The Clock Of The System (clk) is triggered with the Low Reset (rst) to initialise the FEC module operation. The 7-bit Data Input (din) and 15-bit error data are inputs, and the 7-bit data (dout) acts as an output signal. The 16-bit in-phase and Quadrature-phase outputs of the FEC Transmitter are also represented in Figure 1. The FEC TR takes 40.5 Clock Cycles (CC) to generate its first output and is considered the system's Latency. This FEC TR system can detect and correct 2-bit errors in data.

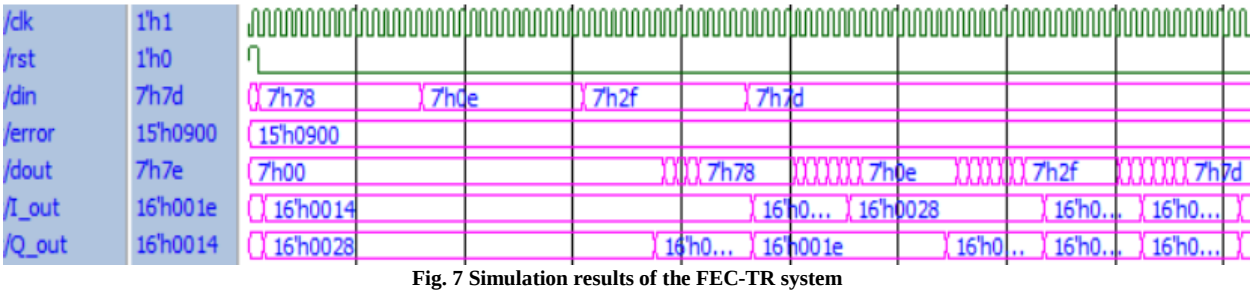

Fig. 7 Simulation results of the FEC-TR system

The performance analysis of the proposed FEC TR system and its submodules, like the Transmitter (TX) and Receiver (RX), is mentioned in Table 1. The chip area utilisation (slices and Lookup Table (LUTs)), Operating Frequency (MHz), Power (mW), Latency (CC), Throughput of the proposed system (Gbps), and hardware usage efficiency (Mbps/Slice) are mainly considered as performance metric parameters in this work. The FEC TX uses only < 1% Chip area and operates at 412.371 MHz, with a total power consumption of 86 mW. The FEC RX uses only < 1% Chip area and operates at 342.525 MHz, with a total power consumption of 86 mW. The FEC TR system utilizes a chip area of 1 % by operating at 343.525 MHz and consumes 87 mW on an Artix-7 FPGA. The FEC TX uses only 22.5 CC as Latency, 1.443 Gbps as throughput, and 13.875 Mbps as hardware efficiency on the FPGA Chip. Similarly, the FEC RX uses a Latency of 18 CC, throughput of 1.202 Mbps, and efficiency of 8.843 Mbps/Slice on an FPGA Chip. Lastly, the FECTR system uses a Latency of 40.5 CC, throughput of 1.202 Mbps, and efficiency of 5.096 Mbps/Slice on an FPGA Chip. The graphical representation of the FEC-TR module's resource utilization is illustrated in Figure 8.

Table 1. Performance analysis of the FEC-TR system

Parameters	FEC-TX	FEC-RX	FEC-TR Core
Slices	104	136	236
LUTs	91	143	233
Max. Frequency (MHz)	412.371	343.525	343.525
Total Power (mW)	86	86	87
Latency (CC)	22.5	18	40.5
Throughput (Gbps)	1.443	1.202	1.202
Efficiency (Mbps/Slice)	13.875	8.843	5.096

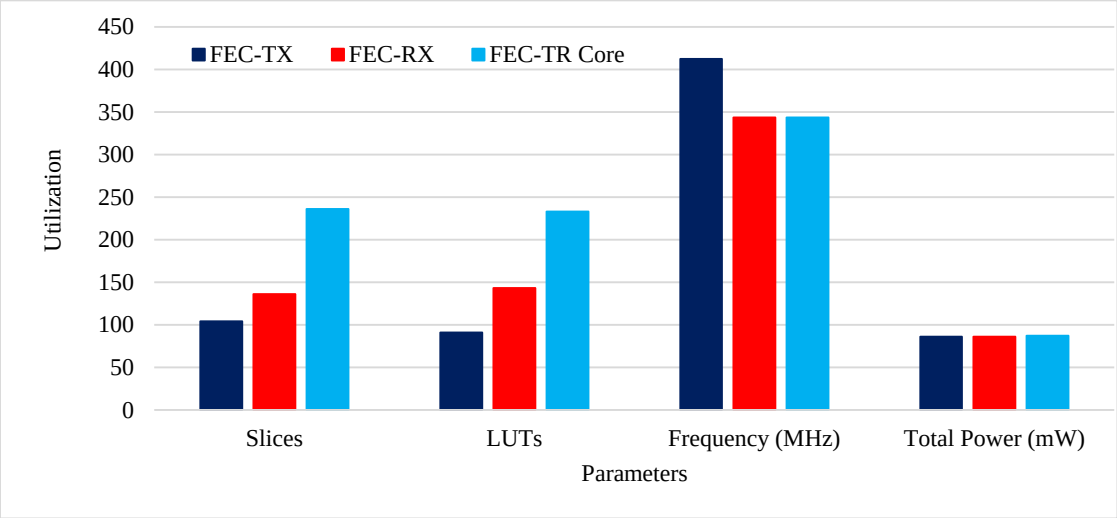

Fig. 8 Graphical representation of the FEC-TR module's resource utilization

Table 2. Resource utilization of the FEC-TR system submodules

Parameters	LUTs	Max. Frequency (MHz)	Latency
BCH Encoder	35	866.927	2
S2P Module	1	761.035	1
LDPC Encoder	8	100*	0.5
Interleaver	44	410.948	18.5
Modulation (QAM)	6	NA	0.5
Demodulation (QAM)	15	NA	0.5
Deinterleaver	60	437.752	12
LDPC Decoder	24	1008.776	2
P2S Module	13	948.227	1
BCH Decoder	40	343.525	2.5

The FEC TX operates at a higher frequency due to the encoding mechanism. The FE CTR system utilizes minimal power due to less chip area (1 %) usage. The Resource utilization of the FEC-TR System submodules is tabulated in Table 2. TX and RX submodules utilize < 1 % chip area (LUTs) on Artix-7 FPGA. Encoding (BCH) and Decoding (LDPC) mechanisms operate at higher frequencies along with Shift register (S2P and P2S) modules. Due to memory access for write and read operations, the interleaver and Deinterleaver modules consume more clock cycles (18.5 and 12).

The proposed system performance comparison of BCH and LDPC with available approaches is illustrated on different FPGAs in Table 3. The FPGA device utilisation, chip area, operating frequency, and overall throughput parameters are compared for performance. The low-complexity-based BCH codes for high-throughput applications are designed on Virtex-7 FPGA [25]. The proposed BCH codes utilize fewer slices of 19.6 %, LUTs of 31.16 %, and improve the throughput of 76.15 % compared to existing BCH codes [25]. The single-bit error correction-based BCH codes for memory computations are designed on a Kintex-7 FPGA [26]. The proposed BCH codes utilize fewer slices, 78 %, and LUTs 83 %, and operate at a better frequency of 84 % compared to existing BCH codes [26]. The complex and soft-input-based BCH codes for concatenated codes applications are designed on Virtex-7 FPGA [27]. The proposed BCH codes utilize fewer slices and LUTs of 87 % and LUTs of 31.16 % and operate at a better frequency of 48 % compared to existing BCH codes [27]. The LDPC coding approach for video broadcasting applications is designed on a Virtex-4 FPGA [28]. The proposed LDPC codes utilize fewer slices of 54 % and LUTs of 82%, and LUTs of 31.16 % and operate at a better frequency of 64 % than existing LDPC codes [28]. The LDPC codes for lightweight cryptography are designed on a Virtex-6 FPGA [29]. The proposed LDPC codes utilize less chip area and operate at a better frequency of 62 % and throughput of 30 % compared to existing LDPC codes [29]. The modified rejection-based LDPC codes using a min-sum approach are designed on a Virtex-7 FPGA [30]. The proposed LDPC codes utilize fewer LUTs of 74 % and LUTs of 31.16 % and operate at a better frequency of 50 % than existing LDPC codes [30].

Table 3. Performance comparison of proposed BCH and LDPC with existing approaches [25-30]

Resources	FPGA	Slices	LUTs	Frequency (MHz)	Throughput (Mbps)
BCH Codes					
Ref [25]	Virtex-5	102	77	115	1700
Ref [26]	Kintex-7	379	316	100	115
Ref [27]	Virtex-7	NA	426	333	111
Proposed BCH	Artix-7	82	53	649	7131
LDPC Codes					
Ref [28]	Virtex-4	102	186	357	21.4
Ref [29]	Virtex-6	903	2326	375	2232
Ref [30]	Virtex-7	NA	125	500	334
Proposed LDPC	Artix-7	46	32	1008.776	3230

The performance comparison of the proposed FEC TR with existing FEC works [31-33] is tabulated in Table 4. The LDPC with BCH Codes implementation is designed on Virtex-2 FPGA [31]. The proposed FEC TR utilizes fewer LUTs of 20 %, a better frequency of 68 %, and a BER improvement of 62.5 % compared to the existing FEC TR [31]. The BCH with LDPC codes for DVB applications is designed on CMOS Technology to improve the BER Characteristics [32]. The proposed FEC TR operates at a better frequency of 89 %, throughput of 87 %, and 12.5 % of BER improvement than the existing FEC TR [32].

Table 4. Performance comparison of proposed FEC TR with existing FEC works [31-33]

Resources	Ref [31]	Ref [32]	Ref [33]	Proposed FEC Core
FPGA	Virtex-2	NA	Spartan-3E	Artix-7
BCH method	BMA	BMA	BMA	CSM
LDPC Method	MSA	MSA	MSA	MSA
Modulation	No	APSK	No	QAM
Slices	180	NA	449	236
LUTs	292	NA	814	233
Frequency (MHz)	112.09	36	100	343.525
Data rate (Mbps)	NA	155	400	1202
BER	10^{-3}	$< 10^{-7}$	10^{-4}	10^{-8}

The BCH with LDPC codes on the Spartan-3E FPGA is designed to realize the BER [33]. The proposed FEC TR utilizes fewer slices of 47 % and LUTs of 71 %, LUTs of 31.16 %, better frequency of 70 %, the throughput of 66 %, and 50 % of BER improvement than the existing FEC TR [33]. The current BCH, LDPC, and concatenated coding approaches use a traditional mechanism to realize the performance. The proposed design uses simple and optimized BCH and LDPC approaches to improve the performance metrics. Overall, the proposed work improves the chip area, operating frequency, throughput, and BER compared to other FEC approaches.

5. Conclusion and Future Work

The efficient FEC transceiver architecture is explained in this manuscript, where BCH and LDPC coding mechanisms are concatenated in order to support the advanced communication system on the Field Programmable Gate Array (FPGA) hardware platform. The proposed work can be identified and remodified with the help of the BCH-based codes in case of double error. The design of the BCH-based encoder is made by an LFSR. The BCH-based decoder and DEC are developed without employing the BMA approach to improve and enhance the chip area and general throughput of the decoder. The LDPC-based decoder is said to take the MSA approach, the Tanner graph, to improve the system throughput and performance while reducing hardware complexity. The utilization of resources of the FEC TR core and its sub-modules is achieved in detail. FEC TR core is a low-power chip consuming 343.5 MHz and uses less than 1 percent of the chip area. Latency of 40.5 CC, Throughput of 1.202 Gbps, and hardware efficiency of 5.096 Mbps/Slice are achieved on the FEC TR core on Artix-7 FPGA. The LDPC, BCH, and FEC TR modules are plotted separately against an already existing similar method with a higher chip area (slices and LUTs), operating frequency, and the overall Throughput. This FEC TR core is provided with appropriate security algorithms to improve the aspect of confidentiality and privacy of data.

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