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Original Article

Advances in Polar Code Decoding for Next-Generation Communication Systems: A Comprehensive Review

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Abstract *- Polar codes have become a milestone in forward error correction, as they can achieve the channel capacity for Binary-input Memoryless Symmetric (BIMoS) channels and Binary input Partial Response (BPR) channels. Nowadays, their practical deployment still suffers challenges, particularly at short to moderate block lengths, because of the high computational complexity and limited level of parallelization offered by polar codes. The paper proposes the recent advances made in decoding algorithms and hardware implementations, which particular emphasis on recent improvements to Successive Cancellation List (SCL) decoders. The developments can be categorized into three: algorithmic enhancements (Fast-SSCL, polarization-adjusted convolutional codes), parallelization schemes (g-computation, g-branching), and hardware accelerations (unrolled architectures, approximate maximum-likelihood decoding). Together, they work to improve decoding speed and latency while reducing power area constraints of the decoders, thus making polar codes ever closer to real-time deployments in contemporary communication systems. Integrating these methodologies with polar codes may significantly enhance communication. The comparative study of the literature survey demonstrates the high performance of decoder, which can reduce implementation complexity. Existing studies largely focus on terrestrial channels, with insufficient domain-specific evaluation of advanced FEC schemes under GNSS and optical satellite channel impairments. This is one of the research gaps identified.*

Keywords *- Polar codes, Forward error correction, Successive cancellation list, Decoding, Low-latency decoders, FPGA implementation, High-throughput communication systems, Fast-SSCL, GNSS, Optical satellite links*.

1. Introduction

Modern communication system demands wireless connectivity, smooth media streaming, and fast integration of IoT devices. To sustain these needs, the future mobile communication systems like the envisioned 5G-and-beyond depend immensely on robust and highly friendly error-correction mechanisms. In a way, the FEC is a stratum of assurance of information integrity against noisy communication channels, as it enables receivers to detect and correct errors themselves, without asking for retransmission. In recent years, polar codes have become very famous for being quite different from most others [14, 15].

Polar codes stand among the great landmarks in coding theory. It is the first celebrated class of codes that has been proven theoretically to attain the symmetric capacity of Binary input Memoryless Channels with a relatively simple encoding and decoding operation. In simple terms, polar codes can indeed send data at rates approaching channel capacity with diminishing probability of error, a property worthy of modern wireless standards like 5G [15, 21].

The central point in the concept of polar codes is channel polarization. Through a recursive combination and splitting operation on two identical channels, polar codes strive to create a set of ones that are highly reliable and others that are highly unreliable. The most reliable among them carry the information bits, while the highly unreliable ones are frozen bits. As the length of the code increases, the effect of polarization becomes stronger so that the code very finely approaches the channel capacity [15].

Taking into account their theoretical elegance for very long code lengths, however, polar codes do have practical limitations at short and moderate block lengths. The originally proposed Successive Cancellation decoding by Arıkan is computationally efficient yet rather weak in error correction for finite-length codes. This error correction performance

becomes an overbearing limitation for applications with stringent delays, such as real-time video transmission, embedded systems, and mobile communication [10, 16].

To fix these issues, the Successive Cancellation List (SCL) decoding method was introduced. In contrast to SC decoding, SCL keeps various decoding paths alive by assigning each decision step with either of the two bit values. The most likely path is chosen optionally through a Cyclic Redundancy Check (CRC). This arrangement greatly helps in error correction for short and medium block lengths, thus paving way for actual implementation of polar codes [10, 15].

SCL decoding cannot solve every problem. Very often, the computational overhead and memory overhead put augmenting the number of paths are becoming too large. The complexity scales with the list size, against high throughput and low latency in hardware-constrained environments. These limitations led to a need to optimize the algorithm and hardware architecture for SCL-based polar decoders [2, 7, 10].

The paper surveys the major developments that have taken place to address these issues. It first reviews algorithmic improvements such as Fast-SSCL and Fast-SSCL-SPC, which rely on the structure of polar codes (e.g., rate-one and single parity check nodes) to remove redundant computations. Then it looks into scheduling and parallelism techniques that work to get around the serial bottlenecks found in SC decoding, particularly via early computation and g-branching approaches. Hardware-specific techniques are next discussed, including unrolled architectures and Approximate Maximum Likelihood (AML) decoders, that provide high throughput with favourable area and energy trade-offs. Furthermore, there are latency-focused measures such as tree pruning and the utilization of Polarization Adjusted Convolutional (PAC) codes to improve performance at finite lengths.

The survey plans to summarize the most recent progress in decoding algorithms and hardware architectures for polar codes, hoping for further research into next-generation systems such as 5G, GNSS, and optical satellite communications. Some of these systems deal with designing efficient FEC codes, low-complexity algorithms for resource-constrained hardware, FPGA implementations, and architectural techniques with energy and area efficiency in mind. More specifically, by studying the advances at the algorithm level and hardware level, this paper aims at the practical realization of polar codes for current high-performance communication environments.

Unlike prior surveys such as [21], which limit their scope to SCL-based decoders for 5G applications, this review extends the coverage to include PAC codes, FPGA architectures, GNSS-specific constraints, and optical satellite systems. Furthermore, a structured comparative table (Table 1) is presented that maps each reviewed work against standardized criteria of methodology, limitations, research gaps, and future directions.

In spite of significant advances in polar codes decoding algorithms, hardware implementation, and implementation of latency reduction strategies in next-generation communication systems, their essence in the field of GNSS and satellite communication applications is still underexplored. This paper addresses this gap by systematically surveying and categorizing advances across these three dimensions, offering a unified perspective to guide the design of practical polar decoders for GNSS and satellite communication applications.

2. Literature Survey

The survey can be classified into algorithmic advances in SCL decoding implemented till date, hardware architecture optimizations used, low-latency decoding techniques formulated to check improvements, and alternative coding schemes which aims to improve the application of polar codes.

2.1. Algorithmic Advances in SCL Decoding

S. A. Hashemi et al in “Fast and Flexible Successive-Cancellation List Decoders for Polar Codes” has proposed a new decoding scheme, termed Fast-SCL and Fast-SSCL-SPL, which and boosts the speed and flexibility of polar codes in successive cancellation list decoding [2]. Polar codes have found a distinguished place in the contemporary communication system where SCL decoding tries to strike a balance between error correction and complexity, with throughput invariably being the constraint. The new method demonstrates that the list size (L) determines if path splitting is necessary during the decoding of rate-one and single parity check codes. This insight allows one to reduce path splitting at no cost to error-correcting performance. Therefore, these optimized algorithms, known as Fast-SSCL and Fast SSCL-SPC, require fewer number of computational steps. Further, the paper presents an approach for practical applications so that speed can be adjusted desirably with little detriment to error-correction capabilities. Then, the paper describes certain hardware architectures that implement these algorithms at a throughput of 1.862 Gb per second. The research states the performance of Fast SSCL SPC, which proves the similar error correction performance as SSCL SPC. The paper discusses the different techniques, such as successive cancellation decoding and list decoding, and algorithm of Fast SSCL and Fast SPC has been proposed by presenting implementation results. The proposed architecture finds a compromise between area occupation and performance.

H. Saber et al in “Simplified Successive Cancellation List Decoding of PAC Codes” has proposes an SSCL algorithm for PAC codes to reduce latency during decoding while keeping the performance intact [5]. PAC codes, being a kind of polar codes, embed a Convolutional-Code-Based (CC) precoder to improve coding gain in both Fano sequential decoding and successive cancellation list decoding. SCL decoding still

holds certain advantages over Fano decoding, especially in low signal-to-noise ratio scenarios and when worst-case latency assurances are needed; hence, the current work optimizes SCL decoding for PAC codes. The basic principle of this method lies in identifying some "special nodes" within the decoding tree and processing them efficiently. It's a great way to reduce latency since the SSCL decoder does not process these subtrees and carries on with unnecessary calculations. The paper defines special nodes in terms of the information-carrier vector, thus adapting the polar-codes concept to take into consideration the effect of the CC precoder. Algorithms are then designed for the handling of these special nodes under the effect of CC encoding for four types of special nodes. These methods reduce latency by 34% in decoding. To reduce the complexity involved, inverse CC encoding is presented in order to have list members at the input of the CC encoder. Such inverse CC encoding is demonstrated to have linear complexity in terms of special node length, and the inverse CC generator polynomial has a nested property that allows for easier implementation. An exhaustive overview of PAC Codes and SCL decoding as applicable in the algorithm, with proceedings for managing the four classes of special nodes, is given by the author. Finally, the paper remarks on the advantages enjoying SSCL decoding of PAC codes.

C. Condo et al. in “Efficient Bit-Channel Reliability Computation for Multi-Mode Polar Code Encoders and Decoders” has devised a method for determining bit channel reliabilities for encoders and decoders in multiple modes [6], which reduces implementation complexity. Polar codes rely on the relative reliability of their bit channels to differentiate information-carrying bits from frozen bits. The proposed procedure trades off the accuracy of reliabilities with the complexity of implementation to allow for a better fit to application constraints. The method works by identifying patterns in the reliability vector by splitting the vector into two halves and representing those halves with a sequence of related variables. These sequences of variables can be used generally, for different code lengths, thereby significantly reducing the storage requirements. Using the Computation technique, an architecture has been designed and implemented such that efficient reliability determination is enabled for both encoder and decoder. These results greatly reduce storage, including error correction performance.

A. Balatsoukas et al. "LLR-Based Successive Cancellation List Decoding of Polar Codes” describes a novel formulation of polar channel codes meant for a successive cancellation list decoder based on the Loglikelihood Ratio (LLP) domain. The paper [10] describes several advantages and the stability offered by the LLR approach, which indeed simplifies the sorting step present in SCL decoding. It mentions an architecture of LLR-based SCL decoders, which require much less irregular and smaller memories as compared to the prior log-likelihood domain implementation. Throughput per unit area is improved due to fewer reductions being made in tandem with improvements to metric sorting. The authors show that the proposed CRC-aided SCL decoders combine some somewhat lower throughput and larger area than conventional successive cancellation decoders of large block-lengthing with much shorter decoding latency. The LLR-based SCL decoder constitutes a path management unit together with low-complexity, parallel LLR-based SC decoders as building blocks. A very important contribution is the simplification of the metric sorter by avoiding useless comparisons that arise because of peculiarities of the LLR-based path metric. The comprehensive synthesis results presented in the paper demonstrate the hardware efficiency and throughput advantages, compared to current LL-based SCL decoder implementations. Next, the effect of different quantization parameters on performance is considered. Then, the efficiency of CRC-aided SCL decoding is studied, showing the trade-off between performance gain and the length of the cyclic redundancy check. The paper ends with a discussion comparing the latency and complexity of SCL and SC decoding.

Research [23], to ameliorate error correction performance and lower implementation complexity, discusses possible generation methods for measuring single parity check nodes within the Successive-Cancellation List decoding of polar codes. High throughput (SCL) decoding architecture is thus contributed by decoding single parity check nodes concurrently. The paper further goes on to mention that the Ratel node Candidate generation algorithm lends itself very well to efficient hardware implementation. This paper then shows huge improvements in terms of energy efficiency. Nonetheless, it talks about the general improvements attained and the prospects for further optimization.

This paper [24] combines complementary works from the SCL-based polar code decoders for short to medium code lengths by analyzing error correction performance, area, power consumption, and energy metrics. The review goes through the evolution of polar code decoding algorithms to further stress the performance-speed-complexity trade off. The hardware architecture of SCL, SSCL, fast-SSCL, and PSCL decoders, along with the memory unit, metric computation units, metric sorting unit, and instances of address translation units are presented by the author. A summary of the synthesis results of each decoder implementation are mentioned while discussing SCL-based decoders as having complexity almost comparable to LDPC codes. The author concluded the discussion with SCL-based polar code decoders being a promising solution for 5G applications.

C. Xiong et al. in “Symbol-Decision Successive Cancellation List Decoder for Polar Codes” has introduced a new detection scheme that would enable polar codes in wireless communication systems to cater to the specific

requirements of LTE and 5G standards. The main advantage of this approach would be to identify user-specific transmissions under stringent time constraints. The proposal in [12] entails sending the Radio Network Temporary Identification (RNTI) in place of frozen bits in the polar codes so these can replace the conventional cyclic redundancy check. The methodology implies decoding in two steps: act on candidates of all transmissions. Depending on the situation, a selected subset of candidates will be nominated for the further decoding process using the more cumbersome Successive Cancellation List (SCL) decoding algorithm, again preserving a balance between decoding speed and error-correcting capability. By simulation, this paper presents a comparative study based on FAR and MDR, also Block Error Rates (BLER). The SCL decoding step has been augmented with early stopping criteria to attempt to gain in average latency and energy consumption by reducing the number of operations performed. The Implementation analysis shows the realizability of implementing polar codes for blind detection in communication systems.

K. Niu et al. in "CRC-Aided Decoding of Polar Codes" have illustrated about the cyclic redundancy check in the successive cancellation decoding technique. The simulation in [15] has demonstrated that by adding gaussian noise to the binary channel can give a gain of 0.5 dB when it is been compared with turbo codes. The block error probability is 10^{-4}. The performance of time complexity shows a countable improvement when compared with the turbo codes for high SNR transmissions.

F. Ercan et al. in "On error-correction performance and implementation of polar code list decoders for 5G" mention various early stopping criteria for the belief propagation belief decoder of polar codes to save energy and latency during that period. It discusses observed disadvantages of performance optimizations for belief propagation while comparing with a Successive Cancellation (SC) decoder. The paper [21] proposes two types of detection early stopping criteria to find an output for belief-propagation decoding. These methods aim to reduce unnecessary iterations. The implementation of the methods demonstrated the methods decrease the signal-to-noise ratio. Allowing for a new channel Condition estimation technique for varying SNR regions. The paper also mentions the limitations of traditional H-Matrix-based detection. The research suggests that making iterative decoder termination strategies beneficial since the iterative decoder often converges early or never converges. The studies also use a scaling parameter to approximate the error induced by the min-Sum approximation in Polar BP decoding.

Z. Chen et al. in "Reduced Complexity List Polar Decoder with an Improved Path Pruning Scheme," has demonstrated about error correction performance and lower implementation complexity. The paper [22] discusses possible generation methods for measuring single parity check nodes within the Successive-Cancellation List decoding of polar codes. High throughput (SCL) decoding architecture is thus gets contributed by decoding single parity check nodes concurrently. The paper further goes on to mention that the Ratel node Candidate generation algorithm lends itself very well to efficient hardware implementation. This paper then shows huge improvements in terms of energy efficiency. Nonetheless, it talks about the general improvements attained and the prospects for further optimization.

2.2. Hardware Architecture Optimizations

G. Sarkis et al. in "Unrolled Polar Decoders, Part II: Fast List Decoders" explains on innovative schemes for speeding up the polar list decoding within the framework of software-defined radio applications. Polar codes, typically held being capable of reaching the symmetric capacity of memoryless channels, lose this stature for short and moderate lengths when decoded through successive cancellation [1]. CRC-aided list decoding possesses better error correcting capabilities and thus needs faster decoding since simultaneous exploration of the paths renders the process slower. Unrolled tree decoding is presented by the author to efficiently speed up list decoding in software. Further, the new algorithmic procedure addresses the computation of log-likelihood ratios while adopting features of the fast-SSC algorithm to realize performance enhancements in speed. A thorough analysis and comparison of the proposed decoder in terms of speed and error correction capabilities is then undertaken, with the findings that the list decoder can keep good error correction performance at small or moderate code lengths with provable faster speed relative to LLP-based list-SC decoding.

Polar codes achieve the symmetric capacity of memoryless channels nevertheless, the error correction performance of successive cancellation decoding is less when compared to error correction than LDPC codes, especially for short to medium block length. The list decoder, with a CRC attached, improves the performance, outperforming LDPC codes of similar length. However, the SC-SCL is slower than the regular SC due to the sequential bit-by-bit operations that characterize list decoding. By unrolling the decoding tree, this paper [1] introduces an extremely efficient and very fast list decoder for software, which speeds it up by a factor of the order of 10 with respect to the state of the art. The proposed approach is well-suited for software-defined radio applications since it beats the LDPC software implementations in the world in speed, yet maintains equal or better error correction performance for shorter or equal code lengths. The respective speedup is obtained by breaking the serial constraint of the successive cancellation. The premise here makes use of the fact that certain decoding stages are redundant for certain bit groups, thus enabling the possibility of simultaneous estimation. Polar codes are the concatenation of smaller codes like frozen bits become 0 and information bits become 1. The proposed algorithm is an extension of the Fast-SSC algorithm under list-based decoding, meant for

different constituent codes like repetition and single parity check codes, processing them together to estimate multiple bits per clock cycle. The algorithm performance is measured on a general-purpose processor through SIMD instructions. Low encoding complexity and high error-correction power of Polar codes with list-CRC decoding jointly enhance the communication capabilities of wireless sensor networks (WSNs) based on SDR. The algorithm is also beneficial for other SDR applications where custom hardware is not justified, but throughput of the order of tens of Mbps is required. A really speedup as compared to the LLR-based list-SC decoding is presented as a result of algorithm reformulation, Fast-SSC approach, derivation of a general path metric, and the application of unrolling techniques.

Y. Ren et al. in "A Sequence Repetition Node-Based Successive Cancellation List Decoder for 5G Polar Codes: Algorithm and Implementation" describe developments of an efficient SR-List decoding algorithm and hardware so that low latency and high-reliability requirements in 5G communication systems can be met. Improving the algorithm and concentrating on hardware implementation are done in this study, which is based on previously published universal SR-List decoding methods, to further improve performance. The existing node-based SCL decoders in [4] are hindered in their further reduction of the decoding time due to their inability to properly decode a wide class of constituent codes. The solution of the SR node structure of splitting into 0 and 1 rated parts, which is followed by ML decoding and Wagner-based list decoding through merged or reduced internal processes. The study of 5G New Radio polar codes allows constraints to be established on special node types, thus allowing a reduction in decoding latency and computational load.

The optimized algorithm is integrated with latency reduction tricks for path update and node traversal. Node based SCL decoder is compatible with 5G new radio polar codes was used as a reference for the implementation of hardware. The above methodology is applicable for multi-level decoding. These methods are joined so as to reduce log-likelihood ratio memory requirements and computation delay. The proposed efficient architecture for SR List decoding increases hardware efficiency by repurposing some modules. A unique approach to rank ordering reduced the area by 45% compared to one with a full rank order sorter, thus improving maximum clock frequency. The results indicate that the SR-List decoder, with a list size of L=8, achieves the throughput of 2.94 Gb/s, whereas the area efficiency results in an impressive 6.70 Gb/s/mm2. Therefore, the optimized decoder represents a feasible solution for 5G NR applications due to improvements in throughput and area efficiency over polar decoders of a similar category. In addition to providing some conclusions on the implementation and exploration of the design space, the paper also describes the SR List decoding algorithm and SR List decoder architecture.

C. Xiong et al. in "A Multi-Mode Area-Efficient SCL Polar Decoder" present improvements on Successive Cancellation List (SCL), a methodology used for decoding polar decoders. The improvement is in terms of flexibility and area efficiency. The paper [7] discusses the decoding throughput and latency of polar codes must be increased while also noting the channel capacity achieved by those codes. A limited number of patterns are unveiled by the detailed analysis of the frozen location patterns in polar codes as per Approximate Maximum Likelihood (AML). Keeping the performance in different channel conditions, the CA-SCL decoder coupled with the LC-AML unit yields a much better trade-off in area efficiency when compared to the SCL decoder that is being implemented usually. Multimode operation, by providing a flexible trade-off among latency, throughput, and error performance, puts emphasis on the necessity for low-overhead flexible communication. The study presents the benefits in flexibility and area efficiency of the proposed decoders by giving detailed information about the hardware implementation, along with synthesis results.

P. Giard et al. in "A multi-Gbps unrolled hardware list decoder for a systematic polar code" propose a hardware-based implementation of a high-throughput polar code decoder based on the SCL application, which deploys an unrolling technique. The polar codes are chosen by the next generation in mobile communications standards because of their capacity to fix errors into codes of small to moderate lengths that can be SCL decoded. The implementation presented in the paper [8] utilizes an SCL decoder with high latency and low throughput. With the presented results, error correction performance was proved to supersede with low density parity check from IEE 802.16e standard protocol. An exhaustive presentation of the adaptation of a totally unrolled pipelined hardware architecture for the SCL decoder is given. In contrast to standard decoders, it is much more of a high-throughput architecture in that all operations are instantiated in hardware, and data are allowed to flow with very little control. For minimum latency, the Fast SSC list decoding approach is used in the implementation, in which special units are employed for the decoding of smaller subcodes. The effect of quantization on error-correction performance is also studied in the paper [8], where it is found that a Qi.Qc.Qf = 6.5.0 configuration guarantees a coding loss of less than 0.25 dB. Finally, the proposed decoder significantly outperforms the SCL-based decoder with respect to both throughput and latency.

J. Lin et al. in "A High Throughput List Decoder Architecture for Polar Codes" has mentioned the existing CRC-aided SCL decoder, where the order of a code is 16384, uses list size L=4 & the proposed method, as per [9], called the Reduced Latency List Decoding Algorithm (RLLD) for polar codes, aims at improving throughput and decreasing decoding delay. Selective node visiting and considering a very limited number of possibilities for information bits are the

central innovations here, whereas classical SCL algorithms visit almost all nodes. The author has proposed such high throughput list decoder architecture which incorporates an index-based partial sum computation method for partial sum calculation to avoid direct copying of partial sums that can be detrimental to hardware implementation. A hybrid partial sum is introduced to store partial sums, which leads to significant area optimization savings over registers. Additionally, a unit has been developed to efficiently identify more reliable decoding paths for the implementation of RLLD algorithms. The major advantage of the RLLD algorithm, it visits fewer nodes and assumes fewer information bit possibilities than an existing SCL decoding algorithm. The paper contains descriptions of the algorithm, architecture, and advantages of the proposed architecture.

S. A. Hashemi et al. in “A Fast Polar Code List Decoder Architecture Based on Sphere Decoding” has presented a code length restriction imposed on the so-called ordinary polar codes. This paper [17] defines an RCPP, which represents a new era in channel coding. Polar codes have poor performance at short lengths, even though theoretically under SC decoding, they can yield channel capacity. It has been shown that concatenating polar codes with CRC codes and decoding using SCL or SCS can convincingly outperform traditional turbo and LDPC codes. However, the practical applications of polar codes are limited by the restriction that their lengths must be powers of two. The RCPP codes circumvent this restriction by utilizing puncturing and constructing codes of arbitrary lengths. Different from random puncturing techniques, the article details a Quasi-Uniform Puncturing (QUP) algorithm for producing puncturing tables and claims it has better row-weight properties. The authors have analytically proved that QUP results in a minimum row weight that is greater than the average of the minimum row weight caused by random puncturing. A system model is presented to illustrate the RCPP coding scheme consisting of CRC concatenation, polar encoding, puncturing, and CRC-aided SCL/SCS decoding. Also, the effect of puncturing on subchannel reliability is taken into consideration, whereby channel reliabilities are suggested to be recalculated using Gaussian approximation, density evolution, or the Tal and Vardy method. The simulations also illustrate the performance of the proposed RCPP codes against turbo codes in WCDMA and LTE wireless communication systems over BI-AWGN channels. The results substantiate that RCPP codes can perform better than their turbo code counterparts, especially with shorter code lengths, in terms of BLER.

L. Johannsen et al in “Parallel Single Parity Check Nodes for High-Throughput Fast-SSCL Polar Code Decoders” address two improvements to overcome the disadvantages of present-day SCS polar decoders. Such decoders were better than SC decoders while still having very high space complexity and high time complexity, and low SNR. The first is the Segmented CRC-aided SCS (SCA-SCS) decoder. Inspired by partitioned and segmented SCL algorithms, this innovation makes use of segmented parity checkers. The price the adaptive SCS decoder must pay is adaptive than the stack depth and the search width. A channel estimator that dynamically selects an appropriate decision criterion based on SNR is proposed. The SCA-SCS decoder brings about a 10.8% reduction in time complexity and a 31.68% reduction in space complexity, while ASCS shows an 11.42% time complexity reduction for average Gaussian noise channels. The paper [20] was implemented and verified using 90nm and 65nm technologies, restricting its advantage with respect to existing solutions. The method aims to balance decoding performance with all Complexities area constrained in the application.

2.3. Low-Latency Decoding Techniques

G. Coppolino et al. in "Efficient Operation Scheduling in Successive-Cancellation-based polar decoders" has presented two novel techniques to optimize the operation scheduling for successive cancellation-based polar decoders to reduce decoding latency in an utmost manner. Being capacity-achieving codes, polar codes have come to be used in the 5G wireless system. The original SC algorithm for decoding has comparatively lengthy latency for lower complexity, thereby providing a motivation for latency reduction techniques. Using Early g computation, the first technique exploits the inherent data dependency in the SC algorithm so that part of the g operation can be carried out in parallel with the preceding comb operation. This is possible because part of the comb operation generates an intermediate result that is directly used in the g operation and hence can be pre-computed. Such an optimization is especially beneficial in scenarios with a low number of PEs. The second method, called "g branching," targets underutilization of PEs at the lower stages of the decoding tree. The method in paper [3] exploits an abundant PE pool to speculatively compute the g operation on both 0 and 1 values of its l input. The selection of the correct value is performed after the determination of the l value by the comb operation. This increases the number of multiplexers but reduces latency significantly when the number of PEs increases. The paper elaborates on implementation considerations for each technique and potential latency reductions, giving analytical expressions to gauge reductions in clock cycles. Together, these two techniques bring latency savings between 15.79% and 33.34%, depending on the decoder parameters and code length. The proposed optimizations may be applied to various SC-based decoder architectures, including those implementing the Fast-SSC and SC-List algorithms. The authors emphasize that the additions incur minimal hardware cost, making them feasible for integration into real-world decoders.

O. Afisiadis et al. in "A low-complexity improved successive cancellation decoder for polar codes" of revolutionary, high-throughput VLSI architecture for list successive cancellation decoding of polar codes is presented

in this work [16], intended particularly for implementations with varying list sizes (L=8, 16, and 32). These works aim to address the high computational complexity bottlenecks in consecutive cancelation decoding while factoring in the intricacies of list management and the limited practical use of LSCD in latency-sensitive applications. At the algorithmic level, the authors propose two optimizations. The first solution adopted to reduce the latency of the LM module is a multi-bit double thresholding approach. MB-DTS, by leveraging multi-bit decoding, double thresholding, and selective expansion, avoids the full tree traversal required by traditional DTS and enables simultaneous decoding of multiple bits within a sub-tree. Second is the partial G-node look-ahead in SCD cores. P-GLAH attempts to balance the benefits of latency reduction provided by G-node look-ahead against the hardware overhead that is generated in the original GLAH approach. This paper presents the VLSI architecture for given algorithms, and it provides special optimizations for the programmable PEs and PMU block to reduce the critical path delay. With an aim to further reduce latency, critical path optimization is also applied. The proposed architecture includes LLR memories, PE arrays, a crossbar network, a partial-sum network, and path memories. Pointers in a lazy copy scheme have been used to minimize data movement. Implementation results display throughputs of 1.103 Gbps, 977 Mbps, and 827 Mbps for list sizes 8, 16, and 32, respectively. The proposed architecture would allow a gain in throughput and area efficiency in implementations of LSCD, particularly for large list sizes. Through simulations, the authors show that this architecture gives good error correction performance.

W. Song et al., "Efficient Successive Cancellation Stack Decoder for Polar Codes" present an innovative partitioned sorting network to enhance the efficiency of metric sorters in Rate-1 and single parity check decoders used for quick list decoding of polar codes. The primary issue under consideration is the high complexity of sorters required in simultaneous bit decoding in Rate-1 and SPC nodes, which is a technique aiming for enhancement in error correction and decrease in latency. The sorting process is separated in two different networks by the proposed PSN. The analysis in paper [18] of Path Metric (PM) ordering plays the role of the first sorting network to trim down the number of input candidate paths. By studying the inherent properties of path metrics and borrowing from concepts of minimum-combination sets, the first stage efficiently reduces less-promising paths, hence lessening the processing load on the later stages. The second sorting network uses the outcome of cumulative path selection analysis. It is found that some paths are selected more frequently than others, hence the frequent ones can be duly marked down, and the sorting complexity reduced accordingly. The paper presents the effectiveness of the PSN through hardware implementation and its comparison with other existing sorting network architectures. The results further show increasing gains, as the proposed PSN reaches operating frequencies higher by 137% and possesses 90% fewer compare and swap units when working with Rate 1 and SPC decoders of list size (L) 8 compared to the traditional design. This proves to be a major accomplishment in fast list decoding, as the metric sorter is most often the component in the decoder that defines the overall working frequency. Korean research and development programs have funded the initiative.

B. Yuan et al. "Early Stopping Criteria for Energy-Efficient Low-Latency Belief-Propagation Polar Code Decoders " describes how to improve the throughput without affecting the performance. This work [19] presents a speed-up technique for the list sequential cancellation decoding of polar codes. The basic philosophy behind this technique is to use the SCL architecture to exploit simplified decoding algorithms for certain constituent polar codes: Rate 0, Rate 1, Repetition (Rep), and Single Parity-Check codes. The algorithm is exact for list sizes of two and introduces some approximations for larger list sizes for a very insignificant effect on performance-less than 0.05 dB. The method further enhances the Simplified SC (SSC) and Fast-SSC framework by incorporating knowledge gained from List Sphere Decoding (List-SD). The study demonstrates that PM computations can be simplified to decode Rate-0 and Rep codes efficiently. For Rate-1 codes, an optimal decoder based on List-SD is proposed that allows faster decoding than conventional SCL. Further, a suboptimal decoder for SPC codes is proposed, which use a matrix reordering concept to improve the speed with little compromise on error-correction performance. A decoder architecture is created under constituent code optimizations. This decoder architecture is built upon CRC-aided SCL decoders with specialized units for each code type. Depending on the design intent to maximize latency, frequency, or complexity, final design decisions, such as different adder tree architectures, are made for Rate-0 and Rep nodes. The special nodes are shortlisted and then identified to perform offline, information utilized by the decoder control unit. With a view toward a short critical path and maximum parallelism. The implementation results in TSMC 65 nm CMOS technology to give massive improvements in throughput (by a factor of 3.16), with reasonable area overhead (14.2%). Error-correction performance curves validate minimal degradation caused by the SPC approximation. Comparisons with state-of-the-art decoders hence demonstrate a worthy trade-off among area, throughput, and latency, thus making the suggested architecture worthy for high-performance polar code decoding.

2.4. Alternative Codes and Schemes

C. Condo et al. “Blind Detection with Polar Codes” an Enhanced technique of polar codes using successive cancellation decoding is presented in [11] which primarily aims to reduce latency by implementing fast parallel decoders. This study builds on Arikan's discovery of polar codes and their capacity-achieving nature, and also builds up on previous

works toward improving the speed of SC decoding through simplified-SC and fast-SSC decoders. The throughput is limited because of SC decoding in the serial structure and inherited computational complexity. The authors define five new constituent codes: Type-I, Type-II, Type-III, Type-IV, and Type-V nodes, all of which correspond to different frozen-bit patterns in the polar code structure. For each type of node, a fast decoder is then described, which exploits the distinctive properties of its frozen-bit pattern to facilitate parallel processing and reduction of computational complexity, specially designed for binary-input symmetric memoryless channels. The proposed decoder can perform well in both scenarios, systematic and non-systematic polar codes. The paper provides theorems and proofs describing key inter-bit relations within each node type, which are then used to build fast decoders. The Wagner decoding approach is used to estimate the decoded bit efficiently. Performance is evaluated via bit-error rate and block-error rate simulations, revealing that the proposed decoder tracks error rates and performance similar to the fast SSC and standard SC ones. The comparison with respect to latency which aims to reduce the number of clock cycles that have to be run compared to that of the present fast SSC decoders. Latency is calculated with the hardware implementation taken into consideration, counting additions/subtractions, check-node, and Wagner decoding operations. The implementation results demonstrate that the speed of decoding in polar codes improves the error rate performance, which is needed in low-latency communication.

S. A. Hashemi et al. "Matrix reordering for efficient list sphere decoding of polar codes" unlocks polar codes with a new approach, which increases throughput and area efficiency by forming Successive Cancellation List (SCL) and symbol-decision Successive Cancellation (SC) decoders. The outline gives symbol decisions from symbol-wise channel transition probabilities by combining recursive channels. The aforementioned approach is a simple combination of bit-wise channel transition probabilities and, therefore, becomes a little less complicated.

The proposed method in [13] has some similarities to Arikan's channel transformation; hence, based on these commonalities, resources can be shared for an efficient hardware implementation to keep symbol-decoding complexity under control and a two-stage list network. Hence, performance in error is traded against decoder complexity in that network. This methodology aims at reducing the memory demand without degrading the speed of execution. A detail of the semi-parallel SCL decoder is introduced to evaluate the symbol decision decoder. The architecture is explored and implemented for different symbol sizes, and sorting is proposed for performance optimization. Compared to the also-bit and symbolic-decision SCL decoders, the suggested results of the paper show a smaller area. The algorithm for symbol-decision decoding is based on the special symbol-wise recursive channel transition method.

K. Niu et al in "Beyond turbo codes: Rate-compatible punctured polar codes" note that such matrix reordering techniques augment the List-sphere decoding (List-SD) technique for polar codes by trading off hardware complexity and error correction performance. Polar Codes, which can achieve capacity on memoryless channels, base their principle on the realization of an efficient decoding algorithm. List-SD has surfaced as an alternative in place of the short polar codes employed as the components in the larger codes. The entire frozen-bit placement arrangement is adjusted using the reordering procedures in (LIST-SD) and is therefore vital for path metric calculations. Under a lesser BLER than turbo codes, the RCPP code benefits from CRC-aided SCL/SCS decoding. The frozen bit placement is aligned by this method with the List-SD decoding direction, thus making the List-SD capable of exploiting this alignment.

The efficiency of the reordering technique is supported through both performance results and hardware implementation. The FER and BER curves show that matrix reordering improves List-SD performance by up to 0.75 dB while complexity (list size) remains the same. In addition, the reordering List-SD is capable of attaining the same error correction performance with a smaller list size, which makes the implementation computationally less expensive. According to hardware synthesis on a Xilinx Virtex-7 FPGA, matrix reordering can preserve the same FER and BER performance as the original List-SD, but, at the same time, it reduces the LUT consumption by 69% and register usage by 50%. Therefore, the authors conclude that the proposed method [14], by exploiting the structure of the generator matrix and by optimizing the decoding order, significantly improves the error correction performance and hardware efficiency of the List-SD algorithm. The literature analysis of various research work as shown in Table 1.

3. Algorithmic Enhancements

The literature uncovers several recent developments in algorithmic improvements for polar code decoding. Methods like Fast-SSCL and Fast-SSCL-SPC [2, 20] optimally reduce path extensions in SCL decoders by opportunistically exploiting special node structures such as rate-one and single-parity check nodes. They are optimized for faster decoding in no way compromising the error correction capabilities. Likewise, with early g-computation and g-branching [3], the sequential bottleneck can smoothly be removed from SC decoding by partial parallelism. PAC codes [5], which include the combination of precoding with convolutional coding, have also attained a significant reduction in decoding latency by exploiting inverse convolutional encoding for special treatment of nodes. These are very much simplified ways of decoding.

3.1. Hardware Architectures

In most of the literature, hardware implementations are considered to accelerate decoding. The pipelined and unrolled

architectures proposed in [1, 8] offer high throughput by parallel mapping of decoder logic onto hardware with simultaneous data flow within the latter. High-speed implementations such as the 10-Gbps decoder of [8] and very low-power VLSI implementations of [17] demonstrate the hardware viability of these proposals. On the other hand, approximate ML decoders [13] and resource-sharing approaches [4] may compromise on power and area to go on without compromising on performance. Architectural flexibility is also one concern of multimode decoders [7] that provide trade-offs between speed, area, and reliability. Polar decoding architecture and algorithmic improvements, as shown in Figure 1.

3.2. Low-Latency Techniques

Algorithms for the reduction of latency run through a spectrum of pruning strategies at the algorithm level to architecture-friendly optimizations. Less Latency List Decoding (RLLD) reduces memory and computational loads by considering fewer paths to explore. Symbol-decision decoding [12] and node-level pruning in PAC-based decoding [5] reduce latency by skipping unnecessary operations. Fast-SSC-based unrolled decoders [1] increase decoding speed by a factor of 10. Multi-bit decoding [20] and sorter optimizations based on path metrics [2] contribute to reducing decoding latency. Such advancements enable the realization of real-time requirements for 5G and future communication systems.

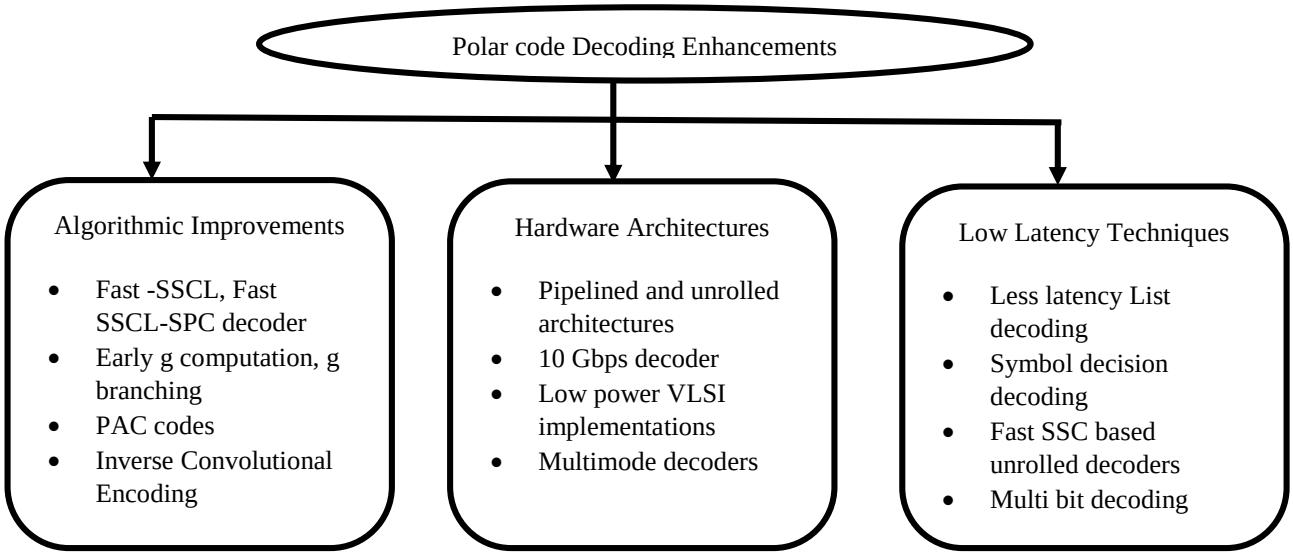

Fig. 1 Polar code architecture

3.3. Comparative Analysis with Existing Survey

The survey distinguishes mostly in two aspects. First, while [21, 4] focuses exclusively on SCL-based decoders suitable for 5G NR, the present work extends coverage to PAC codes, symbol-decision decoding, and optical, GNSS domains. Second, the structured mapping in Table 1 provides a standardized gap-and-future-work analysis for 24 papers, offering researchers a systematic basis for identifying unexplored directions.

4. Methodology and Research Objectives

4.1. Methodology

To provide a thorough survey of the field, this review has structured a rigorous methodology for selecting literature, consistent with Scopus-indexed journal standards. Relevant publications were identified through academic databases such as IEEE Xplore, arXiv, and Scopus. The following inclusion criteria were considered:

1. Concerned with polar code decoding techniques, including Successive Cancellation (SC), Successive Cancellation List (SCL), and CRC-aided decoding.
2. Concerned with algorithmic improvements, hardware implementations, or low-latency decoding strategies.
3. Publications of the last ten years to maintain cutting-edge relevance.
4. Preference for peer-reviewed journal articles and proceedings from highly impactful conferences.

Such a methodology ensures that the works analyzed are both technically relevant and academically sound to lay a solid foundation for an analysis of current trends and directing the future of polar decoding research.

4.2. Research Gaps Identified

The review shall be structured around the following major objectives that pertain to the pragmatic and theoretical challenges involved in the design of forward error correction (FEC) systems for next-generation communication platforms in satellite transmission scenario. These objectives are listed in the Table 2 below:

Table 2. Research gaps

Sl. No	Research Gap
1	Existing studies largely focus on terrestrial channels, with insufficient domain-specific evaluation of advanced FEC schemes under GNSS and optical satellite channel impairments.
2	Despite their performance advantages, GF(3^m)-LDPC codes face challenges related to decoding complexity, memory usage, and hardware implementation cost.
3	Polar codes are well studied, but their potential advantages over LDPC and Reed–Solomon codes in GNSS and optical satellite communication remain underexplored.
4	There is a gap in comprehensive comparative studies that jointly assess error performance, latency, area, and energy efficiency across LDPC, RS, and polar codes.

These research gaps, therefore, present and establish the foundation for analysing current trends and missing links of polar code research, further guiding the classification of advances in terms of algorithmic techniques, hardware designs, and latency reduction. The survey analysis of LDPC and polar Code as shown in in Table 3.

Table 3. Comparison of LDPC and Polar codes

Feature	LDPC Codes	Polar Codes
Construction	Sparse parity-check matrices	Channel polarization-based structures
Decoding Complexity	Iterative message passing (BP, SPA, Min-Sum)	Successive Cancellation (SC) and Successive Cancellation List (SCL) decoding.
Performance	Excellent near-Shannon performance; strong for large block lengths	Capacity-achieving asymptotically; needs improvement for short block lengths
Hardware Implementation	Well-established; highly parallelizable	More sequential, but improving via Fast-SSC, unrolling, and parallel SC
Applications	Wi-Fi, DVB-S2, 5G NR data channels, storage systems	5G NR control channels, GNSS, optical satellite links

5. Conclusion

While LDPC codes are best tuned for applications involving high throughput of data, polar codes have several unique advantages, making their preferred types for GNSS and optical satellite links:

With low complexity decoders (SC, SCL), polar codes are the first codes which theoretically attain the Shannon limit. This benefit is pronounced on large, clean channels like GNSS.

Low latency: With recent improvements in decoding techniques, such as Fast-SSCL decoding, early stopping for SCL, and pruned tree traversal, polar codes even compete with LDPC in real-time implementations.

Hardware efficiency: Greatly enhanced with recent studies about unrolled architectures and approximate ML units, polar codes become super area- and energy-efficient on FPGA and ASIC implementation.

Flexibility: Polar decoders can be adjusted to different list sizes and modes of decoding, therefore rendering them good candidates in heterogeneous systems that include GNSS receivers or optical payloads.

With these developments in mind, this survey favours the study and implementation of polar codes further, especially in low-power, highly reliable, and real-time communication systems, including GNSS signal protection and error correction in optical satellite networks.

Conflicts of Interest

The authors declare that they have no conflicts of Interest in the publication of this work.

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Appendix

Table 1. The comparative table of the survey

SL.NO	TITLE	AUTHOR	METHODOLOGY	LIMITATIONS	RESEARCH GAPS	FUTURE WORK
1	Unrolled Polar Decoders, Part II: Fast List Decoders	Sarkis et al.	Unrolled Fast-SSCL hardware architecture	Area and power overhead of unrolling	Scalability to larger code lengths	More energy-efficient implementations
2	Sequence Repetition Node-Based SCL Decoder for 5G Polar Codes	Ren et al.	Specialized node processing with hardware implementation	Complexity for diverse node types	Support for broader polar configurations	Adaptive node-based architectures
3	A Multi-Mode Area-Efficient SCL Polar Decoder	Xiong et al.	Multi-mode area-optimized SCL architecture	Trade-off between flexibility and performance	Dynamic runtime reconfiguration	FPGA-oriented multi-mode decoders
4	A Multi-Gbps Unrolled Hardware List Decoder for a Systematic Polar Code	Giard et al.	Fully unrolled pipelined list decoder	Large hardware footprint	Power-performance optimization	Portable FPGA/ASIC implementations
5	A High Throughput List Decoder Architecture for Polar Codes	Lin et al.	Reduced-latency list decoding architecture	Memory and routing complexity	Further throughput scaling	Advanced FPGA optimization
6	A Fast Polar Code List Decoder Architecture Based on Sphere Decoding	Hashemi et al.	Sphere-decoding-inspired list architecture	Implementation complexity	Low-power realization	ASIC/FPGA co-optimization
7	Parallel Single Parity Check Nodes for High-Throughput Fast-SSCL Polar Code Decoders	Johannsen et al.	Parallel SPC-node processing for Fast-SSCL	Additional hardware resources	Integration with complete decoder pipelines	Ultra-high-throughput FPGA decoders
8	On Error-Correction Performance and Implementation of Polar Code List Decoders for 5G	Ercan et al.	Performance and implementation study of list decoders	Limited to evaluated configurations	Broader hardware comparison	5G-oriented FPGA implementations
9	Fast and Flexible Successive-Cancellation List Decoders for Polar Codes	Hashemi et al.	Fast-SSCL algorithmic improvements	Still sequential in parts	Greater parallelism	Lower-complexity variants
10	Efficient Operation Scheduling in Successive-Cancellation-Based Polar Decoders	Coppolino et al.	Operation scheduling optimization	Scheduling overhead	Dynamic scheduling strategies	Runtime-adaptive schedulers
11	Simplified Successive Cancellation List Decoding of PAC Codes	Saber et al.	Low-complexity PAC decoding	PAC-specific assumptions	Generalized PAC decoding	Hybrid PAC-polar decoders
12	Efficient Bit-Channel Reliability Computation for	Condo et al.	Reliability computation optimization	Focused on reliability estimation	Integration with adaptive decoding	Dynamic reliability management

	Multi-Mode Polar Code Encoders and Decoders					
13	LLR-Based Successive Cancellation List Decoding of Polar Codes	Balatsoukas-Stimming et al.	LLR-domain SCL decoding	Memory and path-management overhead	Further complexity reduction	Efficient fixed-point implementations
14	Blind Detection with Polar Codes	Condo et al.	Blind detection using polar coding	Application-specific focus	Broader deployment scenarios	Integration with 5G procedures
15	Symbol-Decision Successive Cancellation List Decoder for Polar Codes	Xiong et al.	Symbol-level SCL decoding	Symbol-size design trade-offs	Adaptive symbol decisions	Low-latency symbol decoders
16	Matrix Reordering for Efficient List Sphere Decoding of Polar Codes	Hashemi et al.	Matrix-reordered list sphere decoding	Complexity of reordering	Automated optimization	Hybrid decoding frameworks
17	Beyond Turbo Codes: Rate-Compatible Punctured Polar Codes	Niu et al.	Rate-compatible punctured polar codes	Puncturing performance loss	Improved puncturing patterns	Adaptive rate-compatible schemes
18	CRC-Aided Decoding of Polar Codes	Niu and Chen	CRC-assisted SCL decoding	CRC overhead	Optimal CRC selection	Adaptive CRC strategies
19	A Low-Complexity Improved Successive Cancellation Decoder for Polar Codes	Afisiadis et al.	Complexity-reduced SC decoding	Performance gap vs SCL	SC performance enhancement	Hybrid SC/SCL approaches
20	Efficient Successive Cancellation Stack Decoder for Polar Codes	Song et al.	Stack-based SC decoding	Variable decoding latency	Latency predictability	Adaptive stack management
21	Early Stopping Criteria for Energy-Efficient Low-Latency Belief-Propagation Polar Code Decoders	Yuan and Parhi	Early stopping for BP decoding	Risk of premature stopping	Robust stopping rules	Channel-aware stopping criteria
22	Reduce the Complexity of List Decoding of Polar Codes by Tree-Pruning	Chen et al.	Tree-pruning in list decoding	Potential performance loss	Optimal pruning policies	Adaptive pruning strategies