# Method of Improving Power Quality Using FPGA with SAPF in Power Systems

K.Hemachandran[1], P.Nishanth[2], Dr.B.Justus Rabi[3], Dr.S.S.Darly[4]

[1]*Research Scholar,* [2]*Student,* [3]*Principal,* [4]*Associate Professor*
[1,2]*Dr.MGR Educational & Research Institute University, Chennai, India*
[3]*Shri Andal Alagar College Of Engineering, India*
[4]*University College of Engineering and Technology, thindivanam, India*

***Abstract*** *— Maintaining correct power quality is being a very important task within the operation of the facility. It's compelling by the ability quality standards (IEEE-519) to limit the harmonics distortion at intervals the suitable vary. The excessive use of power electronics devices in distribution system has evolved the matter of power quality leading to harmonics generation & in substantial economic losses. Filters approaches to be the effective & economical technique for harmonics mitigation. This paper presents the method of using FPGA controller in the place of Hysteresis current controller for controlling the shunt active filter to mitigate the harmonics in power systems. Harmonics identification methodology and compensation management adopted are mentioned.*

**Keywords** *— Field Programmable Gate Array, Harmonics, Shunt Active power filter.*

## I. INTRODUCTION

With the increasing energy demand, power quality is one in all the key constraints in facility transmission & distribution. Power quality is essentially the standard of the voltage [14] & [15]. Because of the advancements within the semiconductor technology & the proliferation of the power electronics devices or non linear loads in power distribution systems, the vulnerability of such equipments to power quality issues has exaggerated. The non linear load together with saturated transformers, arc furnaces, and converters for as drives, SMPS & therefore on draw non sinusoidal current from the utility & generate harmonics [1].

Basically, two approaches for the mitigation of power quality issues are load conditioning & line conditioning. During which line conditioning is found to be higher because it becomes troublesome to try to made equipments less sensitive to harmonics. In line conditioning, the system is put in at the purpose of common coupling that suppress for the results created by the non linear-loads. To reduce the effects of harmonics, though there's a accessibility of various technical choices however filters have established to be a viable solution to eliminate harmonics [2].

Traditionally, passive filters are used to mitigate harmonics. Though with varied benefits likes implicitly, simple to implement, produce system resonance cheaper, the passive filter suffer from several disadvantages like standardization problem, fa stened compensation characteristics & their large size. Active filters avoid the drawbacks of passive filters however its performances depend upon the power rating & speed of response [3]. Hybrid filters are planned to mitigate the issues of active & passive filters. It provides value effective & sensible harmonic compensation approach for prime power non linear loads [11] & [12].

Various harmonics detection techniques were adopted to control the power circuit of the active filter. This paper presents FPGA controller is used in place of Hysteresis current controller for controlling the active filter to mitigate the harmonics. Program were written in VHDL and implemented into Spartan 3E using Xilinx ISE. FPGA controller provides better results than those of the traditional methods [4].

## II. SELECTION OF FILTERS

Table.1 gives a proper selection of active filter for all power quality disturbances. Since nowadays many industries are manufacturing active filters [1], [3] & [7].

**Table 1.** Selection of Filters for Harmonic

| S.no | Compensation for particular Application | Active Series | Active Shunt | Hybrid of Active Series and Passive Shunt | Hybrid of Active Shunt and Active Series |
|---|---|---|---|---|---|
| 1 | Voltage Harmonics | XXX | | XX | X |
| 2 | Current Harmonics | | XX | XXX | X |
| 3 | Current harmonics & Reactive power | | XXX | XX | X |
| 4 | Current harmonics, | | XX | | X |

| | | | | | |
|---|---|---|---|---|---|
| | Reactive power & Load Balancing | | | | |
| 5 | Current harmonics, Reactive power, Load Balancing & Neutral Current | | X | | |
| 6 | Voltage Harmonics & Voltage Regulation | XX | | | X |
| 7 | Voltage Harmonics, Voltage Regulation, Voltage Flicker & Voltage Sag & Dips | XX | | | X |
| 8 | Current Harmonics & Voltage Harmonics | | | XX | X |
| 9 | Current Harmonics, Reactive Power, Voltage Harmonics, Voltage Regulation | | | X | XX |
| 10 | Current Harmonics, Reactive Power & Voltage Balancing | | XX | X | |
| 11 | Current Harmonics & Load Balancing | | X | | |
| 12 | Current Harmonics, Neutral Current | | X | XX | |

*AF Configuration with higher number of "**X**" is more preferred

## III. Synchronous Reference Frame Controller

The synchronous system theory or d-q theory is predicated on time-domain reference signal estimation techniques. It performs the operation in steady-state or transient state in addition as for generic voltage and current waveforms. It permits dominant the active power filters in real time system [2]. Another necessary feature of this theory is that the simplicity of the calculations, that involves solely algebraic calculation. The essential structure of SRF controller consists of direct (d-q) and inverse (d-q) -1 park transformation as shown in Fig1. This could be helpful for the valuation of a particular harmonic element of the input signals.

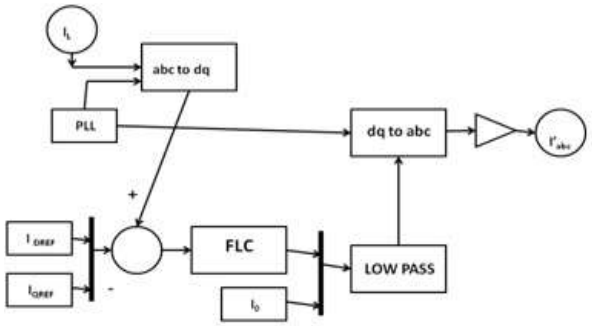


**Fig 1:** Synchronous d-q-0 Reference Frame

The d-q transformation output signals depend upon the load current (fundamental and harmonic components) and therefore the performance of the phase locked Loop (PLL). The a-b-c to d-q-0 transformation is shown in fig 2. The id-iq current is shipped through low pass filter (LPF) for filtering the harmonic elements of the load current that permits solely theelemental frequency elements [9]. The LPF could be a second order Butterworth filter, which's cut off frequency, is chosen to be fifty cycle for eliminating the upper order harmonics. The FLC controller is employed to eliminate the steady state error of the DC element of the d-axis reference signals. Further more, it maintains the electrical device voltage nearly constant. The DC-side electrical device voltage of PWM-voltage supply electrical converter is detected and compared with desired reference voltage for calculative the error voltage. This error voltage is skilful a PI controller whose propagation gain (KP) and integral gains (KI) are 0.1 and 1 respectively [6].

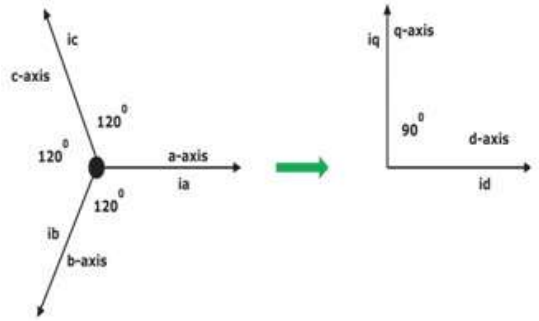


**Fig2:** a-b-c to d-q-0 Transformation

## IV. Hysteresis Current Controller

In hysteresis Current control, two fastened hysteresis b ands are outlined so that reference current are going to be right within the middle of the two bands that have a awfully high dynamic response and are inherently stable [4]. Once the measured current hits the higher or lower band, shift can happen consequently. The present and voltage wave with hysteresis current controller (HCC) are shown in Fig 3. The PWM frequency varies inside a band as a result of peak-to-peak current ripple is needed to be controlled in the least points of the basic frequency wave [2] & [10].

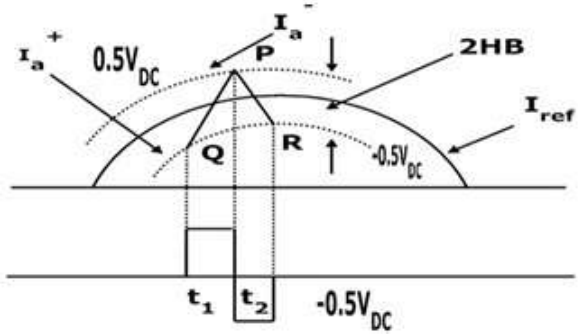


**Figure 3:** Current and Voltage Waveform with HCC

For each part the two-level PWM voltage supply electrical converter systems of the physical phenomenon current controller are utilized severally. The change signal of the 3 phases is generated directly by current controller [9]. The error current is that the distinction between the required reference current $i_{ref}$ (t)and the particular supply current $i_{actual}$(t) .If the error current exceeds the higher physical phenomenon band limit (+h), the higher switch of the electrical converter arm becomes OFF and also the lower switch becomes ON .

The switching logic for phase b and phase c is similar to phase a, using corresponding reference and measured currents and hysteresis bandwidth (HB) and is shown in Fig 4.

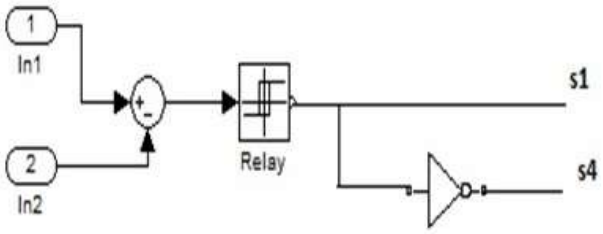


**Fig 4:** Hysteresis Current Controller

## V. Control Strategies

### A. *Block Diagram Representation*

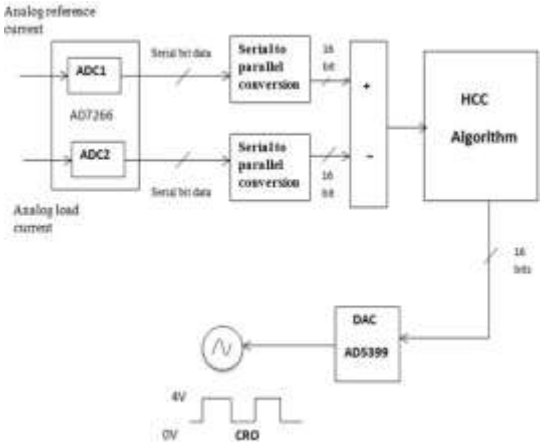


**Fig 5:** Digital Implementation of HCC

### B. *Algorithm*

**Step1:** declare the following inputs – clk (clock), rst (reset), douta and doubt (serial outputs of ADC); declare the following outputs –cs (chip select), a0,a1,a2(channel select), sclk (serial clock)

**Step2:** assign sig=0000, sigl=000 which represents the different states of DAC and ADC. Assign j1=j2=0000 0000 0000 00 which are buffers of 14 bit to get the serial output of ADC.

**Step3:** if rst=1, then set sig as 0000, i.e. move to the first state of ADC

**Step4:** else select the channel 1. sig=sig+1 i.e. move to the next state of ADC

**Step5:** if sig= 0000(i.e. the 1st state), disable the ADC chip AD7266 and set high to sclk

**Step6:** if sig=0001(i.e., the 2nd state), enable the chip AD7266. Set the high to sclk. Concatenate 13 bits (from LSB) of j1 with the douta and 13 bits (from LSB) of j2 with the doutb.

**Step7:** if sig=0010 (the 3rd state), set the low to sclk. Go to the previous state until clock count reaches the value 14. Thus the buffers have the 14-bit output (12 data bits with two preceding zeros) from ADC.

**Step8:** if sig=0011(the 4th state), then set the high to sclk. Disable the chip AD7266. Add x"0800"

with buffer j1 since the buffer value is unsigned and prefix two zeros to the resultant value. Let it be a_data. Do the same with j2. And let it be b_data.

**Step9:** if sig=0100(the 5th state), then prefix "0000" with the 12 LSB bits of a_data and it is digidata_a. do the same for b_data and name it as digidata_b.

**Step10:** In other cases, sig=0000 i.e. move on to the 1st state.

**Step11:** compare the processed 16-bit outputs of ADC (digidata_a and digidata_b) and find the error.

**Step12:** compare error signal with hysteresis band. If error is greater than upper hysteresis band then, set the input to DAC as sdi=0000 0111 1111 1111(4V).

**Step13:** If error is less than lower hysteresis band then, set the input as sdi=0000 1000 0000 0000(0V).

**Step14:** assign sdi as the input of DAC (AD5399) the sdi (serial data input) is the format of input to the ADC in which the MSB is address bit select one of the two DACs, next bit is don't care bit, next is shut down bit, and the next bit is 0 always.

**Step15:** give for each result a duration of 14 clock cycles.

**Step16:** checkout the output waveform in CRO [10].

### *C. Behavioural Simulation of Digital HCC*

The RTL Schematic of Digital HCC is shown in Fig 6. The behavioural model simulation for HCC using Xilinx is shown in Fig 7. a0, a1 and a2 represent the channel selection to be 0. Hence two ADCs are selected. For simulation purpose, the outputs of ADC, output pin DOUTA and DOUTB are assumed.

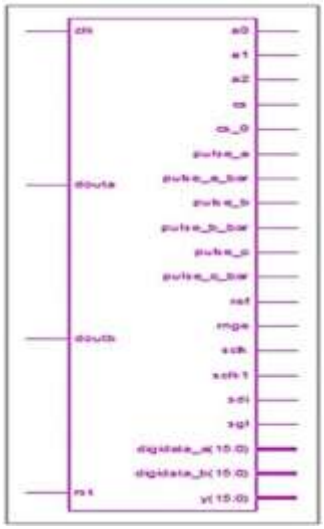

**Fig 6:** RTL Schematic of Digital HCC

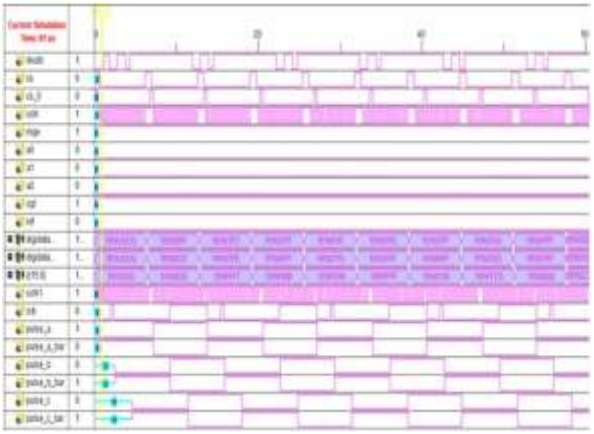

**Fig 7:** Behavioural Simulation of Digital HCC

This output is taken from the DOUTA and DOUTB pins simultaneously after 14 SCLK cycles. The digital outputs of both ADCs are used for generating the error signal. The error signal is represented by variable 'y'. The pulse_a, pulse_a_bar, pulse_b, pulse_b_bar, pulse_c, pulse_c_bar are the six output pulses as a result of digital HCC [8].

### *D. Program in VHDL for generating PWM signals*

```
entity counter_dataB is
Port (clk : in STD_LOGIC;
btn : in STD_LOGIC_VECTOR (1 downto 0);
rst : in STD_LOGIC;
data_outBcounter: out STD_LOGIC_VECTOR (7
downto 0)); end counter_dataB;
architecture Behavioral of counter_dataB is
signal countdatab : std_logic_vector(25
downto 0);
begin process
(clk,rst,btn)
begin
if (clk'event and clk='1')
then if rst= '1' then countdatab<=(others=>'0'); end if;
if((btn(1)='1') and (btn(0)='0') and
(countdatab<X"3FFFFFF")) then
countdatab<=countdatab+1;
end if;
if((btn(0)='1') and (btn(1)='0') and
(countdatab>X"0000000")) then
countdatab<=countdatab-1;
end if;
data_outBcounter <= countdatab (25downto18);
end if;
end process;
end Behavioral;
```

with this program the pwm signals are generated for switching the gates of the IGBT inside the inverter to reduce the harmonics present in the line current [13].

## VI. CONCLUSION

The paper conferred an economical & effective answer to power quality improvement. The bestowed techniques satisfactorily mitigate harmonics & maintain the supply current sinusoidal & meet the IEEE 519 normal recommendation. The harmonic filter includes PI & hysteresis controller. It revels from the reviews delineated within the paper that in the place of the Hysteresis controller FPGA controller has been used with SAPF for Harmonic detection and elimination. In future, FPGA are going to be a pre-eminent controller for Shunt Active Power Filter for power quality issues.

## REFERENCES


[1] C.Nalini Kiran, " Power Quality Improvement Using Active & Passive Power Filters", International journal of Modern Engineering Research (IJMER), Vol.2, Issue 1, pp-076-079.

[2] K.Hemachandran, Dr.B.Justus Rabi and Dr.S.Darly (2014), "Mitigation of Harmonics using Active Shunt Filter with PEMFC", Asian Journal of Applied Sciences,(ISSN: 2321 – 0893), Volume 02 – Issue 06, December 2014, pp-837-845.

[3] A Kannan, V Kumar, T. Chandrasekar, BJ Rabi, "A review of power quality standards, electrical software tools, issues and solutions", at renewable energy and sustainable Energy (ICRESCE) 2013 International conference, IEEE pages – 91-97.

[4] Anil Bharti, Rajat Varshney, Dr S.K.Srivastva, "A Study of PI Controller Based Unified Power Quality Conditioner" in International Journal of Advanced Research in Computer Science and Software Engineering, sept 2012.

[5] Uma P BalaRaju, Bala Krishna Kethineni, Rahul H Shewale, Shiva Gourishetti"Harmonic effects and its mitigation techniques for a non-linear load" International Journal of Advanced Technology & Engineering Research (IJATER), may 2012.

[6] S.Bhattacharya and D.Divan," Synchronous frame base controller implementation for a hybrid seris active filter system," in Conf.Rec.IEEE IAS Annu. Meeting, 1995, pp.2531-2540

[7] Joao L. Afonso, Mauricio Aredes, Edson Watanabe, Julio S. Martins, "Shunt Active Filter for Power Qaulity Improvement" International conference UIE, Lisboa, Portugal, November 2000, pp.683-691.

[8] Mehta.G, Singh S.P, Patidar R.D, Non-linear load compensation in fuel cell grid interfaced system using active power filter", at PEDS, 2011 IEEE Conf. ISSN: 2164-5256, pp-197-202.

[9] Shiuly Mukhehjee, Nitin Saxena, K.k.Sharma,"Power system harmonic compensation using shunt active power filter" IJERA, Vol.4 Issue 7, july 2014,pp.60-63.

[10] S.S. Darly, Dr.P. Vanaja Ranjan and Dr.B.Justus Rabi, (2011),"FPGA Based Series Active Filter For Power Quality Enhancement", International Electrical Engineering Journal (IEEJ), Vol.1, No.1, pp.506-513.

[11] K.Sarasvathi, R.Rajalakshmi, "Applications of Shunt active filter for multiple non-linear loads "International Journal of Advanced Engineering Applications, Vol.1, Iss.2, pp.27-36 (2012).

[12] Uma P BalaRaju, Bala Krishna Kethineni, Rahul H Shewale, Shiva Gourishetti"Harmonic effects and its mitigation techniques for a non-linear load" International Journal of Advanced Technology & Engineering Research (IJATER), may 2012.

[13] K.Hemachandran, B.Justus rabi, & S.Manivannan " PWM signals generation with inconsistent duty cycle using FPGA Spartan-3E" International Journal of Applied Engineering Research, Issn-09734562 vo.10, no.68 (2015).

[14] Amminuddin Ahmad, Pooja Jaglan " Compensation of Source Current Harmonics Using Shunt Active Filters", SSRG International journal of Electrical and Electronics Engineering (SSRG-IJEEE), Vol 1, Issue 5, (2014).

[15] Ladalla Anil, G.Poorna Chandar Rao,"Simulation of Unified Power Quality Controller for Enhacement of Power Quality by using ANN Controller", ", SSRG International journal of Electrical and Electronics Engineering (SSRG-IJEEE), Vol 1, Issue 9, (2014).