Review Paper on Reversible Multiplier Circuit using Different Programmable Reversible Gate

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Abstract - *Reversible logic circuits are increasingly used in power minimization having applications such as low power CMOS design, optical information processing, DNA computing, bioinformatics, quantum computing and nanotechnology. The problem of minimizing the number of garbage outputs is an important issue in reversible logic design. In this paper we have design 5×5 reversible logic gate using programmable reversible gate. We have used different types of programmable reversible gate i.e. Peres gate (PG) and HNG gate, PG and DPG gate, PG and full adder, PG and MHNG to construct the reversible fault tolerant multiplier circuit. We show that the 5×5 reversible multiplier circuit has lower hardware complexity and it is much better and optimized in terms of number of reversible gates and number of garbage outputs with compared to the existing counterparts.*

Keywords—*Peres Gate, Reversible Multiplier, Garbage Output, Quantum Cost*

I. INTRODUCTION

In present day VLSI framework power dissemination is high because of quick exchanging of inner signs. The multifaceted nature of VLSI circuits increments with every year because of pressing more rationale components into littler volumes. Subsequently control dispersal has turned into the primary region of worry in VLSI outline. Reversible rationale has its rudiments from thermodynamics of data preparing. As indicated by this, customary irreversible circuits create heat because of the loss of data amid calculation. With a specific end goal to evade this data misfortune the ordinary circuits are displayed utilizing reversible rationale. Landauer [1961] demonstrated that the circuits planned utilizing irreversible components scatter heat because of the loss of data bits [1]. It is demonstrated that the loss of one piece of data results in dispersal of KT*log2 joules of warmth vitality where K is the Boltzmann steady and T is the temperature at which the operation is performed. Benett [1973] demonstrated that this warmth dispersal because of data misfortune can be kept away from if the circuit is planned utilizing reversible rationale entryways [2]. An entryway is thought to be reversible if for every last information there is an one of a kind yield task. Henceforth there is a balanced mapping between the information and yield vectors. A reversible rationale door is a n –input, n-yield gadget demonstrating that it has same number of inputs and yields. A circuit that is constructed from reversible entryways is known as reversible rationale circuit. In this paper, we outline 5×5 piece reversible multiplier that can perform multiplier operations all the while. Every one of the modules are recreated in modalism SE 6.5 and incorporated utilizing Xilinx ISE 14.

II. OVERVIEW

The research on reversible logic is being pursued towards both design and synthesis. Inthe synthesis of reversible logic circuits there have been several interesting attempts in the literature such as the work in [2-3]. A reversible arithmetic logic unit was designed by Thomsen, Gluck, and that was based on the V-shaped design of the Van Rentergem adder [5].
Majid Haghparast et al. [3], Reversible logic circuits are of interests to power minimization having applications in low power CMOS design, optical information processing, DNA computing, bioinformatics, quantum computing and nanotechnology. In this paper we a novel 4x4 bit reversible multiplier circuit. The reversible multiplier is faster and has lower hardware complexity compared to the existing counterparts. It is also better than the existing counterparts in term of number of gates, garbage outputs and constant inputs. Haghparast and Navi recently proposed a 4x4 reversible gate called "HNG". The reversible HNG gate can work singly as a reversible full adder. In this paper we use HNG gates to construct the reversible multiplier circuit. The proposed reversible multiplier circuit using HNG gate can multiply two 4-bits binary numbers. The proposed reversible 4x4 multiplier circuit can be generalized for NxN bit multiplication. We can use it to construct more complex systems in nanotechnology.
Md. Belayet Ali et al. [4], Reversible logic circuits are increasingly used in power minimization having applications such as low power CMOS design, optical information processing, DNA computing, bioinformatics, quantum computing and nanotechnology. The problem of minimizing the number of garbage outputs is an important issue in reversible logic design. In this paper we design 4×4 universal reversible logic gate. The reversible gate can be used to synthesize any given Boolean functions. The reversible gate also can be used as a full adder circuit. In this paper we have used Peres

gate and the proposed HNG gate to construct the reversible fault tolerant multiplier circuit.

Indrayani Patle et al. [5], This Paper presents the work on implementation of Baugh-Wooley multiplier based on soft-core processor. MicroBlaze soft core is high performance embedded soft core processor developed by XILINX Company. This soft core enjoys high configurability and allows designer to make proper choice based on his
own design requirements to build his own hardware platform. Custom hardware of power optimized Baugh-Wooley signed multiplier is interface with MicroBlaze soft core processor. The major objective for using hardware for realizing Baugh-Wooley multiplier is to utilize hardware for realizing fast and efficient processing capacity.

Hatkar A. P. et al. [6], Reversible logic is very much in demand for the future computing technologies as they are known to produce low power dissipation having its applications in Low Power CMOS, Quantum Computing, Nanotechnology, and Optical Computing. Adders and multipliers are fundamental building blocks in many computational units. In this paper we have presented and implemented reversible Wallace signed multiplier circuit in ASIC through modified Baugh-Wooley approach using standard reversible logic gates/cells, based on complementary pass transistor logic and have been validated with simulations, a layout vs. schematic check, and a design rule check. It is proved that the multiplier is better and optimized, compared to its existing counterparts with respect to the number of gates, constant inputs, garbage outputs, hardware complexity, and number of transistors required.

III. REVERSIBLE GATES

Reversible rationale is picking up significance in ranges of CMOS configuration on account of its low power dispersal. The conventional entryways like AND, OR, XOR are all irreversible doors. Consider the instance of conventional AND door. It comprises of two inputs and one yield. Subsequently, one piece is lost every time a calculation is completed. As per reality table there are three inputs (1, 0), (0, 1) and (0, 0) that compares to a yield zero. Subsequently it is unrealistic to focus an extraordinary info that brought about the yield zero. With a specific end goal to make a door reversible extra information and yield lines are added so that a coordinated mapping exists between the data and yield. This keeps the loss of data that is fundamental driver of force scattering in irreversible circuits. The info that is added to a m x n capacity to make it reversible is known as steady information (CI). Every one of the yields of a reversible circuit require not be utilized as a part of the circuit. Those yields that are not utilized as a part of the circuit is called as waste yield (GO). The quantity of waste yield for a specific reversible door is not settled.The two main constraints of reversible logic circuit is

- Fan out not allowed
- Feedbacks or loops not allowed.

○ BASIC REVERSIBLE GATES

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is shown in figure 1. It is the only 2x2 reversible gates available and is commonly used for fan out purposes. Consider the input B as constant. When B is zero, the gate acts as a copying gate or a buffer where both the output lines contain the input A. When B is one, the complement of A is obtained at the output Q. The 3x3 reversible gates include Toffoli gate, Fredkin gate, new gate and Peres gate, all of which can be used to realize various Boolean functions. Fredkin gate is shown in figure 2.

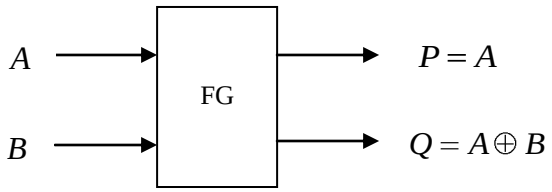

Figure 1: Feynman Gate

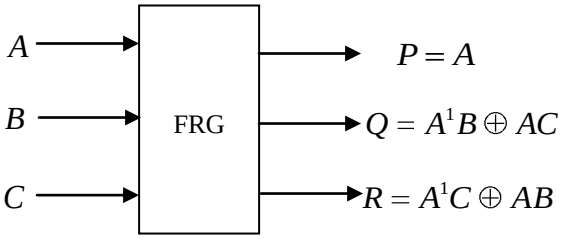

Figure 2: Fredkin Gate

Figure 3 shows the Peres gate. Some of the 3x3 gates are designed for implementing some important combinational functions in addition to the basic functions. Most of the above mentioned gates can be used in the design of reversible multiplier.

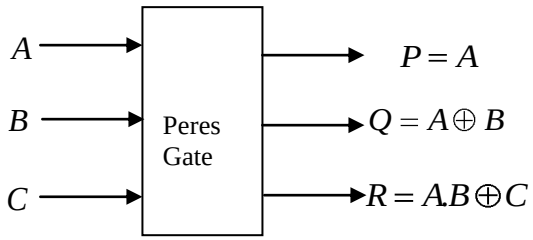

Figure 3: Peres gate

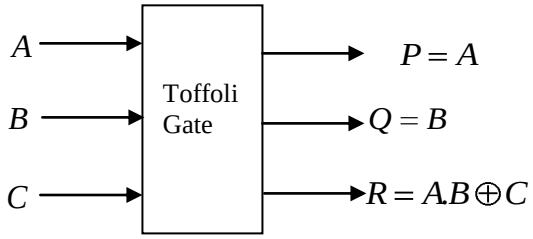

Figure 4: Toffoli gate

The Toffoli gate is a 3X3 gate has quantum cost of 5 and garbage outputs of 2. The Peres gate is also a 3X3 reversible gate whose quantum cost is 4 and garbage outputs are 2.

Several 4x4 gates have been described in the literature targeting low costand delay which may be implemented in a programmable manner to produce a high number of logical calculations. The HNG gate, presented in [7], produces the followinglogical output calculations:

$$P = A \qquad (1)$$

$$Q = B \qquad (2)$$

$$R = A \oplus B \oplus C \qquad (3)$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \qquad (4)$$

The quantum cost and delay of the HNG is 6. When $D = 0$,the logical calculations produced on the R and S outputs are the required sum and carry-out operations for a full adder. The block diagram of the HNG is presented in Fig. 5.

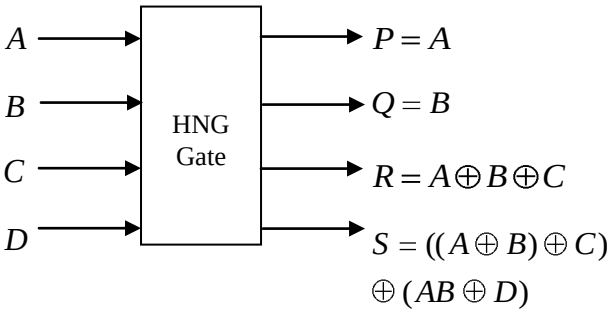

Figure 5: Block Diagram of HNG Gate

IV. REVERSIBLE MULTIPLIER

To compute product of two signed numbers we have used modified Baugh-Wooley approach [8]. Both logical and reversible multiplier design is divided into two parts: partial product generation circuit and then multi-operand addition circuit.

Design of Logical Multiplier:-

First to compute partial product, we used 17 AND and 8 NAND employing the procedure given in figure 6. After generating partial products, next step is a multi-operand addition. We should add the bits of each column given in figure 6. To add these bits, we need FA and HA. We have to add these bits in the way that our circuit will give the best results.

Figure 6 shows the way of adding these bits in our proposed circuit. The Wallace approach has been used to construct a circuit with less delay. To minimize delay in our proposed circuit, P_9 is computed by inverting carry output from earlier FA (FA13). The resulting circuit for multi-operand addition needs one 1-NOT gate, 4-HA and 16-FA.

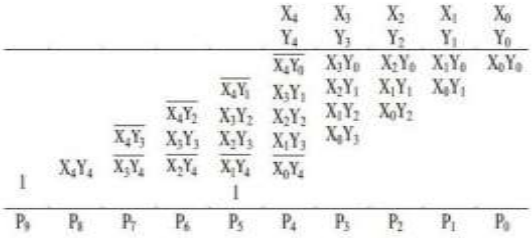

Figure 6: Baugh-Wooley 5 x 5 Signed Multiplier

Design of reversible multiplier:-

The operation of the 5x5 multiplier is depicted in figure 7. It consists of 25 partial product bits of the form $X_i Y_i$.

The reversible 5x5 multiplier circuit has two parts. First, the partial products are generated in parallel using Toffoli gate.

We used 25 Toffoli gates to create 17 ANDs and 8 NANDs as shown in figure. The modified partial the last low replace by Peres gate because Peres gate has quantum cost of 4 as shown if figure 8.

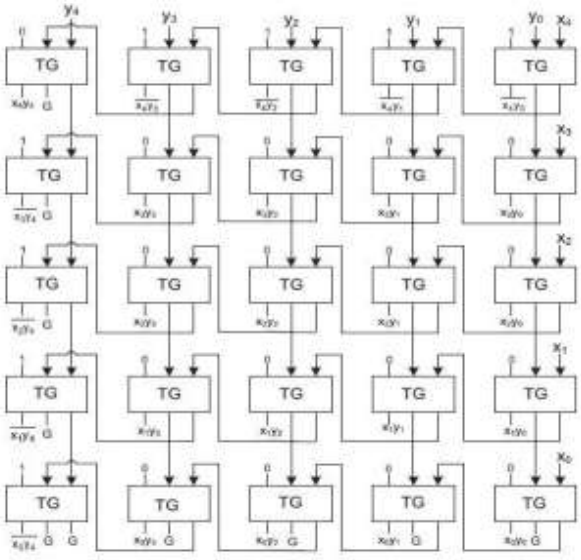

Figure 7: Partial Product Generation by Toffoli Gates

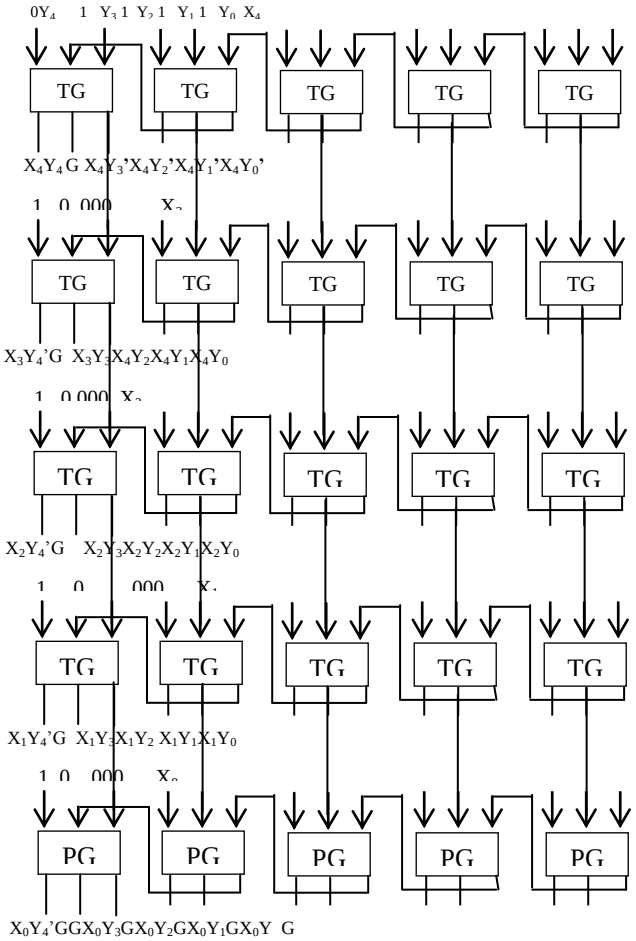

Figure 8: Modified Partial Product Generation by Toffoli and Peres

V. COMPARITIVE RESULT

The proposed reversible multiplier circuit is more efficient than the existing circuit presented by [6], [7], [8] and [9]. The proposed reversible multiplier circuit is divided two part i.e. partial product and multi-operand addition. The proposed partial product is minimize 5 quantum cost in the design. Increase the number bit of the reversible multiplier circuit so reduced the quantum cost.

Table 1: Comparative results of partial product generation circuit

Method	No. of Gate	No. of garbage output	Hardware Complexity	Quantum Cost
Proposed	25	10	25α+25β	120
[6]	25	10	25α+25β	125
[7]	25	10	34α+25β	135
[8]	25+20	30	45α+25β	145
[9]	25+25	35	45α+30β	155

Next step is a multi-operand addition. After generating given in Hatkar A.P. et al. [6]. To add these bits, we need and HA.

Table II: Comparative results of reversible signed multiplier circuit

Method	No. of Gate	No. of garbage output	Hardware Complexity	Quantum Cost
Proposed	45	46	25α+25β	232
[6]	45	46	113α+61β	237
[7]	45	46	122α+61β	228
[8]	65	70	205α+105β	-
[9]	85	80	275α+132β	-

VI. CONCLUSION

In this paper we presented and successfully implemented Wallace reversible signed multiplier circuit. It is proved that not only the proposed multiplier is better and optimized, compared to its existing counterparts with

respect to the number of gates, garbage outputs, hardware complexity, and quantum cost.

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