Design of an Alphanumeric Symbol Encoder Circuit using Quantum Dot Cellular Automata

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Abstract :

For the last few decades Complementary Metal-Oxide Semiconductor (CMOS) has replaced NMOS and PMOS for implementing high speed ICs for its less power consuming characteristics and has become industrial standard for implementing Very Large Scale Integrated (VLSI) circuits. In recent days CMOS technology is being scaled into nanometer level to achieve higher switching speed, higher complexity, smaller circuit size and smaller power consumption. CMOS technology imposes unavoidable limitations after scaling into nanometer level such as subthreshold leakage current, short channel effects, high fabrication costs and interconnect delay etc. and therefore, the outcome is not satisfactory. To solve this many alternative technologies has been proposed in last few years among which QCA has been proved to be most promising technology . A lot of digital circuits have been designed using QCA which includes encoder also. In this paper an alphanumeric symbol encoder circuit is designed using QCA technology. The QCA circuit has been simulated in QCADesigner tool.

Keywords — *Quantum dot cellular automata, alphanumeric symbol, encoder, kink energy.*

I. INTRODUCTION

Message encoding is a very important technique in communication system. Encoding can be defined as a process by which data in one format can be converted into some other format. In character encoding process a series of characters or symbols can be converted to a specialized format for various purposes like data storage, data transmission (textual data), data computation etc. Encoding of textual data also provides the advantage of data encryption because it will be difficult for any unauthorized party to intercept the encoded message. In this paper design of a new kind of alphanumeric symbol encoder circuit has been introduced. This circuit will encode an alphanumeric symbol into a series of binary bits depending on some encoding scheme. This design comprises of two types of encoding scheme; part I: Binary to BCD and part II: BCD to Excess 3 including encoding of the carry bit generated from part I. QCA technology design approach is presented here. For implementing VLSI circuits CMOS technology has become a standard but when CMOS is being scaled down to nanometer level to achieve more switching speed, the power consumed by the circuit is huge and is undesirable. QCA technology is a very promising solution to this problem as it provides low power consumption and smaller circuit size and higher switching speed at the same time [1]-[3]. Unlike digital logic where a certain range of voltage or current represents binary 1 or 0, QCA technology uses position of electrons in quantum dots of a QCA cell to represent binary values [3].

II. BACKGROUND OF QCA

A. QCA Basics

A QCA cell is a fundamental unit of a QCA device having four quantum dots in it with two excess electrons. Each of the electrons is free to tunnel between dots within one cell, as they are confined in that cell [3]-[5]. Electrostatic repulsion between these two electrons will result into only two stable states for each cell as shown in Fig. 1 [1]. One of them represents binary '1' and other one to represent binary '0' [6], [7]. The state of a cell is also termed as polarization. In this paper polarization +1 has been chosen to represent logic 1 and polarization -1 to represent logic 0. QCA cells are placed one after another to form an array like structure which are the building blocks of a QCA circuit [4],[8],[9]. Information through the array is being passed using Columbic interaction between the cells [1],[4],[10]. In digital logic AND OR NOT are the basic gates, but in QCA technology the main operator is a 3 input majority gate [11] (shown in Fig. 2) which is used to implement the basic 2-input AND and 2-input OR gate as shown in Fig. 3 [3]. Another important operator is QCA inverter that can be implemented in various ways but in the current design a two cell inverter (shown in Fig. 4) has been used. In this paper the alphanumeric symbol encoder circuit is designed based on these basic QCA logic gates only. The proposed circuit has a great potential in reducing the power consumption in information processing system and can trigger higher digital applications in QCA [3],[5].

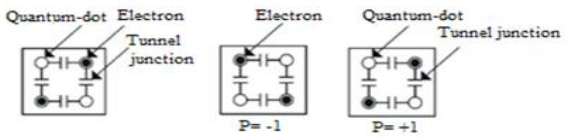

Fig. 1 (a) Basic QCA Cell (b) Basic QCA Cell with the Two Possible Ground-State Polarizations

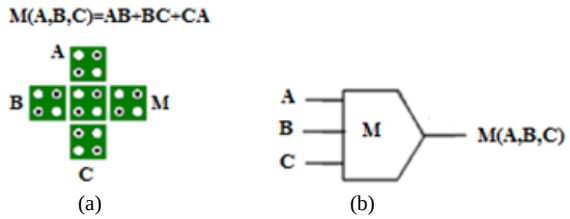

Fig. 2 (a) QCA Majority Gate (b) Majority Gate Symbol

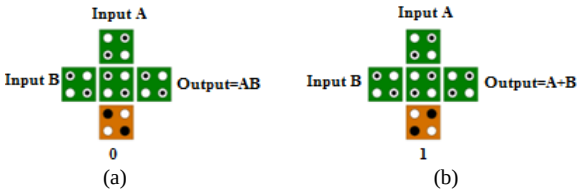

Fig. 3 QCA Implementation of (a) 2-Input AND Gate (b) 2-Input OR Gate

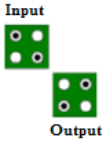

Fig. 4 QCA Inverter

III. DESIGN OF ALPHANUMERIC SYMBOL ENCODER CIRCUIT: PART I

Alphanumeric is an amalgamation of alphabetic and numeric characters which describes the range of Latin letters and Arabic digits or a text constructed from this range. In this paper an alphanumeric symbol is being encoded to a series of binary digits using two different encoding schemes.

Every alphanumeric symbol has a corresponding Hex Value and Hex values can easily be represented with binary digits. In the part I of this design binary representation of Hex values are converted to a valid BCD number in a different way.

A. PART I: Binary to BCD Code Converter

Each alphanumeric symbol has a Hex value. Each hex digit is represented with binary numbers and can be converted to a valid BCD number as shown in Table 1.

Table I : Truth Table of Binary to BCD Code Conversion

Binary Code				BCD Code				
D	C	B	A	B_4	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	0
0	0	1	1	0	0	0	1	1
0	1	0	0	0	0	1	0	0
0	1	0	1	0	0	1	0	1
0	1	1	0	0	0	1	1	0
0	1	1	1	0	0	1	1	1
1	0	0	0	0	1	0	0	0
1	0	0	1	0	1	0	0	1
1	0	1	0	0	1	0	1	0
1	0	1	1	1	0	0	0	0
1	1	0	0	1	0	0	0	1
1	1	0	1	1	0	0	1	0
1	1	1	0	1	0	1	0	0
1	1	1	1	1	0	1	0	1

Here [D C B A] represents the binary number and [B4 B3 B2 B1 B0] represents the valid BCD number. After doing the K-map simplification, the following was found;

B4=DC+DB;
B3=DC'B';
B2=D'C+CB;
B1=DCB'+D'B; B0=A

The QCA implementation of the circuit using this logic has been shown in Fig. 5. Only basic gates like AND, OR, NOT gates has been used.

B. QCA Implementation

QCA implementation of basic gates like AND, OR, NOT has been shown in Fig. 3 and Fig. 4. Following that convention the circuit using the logic mentioned above has been implemented in QCA technology using QCADesigner software. The final QCA implementation of Binary to BCD code converter circuit has been shown in Fig. 5. The circuit is designed with minimum area where minimum number of cells is required.

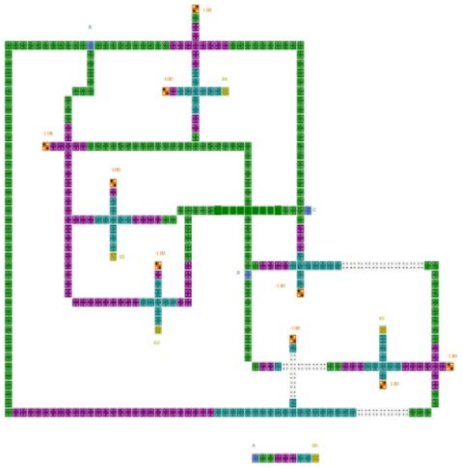

Fig. 5 QCA Implementation of Binary to BCD Code Converter Circuit.

C. Output

Let the word to be encoded is 'IEM'. Input of Part I is represented by [D C B A] and output is represented by [B_4 B_3 B_2 B_1 B_0]. Input and output of Part I is shown in Table 2 below.

Table II: Input and Output of Part I

Alphanumeric Symbol	Hex Value	Hex Digit	Input				Output				
			D	C	B	A	B_4	B_3	B_2	B_1	B_0
I	49	4	0	1	0	0	0	0	1	0	0
		9	1	0	0	1	0	1	0	0	1

E	45	4	0	1	0	0	0	0	1	0	0
		5	0	1	0	1	0	0	1	0	1
M	4D	4	0	1	0	0	0	0	1	0	0
		D	1	1	0	1	1	0	0	1	1

D. Simulation Results

The simulation result of binary to BCD code converter circuit in Fig. 6 shows the values of output bits B_4 to B_0 as mentioned in the Table 2.

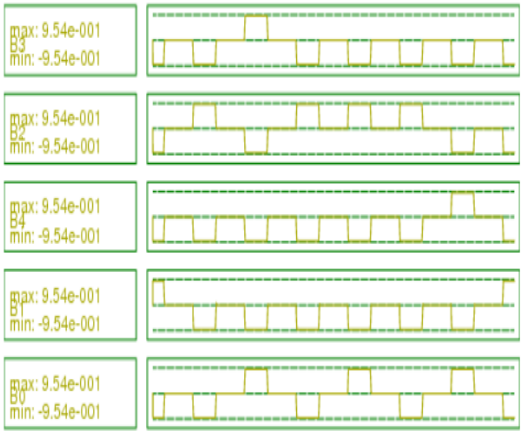

Fig. 6 Simulation Results of Binary to BCD Code Converter Circuit for the Input word 'IEM'

E. Automatic Layout Generation of Binary to BCD Code Converter Circuit

The Binary to BCD code converter circuit layout can be generated automatically using MVSIS tool. MVSIS stands for multi-valued SIS (Sequential Interactive Synthesis) and it is a logic synthesis tool for combinational and sequential circuits, which improves conventional binary logic synthesis with capabilities related to multi-value logic. Automatic layout generation process will save a lot of time when compared to designing the circuit from scratch through cell by cell. The input file to MVSIS tool contains a program that uses the logic expressions for the circuit. The tool produces a QCA file where the layout is generated automatically [12].The layout for Binary to BCD converter circuit generated through this process is shown in Fig. 7.

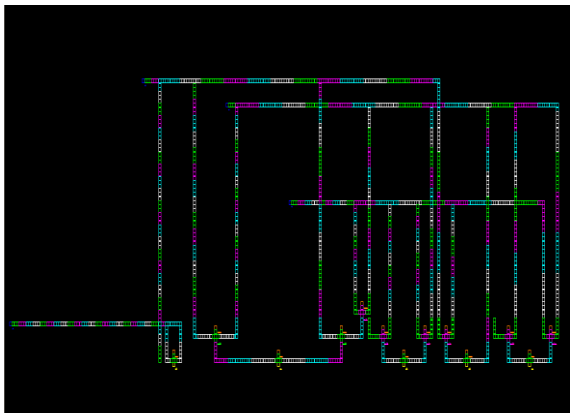

Fig. 7 Automatically Generated Layout for Binary To BCD Code Converter

IV. DESIGN OF ALPHANUMERIC SYMBOL ENCODER CIRCUIT: PART II

A. PART II: BCD to Excess 3 Code Converter

Output of part I represent the BCD code for each alphanumeric symbol in a different way. This BCD code excluding the MSB bit can be converted to an excess 3 code using the truth table shown in Table 3.

Here [B3 B2 B1 B0] represents the BCD code where as [A3 A2 A1 A0] represents the excess 3 code. After doing the K-map simplification the following expressions were found.

A3=B3+B2.(B1+B0),
A2=B2'.(B1+B0)+B2.(B1+B0)',
A1= B1.B0+(B1+B0)' ,
A0= B0'

Table III : Truth Table for BCD to Excess-3 Code Conversion

BCD Code				Excess-3 Code			
B_3	B_2	B_1	B_0	A_3	A_2	A_1	A_0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

B. PART IIA: Encoding the MSB Bit (B_4) in the Output BCD Code of Part I

The MSB bit B_4 in the output BCD code of part I is also encoded to a 4 bit number [A_7 A_6 A_5 A_4] following the excess-3 code logic. If B_4 bit is 0 then it is encodes as '0011' which is the binary equivalent of 3(0+3=3) and if B_4 bit is 1 then it is encodes as '0100' which is the binary equivalent of 4(1+3=4) So B_4 bit is encoded using the truth table shown in Table 4. The circuit diagram using this logic has been shown in Fig. 8.

Table IV : Truth Table for Encoding the Msb Bit B4

Input Bit(B_4)	Output
0	0011
1	0100

Circuit Diagram using Basic Gates:

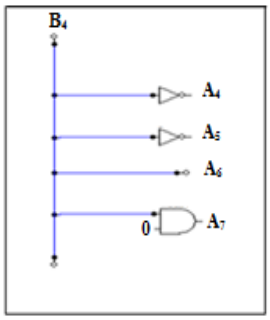

Fig. 8 Encoding of the MSB bit B4

C. QCA Implementation

QCA implementation of basic gates like AND, OR, NOT has been shown in Fig. 3 and Fig. 4. Following that convention the circuit using the logic mentioned above has been implemented in QCA technology using QCADesigner software. The final QCA implementation of BCD to Excess-3 code converter circuit has been shown in Fig. 9. The circuit is designed with minimum area where less number of cells is required.

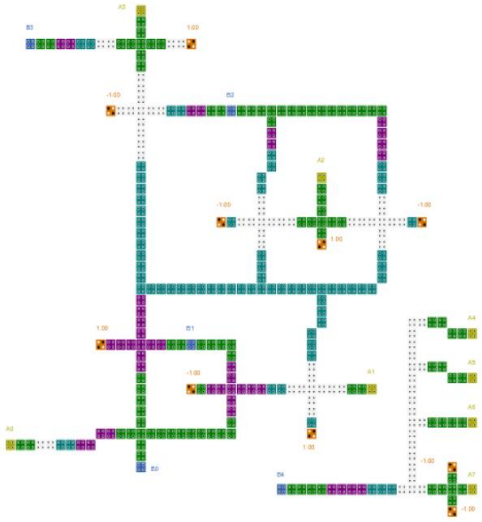

Fig. 9 QCA Implementation of BCD to Excess-3 Code Converter Circuit

D. Output

Output of Part I represented by [B_4 B_3 B_2 B_1 B_0] is fed as the input of Part II. [B_3 B_2 B_1 B_0] is converted to excess-3 code [A_3 A_2 A_1 A_0]. B_4 bit is encoded as [A_7 A_6 A_5 A_4]. So output of Part II is represented by [A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0]. Input and output of Part II is shown in Table 5.

Table V : Input and Output of Part II

INPUT					OUTPUT							
BCD CODE					Encoded B_4 Bit				Excess-3 Code			
B_4	B_3	B_2	B_1	B_0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	1	0	0	0	0	1	1	0	1	1	1
0	1	0	0	1	0	0	1	1	1	1	0	0
0	0	1	0	1	0	0	1	1	1	0	0	0
0	0	1	0	0	0	0	1	1	0	1	1	1
0	0	1	0	0	0	0	1	1	0	1	1	1
1	0	0	1	1	0	1	0	0	0	1	1	0

E. Simulation Results

The simulation result shows the values of output bits A_7 to A_0 as mentioned in the Table 5. This also shows the simulation result of the final circuit as mentioned in Fig. 12.

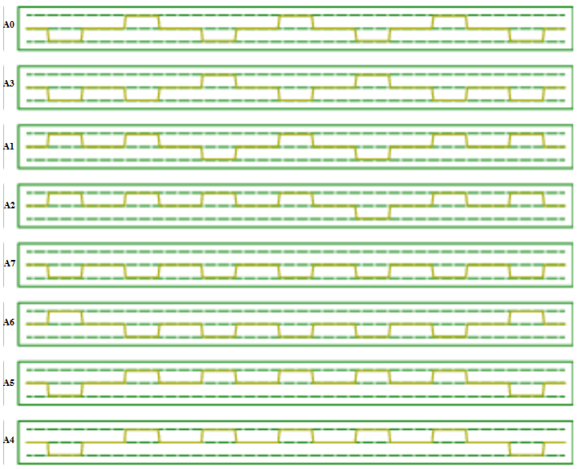

Fig. 10 Simulation Results of BCD to Excess-3 Code Converter Circuit for the input word 'IEM'

F. Automatic Layout Generation of BCD to Excess-3 Code Converter Circuit

The layout for BCD to Excess-3 code converter circuit also can be generated automatically using MVSIS tool [12] in the similar way as mentioned in section 3.5. The generated layout is shown in Fig. 11.

Fig. 11 Automatically Generated Layout for BCD to Excess-3 Code Converter

V. DESIGN OF ALPHANUMERIC SYMBOL ENCODER CIRCUIT: COMBINING BOTH PART

A. QCA Implementation of Both Part I and Part II Together

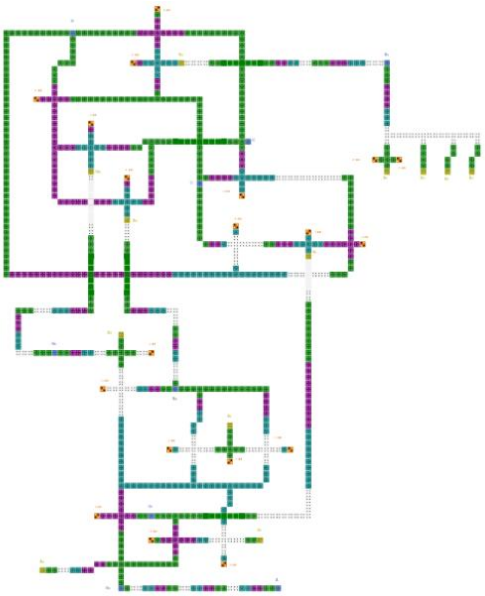

Fig. 12 QCA Implementation of Both Part Combined

B. End Result

Final output for encoding of the word 'IEM' where each letter is an alphanumeric symbol is shown in Table 6 below.

Alpha numeric Symbol	Input to Part I D C B A				Output of Part I and Input of Part II B_4 B_3 B_2 B_1 B_0					Output of Part II A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0							
I	0	1	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1
	1	0	0	1	0	1	0	0	1	0	0	1	1	1	1	0	0
E	0	1	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1
	0	1	0	1	0	0	1	0	1	0	0	1	1	1	0	0	0
M	0	1	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1
	1	1	0	1	1	0	0	1	1	0	1	0	0	0	1	1	0

Table VI : Encoding of the Word 'Iem'

C. Complexity and Area of QCA Structures

Complexity, area and latency are calculated for the QCA circuits mentioned in this paper and shown in Table 7 below.

Table VII : Complexity and Area of Qca Structures

QCA Structure	Complexity	Area	Latency
Part I in Fig. 5	428 cells	1.24 μm^2	1.75
Part I in Fig. 7	1587 cells	7.08 μm^2	6.25
Part II in Fig. 9	292 cells	0.89 μm^2	1.25
Part II in Fig. 11	1658 cells	6.90 μm^2	7.25
Circuit in Fig. 12	950 cells	3.08 μm^2	4.25

VI. KINK ENERGY CALCULATION

To prove that proposed design is robust and stable kink energy of the circuit is calculated which is defined as the energy cost of two different neighbouring cells. Kink energy does not depend upon the temperature variation of the QCA cells but depends upon the spacing between two adjacent cells [13]. Table 8 shows output bit's kink energy for various input combinations. From the calculation it is observed that output is a steady one as there is not any significant fluctuation of energy for a particular combination.

To calculate the kink energy the following formula is used [14]-[19]:

$$U=\frac{k\times Q1\times Q2}{r};$$

Where U is the kink energy, k is a constant value and $k=1/(4\pi\varepsilon_0\varepsilon_r)=9\times10^9$ [15]-[18]. Q_1 and Q_2 are charges of the two electrons for which the energy is being calculated and r is the distance between them. By putting the values of k, Q_1 and Q_2

$$k\times Q_1\times Q_2=9\times10^9\times1.6\times10^{-19}\times1.6\times10^{-19}=23.04\times10^{-29}$$

In this paper kink energy is calculated for those cells which are responsible for determining the output. Output bit B_4 from Part I is taken as an example. The output portion for B_4 bit is shown in Fig. 13. Here input bits are taken as 1 0 1 but energy can be calculated in similar way for other combinations also. At first kink energy is calculated between each of the electrons (shown as e_1, e_2, e_3, e_4, e_5, e_6, e_7, e_8, e_9, e_{10}, e_{11}, and e_{12}) with electron 'x' [14] in the Fig. 13. Then these kink energies are summed up and denoted as $U_{T1.}$ Similar process is followed for electron 'y' and the kink energy is denoted as U_{T2}. Total kink energy for bit B_4 is calculated as:

$$U_T=U_{T1}+U_{T2}$$

For this calculation it is assumed that all cells are identical having square shape whose each side has a length 18nm. Inter cell spacing for two adjacent cells is assumed to be 2nm.

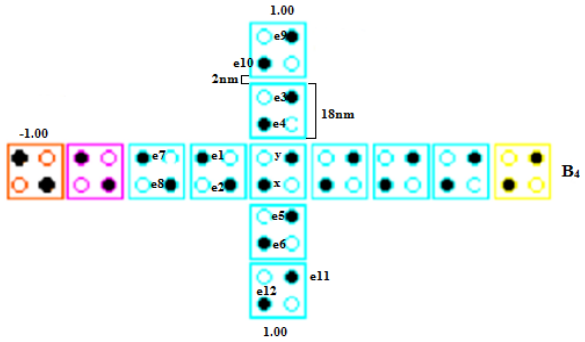

Fig. 13 Kink Energy Calculation for bit B4

Calculations for electron x in Fig. 13	Calculations for electron y in Fig. 13
$U_1= (23.04\times10^{-29}) / (26.91\times10^{-9}) \approx 0.86\times10^{-20}$(J)	$U_1= (23.04\times10^{-29}) / (38\times10^{-9}) \approx 0.61\times10^{-20}$(J)
$U_2= (23.04\times10^{-29}) / (2\times10^{-9}) \approx 11.52\times10^{-20}$(J)	$U_2= (23.04\times10^{-29}) / (26.9\times10^{-9}) \approx 0.86\times10^{-20}$(J)
$U_3= (23.04\times10^{-29}) / (42.05\times10^{-9}) \approx 0.55\times10^{-20}$(J)	$U_3= (23.04\times10^{-29}) / (20\times10^{-9}) \approx 1.15\times10^{-20}$(J)
$U_4= (23.04\times10^{-29}) / (20\times10^{-9}) \approx 1.15\times10^{-20}$(J)	$U_4= (23.04\times10^{-29}) / (18.11\times10^{-9}) \approx 1.27\times10^{-20}$(J)
$U_5= (23.04\times10^{-29}) / (18.11\times10^{-9}) \approx 1.27\times10^{-20}$(J)	$U_5= (23.04\times10^{-29}) / (20\times10^{-9}) \approx 1.15\times10^{-20}$(J)
$U_6 = (23.04\times10^{-29}) / (20\times10^{-9}) \approx 1.15\times10^{-20}$(J)	$U_6 = (23.04\times10^{-29}) / (42.05\times10^{-9}) \approx 0.55\times10^{-20}$(J)
$U_7= (23.04\times10^{-29}) / (43.86\times10^{-9}) \approx 0.52\times10^{-20}$(J)	$U_7= (23.04\times10^{-29}) / (58\times10^{-9}) \approx 0.38\times10^{-20}$(J)
$U_8= (23.04\times10^{-29}) / (22\times10^{-9}) \approx 1.05\times10^{-20}$(J)	$U_8= (23.04\times10^{-29}) / (43.86\times10^{-9}) \approx 0.52\times10^{-20}$(J)
$U_9= (23.04\times10^{-29}) / (60.73\times10^{-9}) \approx 0.38\times10^{-20}$(J)	$U_9= (23.04\times10^{-29}) / (40\times10^{-9}) \approx 0.58\times10^{-20}$(J)
$U_{10}= (23.04\times10^{-29}) / (40\times10^{-9}) \approx 0.58\times10^{-20}$(J)	$U_{10}= (23.04\times10^{-29}) / (28.42\times10^{-9}) \approx 0.81\times10^{-20}$(J)
$U_{11}= (23.04\times10^{-29}) / (28.42\times10^{-9}) \approx 0.81\times10^{-20}$(J)	$U_{11}= (23.04\times10^{-29}) / (40\times10^{-9}) \approx 0.58\times10^{-20}$(J)
$U_{12}= (23.04\times10^{-29}) / (40\times10^{-9}) \approx 0.58\times10^{-20}$(J)	$U_{12}= (23.04\times10^{-29}) / (60.73\times10^{-9}) \approx 0.38\times10^{-20}$(J)
$U_{T1}=\sum U_i=20.42\times10^{-20}$(J)	$U_{T2}=\sum U_i=8.84\times10^{-20}$(J)
$\mathbf{U_T= U_{T1} + U_{T2} = 29.26\times10^{-20}(J)}$	

In similar way kink energies for other bits are calculated. For each bit two types of input combinations have been taken.

Table VIII : Kink Energy Calculation

	Bit	Input Combination	Output	Kink Energy (10^{-20}(J))
PART I	B_4	1,0,1	1	29.26
		0,0,1	0	29.26
	B_3	0,0,1	0	29.26
	B_2	1,0,1	1	29.26
		1,0,0	0	30
		0,0,0	0	19.41
	B_1	1,1,0	1	29.5
		0,1,0	0	29.26
	B_0	1	1	6.47
		0	0	6.47
PART II	A_7	0,1,0	0	29.26
		0,0,0	0	19.41
	A_6	1	1	6.47
		0	0	6.47
	A_5 , A_4	1	0	5.55
		0	1	5.55
	A_3	0,0,1	0	29.26
		0,1,1	1	29.26
	A_2	1,1,0	1	29.5
		1,1,1	1	19.65
	A_1	1,0,1	1	29.26
		0,0,1	0	29.26
	A_0	1	0	5.55
		0	1	5.55

VII. CONCLUSION AND FUTURE SCOPE

This paper represents a design of alphanumeric symbol encoder circuit based on QCA logic design. The circuit designed with QCADesigner provides a new functional platform for information encoding. In a communication system any message which contains alphanumeric symbols can be encoded by using this circuit and then can be transmitted to provide information security. This design is implemented using minimum number of QCA cells, lesser clock delays and reduced area which will provide high-speed computing, high-density application. To check the robustness of the circuit kink energy or the energy cost calculation is done, which proves the designed coder gives a stable output. This paper also describes a layout generator circuit which will generate automatically the required design in QCA environment after programming. Layout consists of more number of cells compare to the design by using QCADesigner tool. So in future it is aimed to reduce the number of cells in layout design.

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