Analysis of Front-End High Gain DC-DC Converters for Pulsed Electric Field Application

R.Kavitha[1#], V.Rajini, S.Krishnaveni

Department of electrical and electronics engineering, SSN College of Engineering, Tamil-Nadu, India

Abstract

This paper presents a comparative analysis of two high gain dc-dc converters with Voltage Multiplier Cells (VMC) for Pulsed Electric Field (PEF) applications. Voltage Multiplier Cells (VMC) are used to improve the voltage conversion ratio. These high gain dc-dc converters are used as the front-end converters for Pulsed Electric Field (PEF) circuit to produce pulsed output of higher amplitude for bacterial inactivation in food particles. The basic concepts of two high gain converters are discussed and a comparison in terms of the switch voltage stress, output diode voltage stress, input current and output voltage from the Pulsed Electric Field (PEF) circuit are done. The performance comparison and analysis for both the converters are achieved through the results from MATLAB simulation.

Keywords—*PEF, dc-dc converter, built-in transformer, voltage multiplier cells,front-end converter, boost-integrated isolated converter*

I. INTRODUCTION

In the traditional thermal method of food preservation increase in temperature will cause the detrimental effect on food quality attributes. Pulsed Electric Field (PEF) technology is a non-thermal method which utilises high pulsed electric field and causes microbial decontamination in food particles like milk, egg, apple, orange juice, potato, yogurt drinks etc. This enhances the shelf period of the food particle while retaining the flavour, protein,vitamin, and all other nutritional content of the food particles.[1]

When biological tissues are exposed to PEF treatment, the process of electro perturbationoccurs. The cell membrane of the biological tissues are made permeable which allows easy access to the nuclei and mitochondria without damaging the outer cell membrane [2].

For producing such effects in biological cells, there occurs a need for high voltage source to the PEF circuit and a dc-dc converter with high voltage gain could be suitably used in the front end of PEF circuit for high voltage production.

The switched capacitor based converter [3]was introduced to replace the conventional boost converter to minimise the diode reverse recovery problem and switching losses. Due to the occurrence of large transient current, the life period of capacitors were reduced in this method.

To reduce the switching losses, soft switching techniques were introduced [4]. In this converter topology,a part of the circuit resonates for a small period of the switching cycle that provides soft switching for the converter thus reducing the switching losses and improves the converter efficiency.

To overcome the problem of extreme duty cycle coupled inductor technique [5]-[8] was suggested which has reduced the voltage stress across switches without extreme duty cycle. The main drawback in this method was that the input side capacitor had more current ripple.

Interleaved high step-up converter with cross-coupled inductor were introduced to reduce the current ripple but due to the cross-coupled inductor winding,the circuit complexity was increased.

To provide high voltage gain and to reduce the voltage stress, Voltage Multiplier Cells (VMC)[9],[10]were introduced into the boost converters. The voltage gain was improved by cascading several multiplier cells which reduces the input current ripple.

In addition to switch duty cycle, the turns ratio of the built-in transformer [11]-[13] can be used to increase the voltage gain which is an added advantage to the isolated converter.

To achieve a high voltage gain with high efficiency a non-isolated high step up stacked converter based on boost-integrated isolated converter [14] is proposed. A voltage-doubler-rectifier boost-integrated half-bridge (VDRBHB) converter is introduced to improve the voltage gain and to decrease the voltage stress. In addition to the primary side, the secondary side of the converter is stacked to obtain the high voltage conversion ratio. The main shortcoming in this converter is that the turnsratio of the transformer has to be maintained at a higher value to have a high voltage gain.

To obtain a high voltage gain with minimum value of turns ratio an interleaved high step-up zero voltage transition (ZVT) converter with built-in transformer voltage doubler cell[15] was proposed, in which the transformer turns ratio and the switch duty cycle were varied to improve the voltage ratio.

Voltage doubler cells consists of three winding transformer, diodes and capacitors. ZVS soft switching technique was employed for reducing the switch voltage stress. Additional clamp switches are necessary to absorb the energy and the interleaved phases are coupled with diode which increase the circuit complexity.

To over come the above complications, a high gain interleaved DC-DC converter using transformer voltage multiplier cell [16] is proposed. The clamp switches in converter [15] are replaced by diodes in converter [16] and the coupled interleaved phase in converter [15] were decoupled in converter [16].Built-in transformer voltage multiplier cell is inserted into each phase of the conventional interleaved boost converter. Built-in transformer, diodes and capacitors together constitute the voltage multiplier cell.

This paper analyses the suitability of high gain front end converter proposed in [14] and [16] for PEF application. Comparison between the converters is being made on voltage stress across the switches and output diode, voltage gain, efficiency and input current to the converters.

This paper is organised as follows: Section II contains the detailed description of the high gain interleaved converter with built-in transformer VMC [16] with its various modes of operations. Section III deals with the high gain converter based on boost-integrated isolated converter [14]. Section IV shows the various simulated results for the converter [14] and [16]. Section V describes about the PEF circuit and its coupling with the dc-dc converters [14] and [16].Section VI investigates the performance comparison between the converter [14] and [16] and discuss about the suitability of the front end converter for the PEF application. Section VII summarises the conclusion.

II. OPERATION OF HIGH GAIN INTERLEAVED CONVERTER WITH BUILT-IN TRANSFORMER VMC[16]

The high gain interleaved converter with built-in transformer VMC [16] is shown in Fig.1. The two MOSFET switches are given by S_1 and S_2, the output diodes are denoted by D_{o1} and D_{o2}, the input inductors are given by L_1 and $L_2$and $C_o$is the output capacitor. The number of turns in the primary winding is given by $n_1$and the number of turns in the secondary and third windings are both n_2. $N(n_2/n_1)$ is the turns ratio of the transformer. The leakage inductance of transformer is denoted as L_{lk}. Clamp diode are given by D_{c1} and D_{c2}, regenerative diode are D_{r1} and D_{r2}, Clamp capacitors are C_{c1} and C_{c2}, multiplier capacitors areC_{m1} and C_{m2}.V_{in} and $V_{out}$are the input and output voltages of the high gain converter. The transformer winding, clamp diode, regenerative diode, clamp capacitor and multiplier capacitor together forms the voltage multiplier cells. The voltage multiplier cells are represented in the Fig.1. In this high gain converter [16] there are 12 operating stages in one switching period. Due to the symmetrical operating nature of the converter only 6 modes of operation are discussed below. The various modes are given in table I.

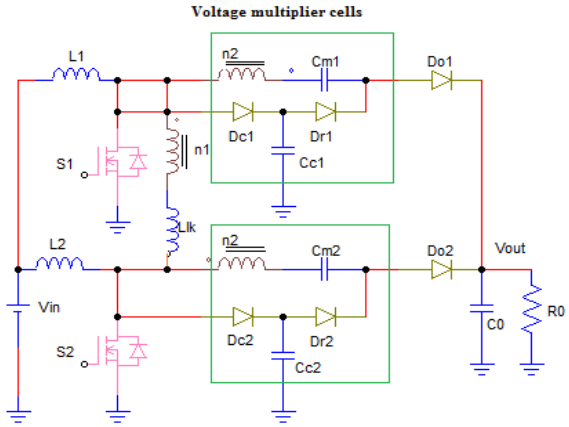

Fig.1 High gain interleaved converter with built-in transformer VMC [16]

TABLE I
VARIOUS MODES OF OPERATION FOR HIGH GAIN INTERLEAVED CONVERTER WITH BUILT-IN TRANSFORMER VMC [16]

Mode	Interval	Operation
1	(t_0,t_1)	Before t_1, S_1,S_2- ON state D_{c1},D_{c2},D_{r1},D_{r2},D_{o1},D_{02} are reverse biased and L_1 , L_2 are charged by V_{in}
2	(t_1,t_2)	At t_1, S_2 – OFF state,C_{S2} is charged linearly by current of L_2
3	(t_2,t_3)	At t_2, V_{ds2} is charged. D_{c2} is forward biased and C_{C2} is charged linearly by current of L_2
4	(t_3,t_4)	At t_3, D_{o2} is turned ON. The current through D_{o2} increases as current through C_{c2} decreases. As D_{r1} conducts and the energy stored in C_{c1} is transferred to C_{m1}
5	(t_4,t_5)	At t_4, current through C_{c2} decreases to zero and D_{c2} is turned OFF naturally. The energy stored in C_{m2} is transferred to load
6	(t_5,t_6)	At t_5, S_2 is turned ON with ZCS and D_{o2} is turned OFF at the end of the mode

III.HIGH GAIN CONVERTER BASED ON BOOST INTEGRATED ISOLATED CONVERTER [14]

The high gain non-isolated high step up stacked converter based on boost-integrated isolated

converter [14] is shown in Fig.2. The two power MOSFET switches are given by Q_M and Q_A.V_S is the supply voltage, V_O is the output voltage, I_O is the output current, L_B is the input side boost inductor and L_{LK} is the transformer leakage inductance. The primary turns is given by $n_1$and secondary turns is given by n_2. N (n_2/n_1) is the turns ratio of the transformer. The secondary side output diodes are represented by D_{S1} and D_{S2}. The primary side output capacitors are given by C_{P1} and C_{P2} and the voltage across the capacitors are given by V_{CP1} and V_{CP2} respectively. The secondary side output capacitors are given by C_{S1} and C_{S2} and the voltage across the capacitors are given by V_{CS1} and V_{CS2} respectively. The primary voltage V_P and secondary voltages $V_S$and the output voltage Vo are expressed as follows:

$$V_P = V_{CP1} + V_{CP2} \quad (1)$$

$$V_S = V_{CS1} + V_{CS2} \quad (2)$$

$$Vo = V_P + V_S \quad (3)$$

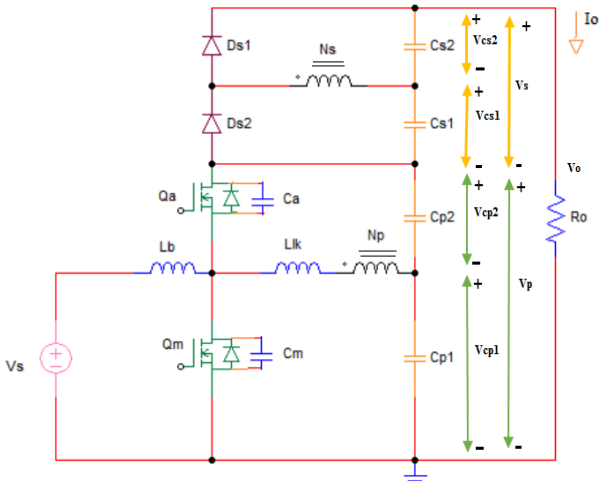

Fig.2 High gain converter based on boost integrated isolated converter [14]

IV. SIMULATION RESULTS

The simulation and the performance analyses are carried out by considering the high gain interleaved converter with built-in transformer VMC [16] as converter 1 and the high gain converter based on boost-integrated converter [14] as converter 2.The simulation parameter for the converter 1 and 2 are given in table 2. The dc-dc converters 1 and 2 are simulated using MATLAB and the results are presented from Figs.3 to 7.The gating pulsesfor converter 1 and 2 are given in Fig.3. The voltage stress across the switches for converter 1 and 2 is given in Fig.4. The voltage stress across the output diode for converter 1 and 2 is given in Fig.5. The output current for converter1 and 2 are given in Fig.6. The output voltage for converter 1 and 2 are given in Fig.7. The efficiency curve for both the converters are given in Fig.8.

Table II. Specification for Converter 1 and 2

Components	Converter 1	Converter 2
Input voltage	24V	24V
Output voltage	230V	230V
Power level	200W	200W
Switching frequency	20kHz	20kHz
Voltage gain	9.5	9.5
Duty cycle	0.58	0.58
Capacitor	$C_{c1,2}$ - 4.7 µF	$C_{P1,2}$ -100 µF
	$C_{m1,2}$ -4.7 µF	$C_{S1,2}$ -100 µF
	$C_{o1,2}$ -470 µF	
Input inductor	$L_{1,2}$ -50 µH	L_B -120 µH
Output resistance	260Ω	260Ω
Turns ratio	1	3

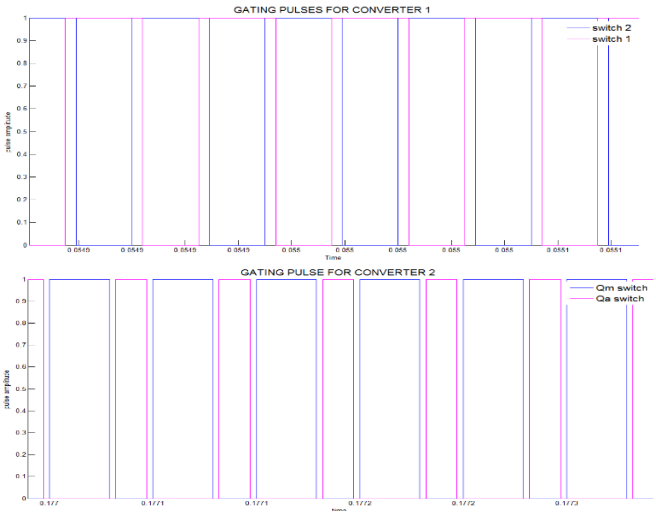

Fig.3 Gating pulses to MOSFET switches for converter 1 and 2

Fig.4 Voltage stress across the switches for converter 1 and 2

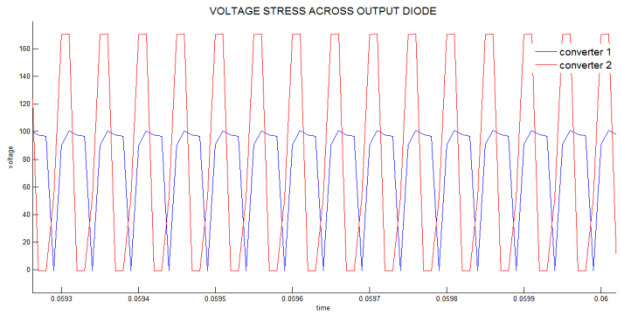

Fig.5 Voltage stress across the output diode for converter 1 and 2

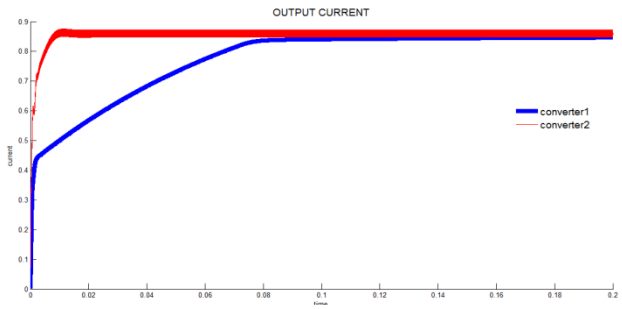

Fig.6 Output current for converter 1 and 2

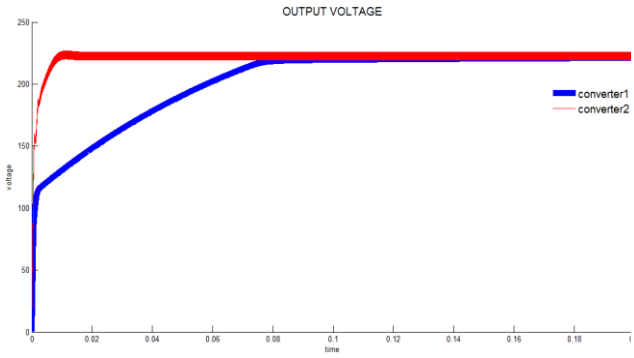

Fig.7 Output voltage for converter 1 and 2

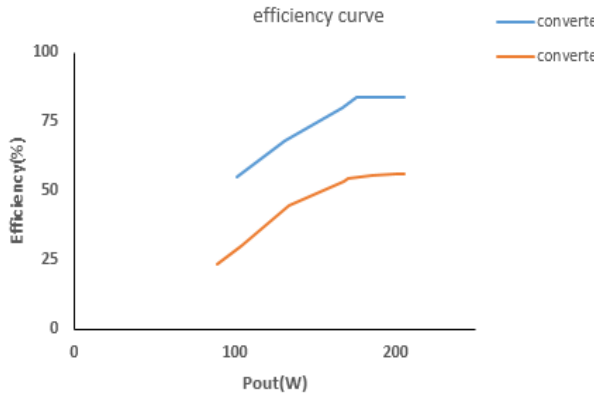

Fig.8 Efficiency curve for converter 1 and 2

V. CONVERTER 1 AND 2 AS THE FRONT END CONVERTER FOR PEF APPLICATION

The overall block diagram is given in Fig.9.The PEF circuit needs higher voltage source to produce the pulsed waveform of higher amplitude. So these converters 1 and 2 can be suitably used as a front end converter for PEF circuit to produce higher voltage level. The output from the PEF circuit is delivered to the biological load to kill the microorganism in the living cell. As a result it enhances the quality and the shelf-period of the food particles.

PEF circuit diagram is given in Fig.10. The specification parameters for the PEF circuit are given in table III.

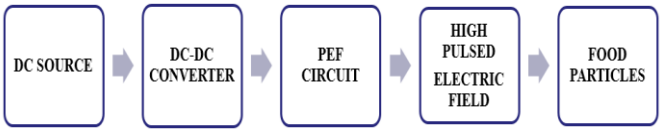

Fig.9 Block diagram

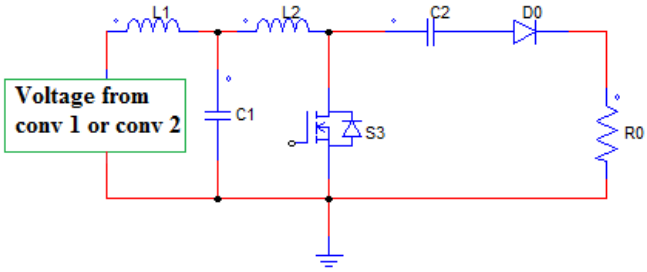

Fig.10 PEF circuit diagram

Table III-Specifications for PEF Circuit

Components	Parameters
Input voltage(V_{in})	230 V
Switching frequency(F_s)	20 kHz
Inductors (L_1,L_2)	50 µH
Input capacitor(C_1)	50 µF
Output capacitor(C_2)	1 µF

The converter 1 and 2 are connected as a front-end converter for the PEF circuitand the MATLAB simulation diagram with converter 1 as front end converter for PEF circuit is shown in Fig.11 and converter 2 as the front end converter for PEF circuit is shown in Fig.12. The simulation result after coupling the converters with the PEF circuit are given in Fig.13 and 14. The pulsed output voltage from the PEF circuit are given in Fig.13 and the current in the input side of the converters after coupling with PEF circuit are given in Fig.14.

The pulsed output voltage of the PEF circuit with converter 1 as the front end converter is about 3.5kV and with converter 2 as the front end converter is about 3.2 kV.

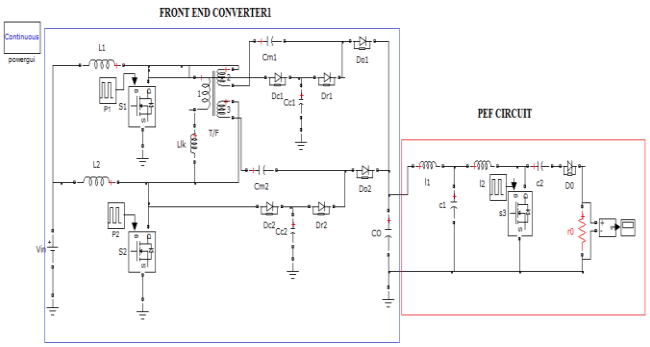

Fig.11 Simulation diagram with converter 1 as front end converter for PEF circuit

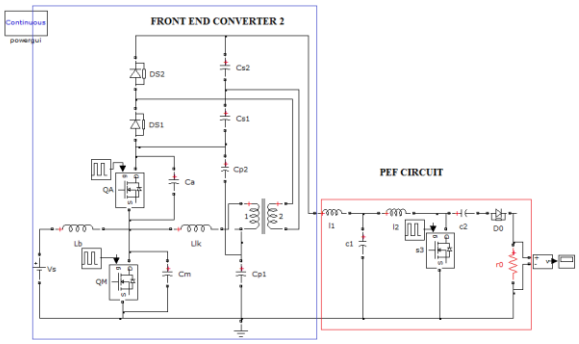

Fig.12 Simulation diagram with converter 2 as front end converter for PEF circuit

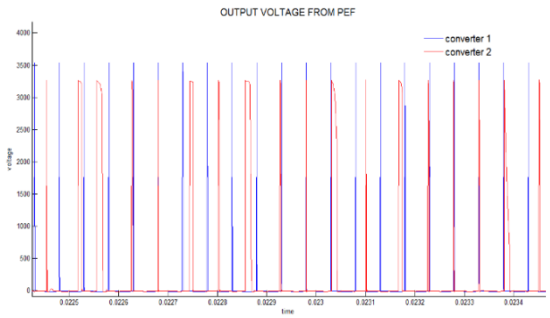

Fig.13 Pulsed output voltage from PEF circuit for converter 1 and 2

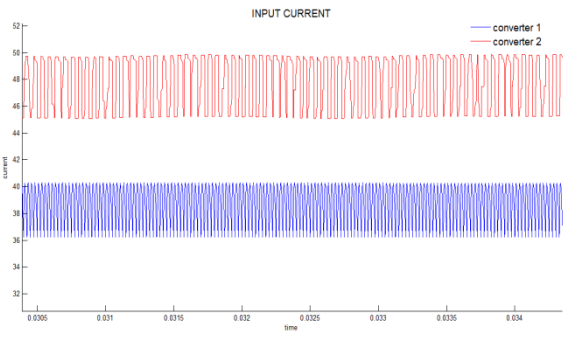

Fig.14 Input current for converter 1 and 2 after coupling with PEF circuit

VI. PERFORMANCE ANALYSIS AND DISCUSSION ON RESULTS

From the circuit diagram and the simulated results, performance analysis for the converter 1 and 2 are carried out and are provided in the table IV.

From table II it is clear that both the converters are operated with same input level of 24 V, duty cycle of 0.58 and switching frequency of 20 kHz. The output voltage of 230V and the output power of 200W are same for both the converters. In order to obtain the same voltage gain of 9.5 as converter 1, the turns ratio of converter 2 has to be maintained at 3 while for converter 1 the turns ratio is 1.

Table IV-Performance Analysis for Converter 1 and 2

Parameters	Converter 1	Converter2
Switch voltage stress	45V	60V
Output diode voltage stress	100V	170V
Turns ratio	1	3
Efficiency	85%	53%
Output voltage after coupling PEF	3.5kV	3.2kV
Input current after coupling PEF	40A	50A

From table IV it is evident that switch voltage stress, output diode voltage stress and converter input current are less for converter 1 than converter 2. The efficiency of converter 1 is 60% higher than converter 2 and the output voltage from PEF circuit for converter 1 has higher amplitude than converter 2.

All these analysis and simulation results portrays that converter 1 is best suited as the front end converter for PEF application. Since the input current, voltage stress, turns ratio of transformer are lesser for converter 1, the rating of devices used for converter 1 are lower than that of converter 2. This reduces the cost of overall system with an improved efficiency.

VII. CONCLUSION

This paper presents a comparison between two high gain dc-dc converters where in both the converters VMC are used to improve the voltage conversion ratio. The simulation results and the performance comparison between the converters reveals that converter 1 is more advantageous for PEF application over converter 2. The converter 1 has the following major advantages:

- ZCS soft switching technique is used and the diode reverse recovery problems are eliminated.
- The efficiency of converter 1 is more than that of converter 2 by 60%.
- Voltage stress across the diode is 100 V which is lower than the output voltage level 230 V.

- Built-in transformer provides an additional control freedom to achieve the higher voltage conversion ratio.
- Diode peak current and current ripples are reduced compared to conventional boost converter.

Hence it can be concluded that converter 1 can be suitably used as a front-end converter for PEF applications to produce pulsed output voltage of higher amplitude which have a great impact in destroying the microorganism and thereby increasing the quality and shelf period of the food particles.

ACKNOWLEDGMENT

The authorsthank SSN College of engineering for the financial support provided to carry out this research work.

REFERENCES

[1] "Pulsed Electric Fields for Food Processing Technology", Maged E.A. Mohamed and Ayman H. AmerEissa, Department of Agriculture Engineering, Faculty of Agricultural, Minoufiya University, Egypt Date Palm Research Center, King Faisal University, Saudi Arabia

[2] Tao Tang, Fei Wang, AndrasKuthi, and Martin A. Gundersen, "Diode Opening Switch Based Nanosecond High Voltage pulse Generators for Biological and Medical Applications" Department of Electrical Engineering- Electrophysics, University of Southern California Los Angeles, CA 90089-0271, USA

[3] F. Zhang, L. Du, F. Z. Peng, and Z. Qian, "A new design method for high-power high-efficiency switched-capacitor DC–DC converters," IEEE Trans. Power Electron., vol. 23, no. 2, pp. 832–840, Mar. 2008

[4] C. P. SaiKiran, M. Vishnu Vardhan and K. Eswaramma,"ZVT Boost Converter Employing Auxiliary Resonant Circuit in PV Energy Systems", SSRG International Journal of Electrical and Electronics Engineering (SSRG-IJEEE) – vol. 1 Issue 9 Nov 2014

[5] W. Li and X. He, "A family of interleaved DC/DC converters deduced from a basic cell with winding-cross-coupled inductors (WCCIs) for high step-up or step-down conversions," IEEE Trans. Power Electron.,vol. 22, no. 4, pp. 1499–1507, Jul. 2008.

[6] Y. Zhao,W. Li, and X. He, "Single-phase improved active clamp coupledinductor-based converter with extended voltage doubler cell," IEEE Trans.Power Electron., vol. 27, no. 6, pp. 2869–2878, Jun. 2012

[7] Manish.G.Rathi and Gururaj.Sajjan,"Transformer-less High gain Boost Converter with Input Current Ripple Cancellation at SelectableDuty Cycle" SSRG International Journal of Electrical and Electronics Engineering (SSRG-IJEEE) – volume 2 Issue 1 Jan 2015

[8] L. S. Yang, T. J. Liang, H. C. Lee, and J. F. Chen, "Novel high step-upDC–DC converter with coupled-inductor and voltage-doubler circuits," IEEE Trans. Ind. Electron., vol. 58, no. 9, pp. 4196–4206, Sep. 2011

[9] W. Li, Y. Zhao, Y. Deng, and X. He, "Interleaved converter with voltage multiplier cell for high step-up and high efficiency conversion," IEEE Trans. Power Electron., vol. 25, no. 9, pp. 2397–2408, Sep. 2010

[10] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, andR. Gules, "Voltage multiplier cells applied to non-isolated DC–DC converters," IEEE Trans. Power Electron., vol. 23, no. 2, pp. 871–887,Mar. 2008

[11] W. Li, W. Li, X. He, D. Xu, and B. Wu, "General derivation law of non-isolated high step-up interleaved converters with built-in transformer,"IEEE Trans. Ind. Electron., vol. 59, no. 3, pp. 1650–1661, Mar. 2012

[12] Y. Deng, Q. Rong, W. Li, Y. Zhao, J. Shi, and X. He, "Single switch high step-up converters with built-in transformer voltage multiplier cell," IEEE Trans. Power Electron., vol. 27, no. 8, pp. 3557–3567 Aug. 2012

[13] D.Santhoshkumar and P.Varunkrishna,"Single-Phase Isolated Converter For Ripple Current Reduction"SSRG International Journal of Electrical and Electronics Engineering (SSRG-IJEEE) – volume 1 Issue 7-Sep 2014

[14] K. B. Park, G. W. Moon, and M. J. Youn, "Non-isolated high step-up stacked converter based on boost-integrated isolated converter," IEEETrans. Power Electron., vol. 26, no. 2, pp. 577–587, Feb. 2011

[15] W. Li, X. Xiang, C. Li, W. Li, and X. He, "Interleaved high step-up ZVT converter with built-in transformer voltage doubler cell for distributed PV generation system," IEEE Trans. Power Electron., vol. 28, no. 1, pp. 300–313, Jan. 2013

[16] Wuhua Li, Weichen Li, Xin Xiang, Yihua Hu, and Xiangning He, "High step-up interleaved converter with built-in transformer voltage multiplier cells for sustainable energy applications" IEEE Trans. Power Electron.., vol. 29, no. 6, June 2014