# Comparative Study of THD Spectrum on Switched Capacitor Inverter

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***Abstract***

*Multilevel inverter is a commonly used power electronic device because of its characteristics of synthesizing a sinusoidal output on several steps. They give good quality output resulting with lower harmonic distortion in the output. This topology is designed based on Switched Capacitor with charge pump technique and the number of output levels is determined by the number of Switched Capacitor (SC) cells used. A small input voltage can be used to produce a boosted output voltage, by switching the capacitors in series and in parallel by properly switching the power electronic switches. Number of switching devices used in the circuit is reduced as compared to the conventional cascaded multilevel inverter. This work also presents the comparative study of controllers using various Multicarrier Pulse Width Modulation (MCPWM) techniques. Performance factors such as % THD, voltage stress, ripple voltage etc. are measured for different modulation techniques and the results are studied. MCPWM method with the different modulating signal based PWM such as Sinusoidal Multicarrier PWM, Sampling PWM, Rectified Sinusoidal PWM and Trapezoidal PWM has been analyzed. The simulations are done with MATLAB/ SIMULINK software. From the simulation results seven level inverter shows less THD using Alternate Phase Opposition Disposition (APOD) PWM. The control strategy is the key part for the circuit and switching signals are generated with the help of PIC16F877A microcontroller.*

**Keywords** — *Multilevel Inverter, charge Pump, Charging, Single DC Source, Switched Capacitor*

## I. INTRODUCTION

Inverter performs DC to AC conversion for distributed electrical energy systems and electrical vehicles. In recent years, multilevel inverters are attracting lot of attentions due to the increasing higher power quality requirements. It possesses the several features such as reduced harmonic distortion, near sinusoidal output voltage waveform and reduces *dv/dt* stress.

One of the significant advantages of multilevel inverter configuration is the harmonic reduction in the output waveform without increasing the switching frequency or decreasing the inverter power output. Conventionally, multilevel inverters are classified in to two categories: Type 1 and Type 2. Type 2 inverter uses multiple DC voltage capacitors; neutral point clamped [1] and flying capacitors. Type 1 inverter uses multiple DC voltage sources; cascaded H-bridge inverter [2]. Type 1 inverters are again divided in to two: symmetrical and asymmetrical inverters. In cascaded symmetrical inverters all the DC voltage sources are equal where as asymmetrical inverter uses unequal voltage sources. However, their drawbacks are also apparent such as Cascaded H – bridge inverte requires multiple separate dc sources. Problem of voltage balancing among DC link and clamping capacitors exists in both neutral point clamped and flying capacitor inverters [2]. Diode clamped or neutral clamed has the difficulty of increase in the number of clamping diodes as the level increases. Similarly, in flying capacitor the number of capacitors increases and system becomes bulkier. Among these inverter topologies cascaded inverter achieves greater reliability and simplicity because it does not requires any power electronic devices other than switches and capacitor voltage balancing technique.

From normal inverter, magnitude of the inverter output is same as that of input voltage when the modulation index is equal to one. To offer output voltage greater than input we have to use a DC-DC boost converter. Other method is to use inductors or transformers but at higher power, transformer should withstand heavy magnetic core so that it can sustain higher power level [3]. As a solution charge pump [20] technique is used with switched capacitors, which does not requires any inductors. Charge pump technique generates larger output voltage from a small DC voltage with a switched capacitor [3]-[5].

Multilevel inverters are mainly controlled by Multicarrier Pulse Width Modulation method and the harmonic contents can be reduced by using PWM techniques [6]. There are two PWM methods mainly used in multilevel inverter control strategy [7]. One is fundamental switching frequency and another one is high switching frequency. The high switching frequency strategy is classified as space vector PWM, Selective Harmonic Elimination PWM and Sinusoidal Pulse Width Modulation (SPWM). Among these PWM methods SPWM is mostly used for the multilevel inverter, because it is very simple and easy to implement. In this paper, SPWM method with the different carrier based PWM such as Phase Disposition (PD) PWM, Phase Opposition Disposition (POD) PWM, Alternate Phase Opposition Disposition

(APOD) PWM, Variable Frequency (VF) PWM, Carrier Overlapping (CO) PWM and Sampling PWM has been analysed [6] [7].

In this paper, the performance analysis of switched capacitor seven level inverter is evaluated using APOD technique.

## II. CIRCUIT TOPOLOGY OF SEVEN LEVEL INVERTER

A boost switched-capacitor (SC) multilevel inverter is formed by cascading two structures, a switched capacitor network and a two level inverter [6] - [8]. By cascading N-number of switched capacitor cells generates (2N+3) levels in the output and the maximum output voltage is $(N+1)V_{dc}$. Only one DC voltage source is needed and the problem of capacitor voltage balancing is avoided. One basic switched capacitor cell is formed by one capacitor, one switching devices with two diodes as shown in figure 1. Each of these cells is connected in parallel with each other to increase the number of levels required in the multilevel output. Each cell is made to operate as a parallel-series converter, when the switch $S_a$ is turned off and common switch $S_b$ is turned ON; the capacitor comes in parallel with the source by the forward biased diodes. And when the switch $S_a$ is turned ON; charged capacitor is in series with the input source. The proper switching of these devices is required for obtaining the desired output. Each switched capacitor cells are connected across the input DC source through a common switch $S_b$ shown in figure 2.

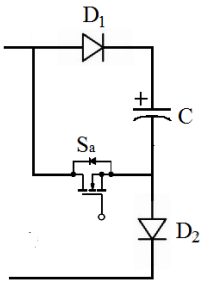



**Fig 1: Proposed Switched Capacitor Cell**

Figure 2 shows the structure of seven level inverter. A Switched Capacitor (SC) circuit is used in order to obtain a boost multilevel DC voltage waveform, which is inserted between the source and the full bridge inverter [8]. The multilevel AC output voltage of the switched capacitor circuit is the input voltage of the full bridge inverter, resulting in a staircase output voltage waveform. The multilevel output voltage is larger voltage than the input voltage by connecting the capacitors in series and in parallel to the input.

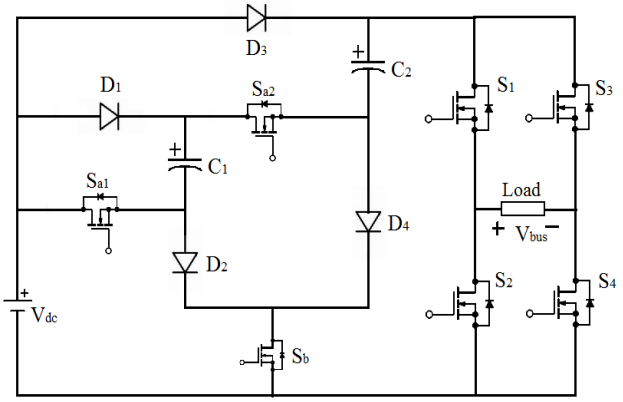



**Fig 2: Circuit diagram of Seven Level Inverter**

Such a multilevel waveform is close to a sinusoidal, its harmonic content can be reduced when compared to the conventional multilevel inverter by using the PWM control strategy.

## III. OPERATING PRINCIPLE OF SEVEN LEVEL INVERTER

A switched capacitor multilevel inverter which is capable of giving a maximum of seven level is analyzed here, the number of capacitor cells to be used in the circuit are N=2. When the capacitor and the input voltage source are connected in parallel, the capacitors are charged. When the capacitor and input voltage source are connected in series, the capacitors are discharged.

### A. *Mode 1 ($V_{bus}$ = 0 V )*

All capacitors are made in parallel with the input source voltage by turning ON the switch $S_b$, thus each capacitor maintains an input voltage across it. Switches in same upper/lower limb conduct either $S_2$ and $S_4$ or $S_1$ and $S_3$ are turned ON to produce the zero voltage at the output shown in figure 3.

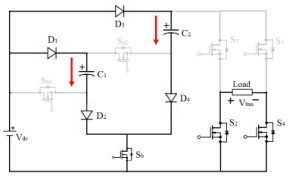


**Fig 3: Mode 1**

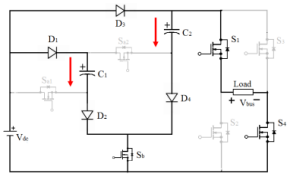


**Fig 4: Mode 2**

### B. *Mode 2 ($V_{bus} = V_{dc} - V_f$)*

In this mode switches $S_1$ and $S_4$ of full bridge inverter are turned ON to generate the first level, which is equal to $(V_{dc} - V_f)$ shown in figure 4. Where $V_f$ is the forward voltage drop of diode $D_3$. Switch $S_b$ is also ON to make the capacitor to get charged.

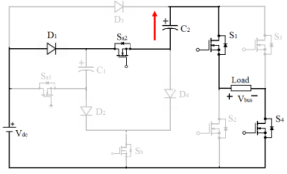


**Fig 5: Mode 3**

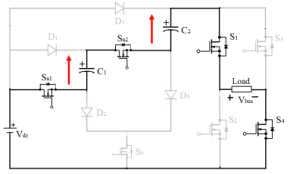


**Fig 6: Mode 4**

### C. Mode 3 ($V_{bus} = V_{dc} + V_{C2} - V_f$)

This is the mode when one capacitor is connected in series. The capacitor $C_2$ is connected in series with the source by simultaneous turning ON of switch $S_{a2}$ shown in figure 5. The switches $S_1$ and $S_4$ of full bridge inverter are conducting in this period. So the output voltage is ($V_{dc} + V_{C2} - V_f$ ). Where $V_f$ is the forward voltage drop of diode $D_1$ and $V_{C2}$ is the voltage of capacitor $C_2$.

### D. Mode 4 ($V_{bus} = V_{dc} + V_{C1} + V_{C2}$)

In this mode all the two capacitors are connected in series. The capacitor $C_1$ and $C_2$ are connected in series with the source voltage by making switches $S_{a1}$ and $S_{a2}$ conducting shown in figure 6. The switches $S_1$ and $S_4$ of full bridge inverter are conducting in this period. So the last voltage level is ($V_{dc}$ + $V_{C1}$ +$V_{C2}$ ). Where $V_{C1}$ is the voltage of capacitor $C_1$ and $V_{C2}$ is the voltage of capacitor $C_2$.

Similarly the negative half cycle can be obtained by turning ON $S_2$ and $S_3$ instead of $S_1$ and $S_4$, thus seven level output can be obtained. The maximum voltage stress across each of the switches of switched capacitor network is the input voltage.

## IV. PULSE WIDTH MODULATION SCHEMES

To control and to generate high quality output waveform, an appropriate modulation scheme is required. Among the various modulation schemes, an important family of modulation technique, multicarrier pulse width modulation stands out because it offers significant simplicity and easy to implement switching waveforms. The frequency ratio $m_f$ is defined in the relation (1)

$$m_f = \frac{f_c}{f_m} \quad (1)$$

where, $f_c$ is the carrier (triangular) signal frequency

$f_m$ is the modulating signal frequency

The amplitude modulation index $m_a$ is defined as

$$m_a = \frac{2A_m}{(m-1)\,A_c} \quad (2)$$

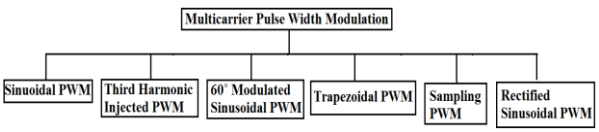
where, $A_m$ is the amplitude of the modulating signal

$A_c$ is the peak amplitude of the carrier signal

m is the number of output levels

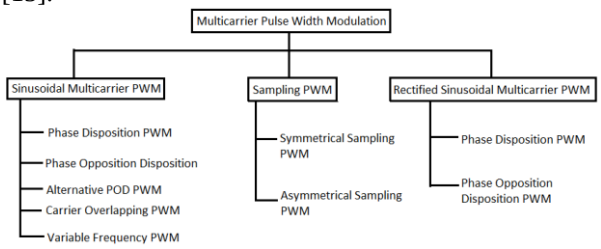
### Type of Modulating Signals

This work focuses on multicarrier based Sinusoidal PWM, Sampling PWM, Rectified Sinusoidal PWM and Trapezoidal PWM Strategies which have been used in chosen Multilevel Inverter [14] - [16].




### Types of carriers

In this section, simplified way to generate different type of carrier signals are illustrated [14] - [15].




### A. Sinusoidal Multicarrier PWM

For an m-level inverter, (m-1) carriers with same carrier frequency are continuously compared with the sinusoidal reference waveform. Sinusoidal Phase Disposition (PD) uses six triangular carrier and all the carriers are in phase with each other shown in figure 7. In Phase Opposition Disposition (POD) the carrier signals above the zero axis and below the zero axis have same frequency, same amplitude and but 180˚ out of phase [6] - [8]. But in Alternative Phase Opposition Disposition (APOD) alternate carriers are phase shifted by 180˚ from its neighbour. The Principle of Variable Frequency (VF) PWM technique is to use the several carriers of different frequencies with single modulating waveform. In the Carrier Overlapping (CO) technique, 6 carriers are disposed such that the bands they occupy overlap each other, the overlapping vertical distance between each carrier is $\frac{A_c}{2}$ ($A_c$=1) [6] - [8].

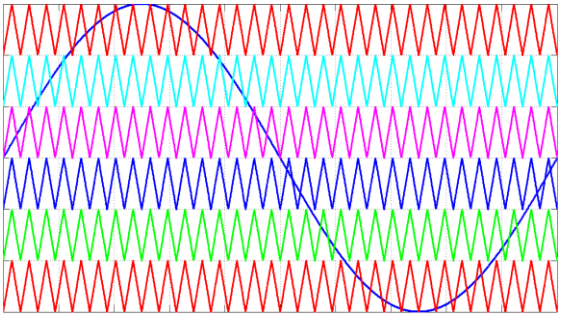


**Fig 7: Sinusoidal Phase Disposition PWM**

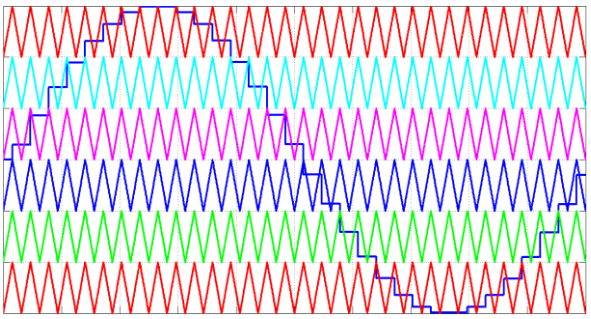


**Fig 8: Symmetrical Sampling PWM**

### B. Sampling Multicarrier PWM

The Principle of this PWM technique is to use the several carriers compared with sampled

version of sinusoidal modulating waveform. Six triangular carrier waveforms are compared with one sampled sinusoidal reference waveform for seven level output. Sampling PWM technique is classified based on the sampling instant. In symmetrical sampling, sampling is carried out at the instant of positive peak of the carrier only shown in figure 8. But in asymmetrical sampling, sampling is carried out at the positive and negative peak of the triangular carrier [29].

### C. *Rectified Sinusoidal Multicarrier PWM*

For an m-level inverter, $\frac{(m-1)}{2}$ carriers with same frequency $f_c$ and same peak-to-peak amplitude $A_c$ are continuously compared with rectified sinusoidal reference waveform having amplitude $A_m$ and frequency $f_m$ shown in figure 9. In this technique, number of carriers required is less compared to other PWM techniques.

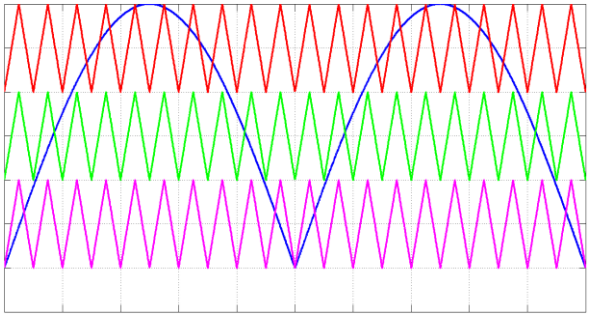


**Fig 9: Rectified Sinusoidal PWM**

### D. *Trapezoidal PWM*

This scheme uses trapezoidal modulating signal with multiple triangular carriers shown in figure 10. The intersection between the trapezoidal signal and carrier signal defines the switching instant of the PWM pulse.

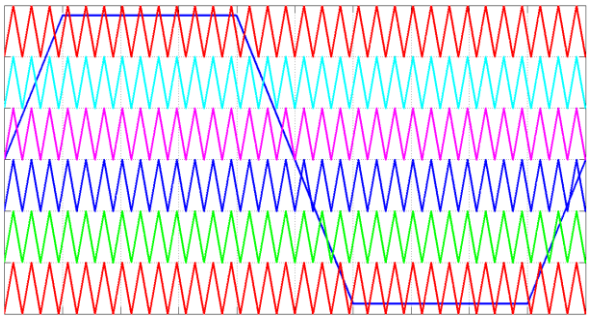


**Fig 10: Trapezoidal PWM**

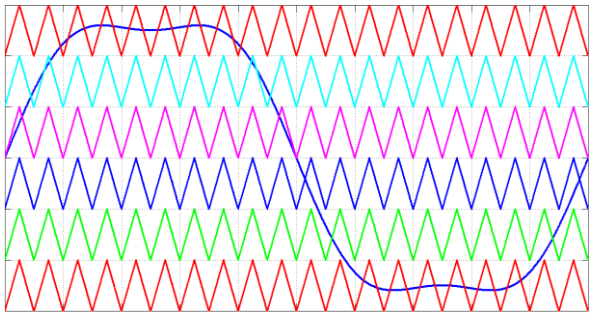


**Fig 11: Third Harmonic Injected PWM**

### E. *Third Harmonic Injected PWM*

Injecting third harmonic in the pure sinusoidal signal is known as Third Harmonic Injected PWM shown in figure 11. By flattering the top of the reference signal not only increases the linear modulation range but also increases the fully utilization of the DC link voltage. It improves the inverter performance.

### F. *$60^0$Modulated Sinusoidal PWM*

In this PWM technique the modulating signal is flattened by limited the amplitudes of sinusoidal signal to $60^0$, i.e., clamped the sinusoidal signal with $60^0$ angles or higher than this angle. Variation in angle would decide the quality of the output waveform. Generation of signal is shown in figure 12.

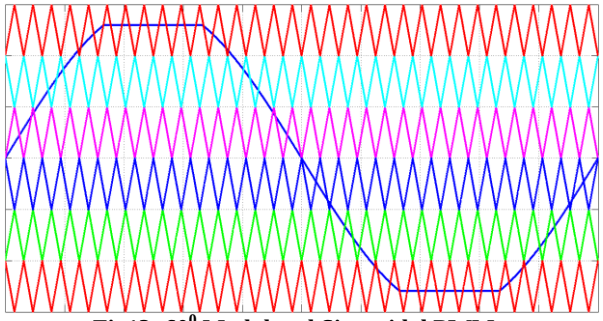


**Fig12: $60^0$ Modulated Sinusoidal PWM**

### G. *Switching Strategy for Switched Capacitor Cell*

Switched Capacitor network has two switching situations in each quarter cycle. Each SC cell switch turns ON in the first quarter cycle at a predetermined angle ( $\theta_i$ ), and turns OFF at a respective angle $(\pi - \theta_i)$ in the second quarter cycle shown in figure 13. These switching patterns repeat every half cycle. Duty Cycle of the SC cell is:

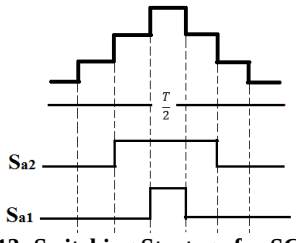



**Fig 13: Switching Strategy for SC cell**

$$D = \frac{T_{on}}{T/2} \quad (3)$$

Where, $T_{on}$ = ON duration of Switch

T = Time period of Switching Pulse

Switching pulses for switched capacitor network ($S_{a1}$ & $S_{a2}$) are based on the "FIRST ON LAST OFF" (FOLO), since the first SC cell is turned ON, will be the turned OFF last. And the SC cell turned ON last will turned OFF first [21].

## V. SIMULATION AND RESULTS

For an input of 5V, switching frequency $f_c$ as 1kHz and reference frequency $f_m$ as 50Hz, the proposed multilevel inverter was simulated in Matlab Ra2014a. The capacitance $C_i$ can be determined properly with considering the voltage ripple of the capacitors $C_i$. The smaller voltage ripple of these capacitors leads to the higher efficiency.

### A. Gate Pulse Generation

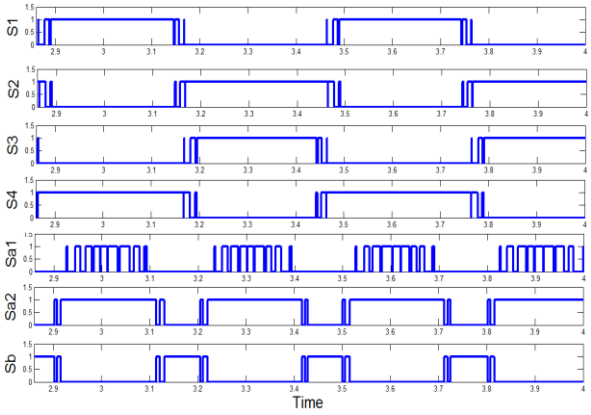



**Fig 14: Switching Pulses using APOD techniques**

Gate signals are obtained by comparing sinusoidal reference or modulating signal at fundamental frequency (50Hz) with triangular carrier signal which are at higher frequency. Here switching frequency is selected as 1kHz for better performance or a carrier to fundamental frequency ratio of 20. Figure 14 shows the seven switching pulses using APOD technique.

### B. Output Voltage and output current

In seven level inverter output contains three steps. First step is the input voltage, because full bridge switches are turned ON, such that load is connected across the input source. In the next step voltage equals to sum of input DC voltage and capacitor voltage. Similarly for the third level is the sum of input DC and all the series connected capacitor voltages. Figure 15 show the seven level output voltage using Alternative Phase Opposition Disposition PWM technique.

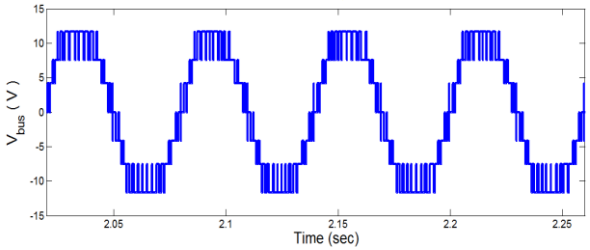



**Fig 15: Output Voltage (R Load)**

Figure 16 shows the Seven level output current of the inverter.

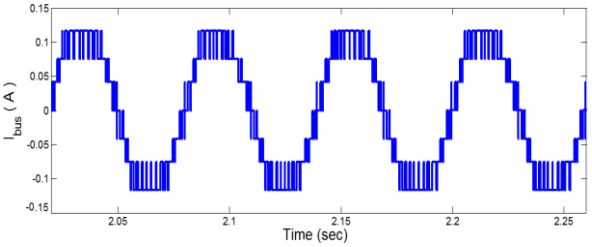



**Fig 16: Output Current (R Load)**

### C. Voltage Stress across the Switches

Figure 17 shows the voltage stress across the seven switches using Alternative Phase Opposition Disposition PWM technique. From the simulation, voltage drop across the switches in the full bridge inverter is 11.8V. Voltage stress across switch $S_{a1}$is 4.2V and $S_{a2}$ is 3.4V. For a common switch $S_b$ is 7.6V.

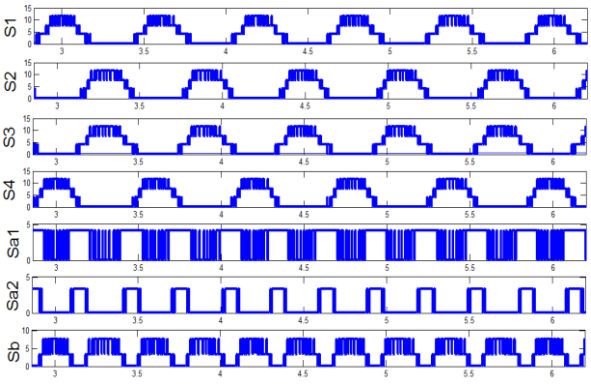



**Fig17: Voltage Stress of Switches**

## VI. SIMULATION ANALYSIS

### A. Switching Angle Calculation

For a multilevel inverter each level is occurred at a particular switching angle. Seven level inverter has three switching angles corresponding to three levels shown in figure 18. For any level inverter switching angles are calculated using the equation (4)

$$\theta_j = \sin^{-1}\left(\frac{2j-1}{m-1}\right) \quad (4)$$

Where, j = 1, 2,…….$(\frac{m-1}{2})$

m = output levels

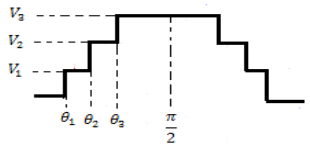



**Fig 18: Calculation of Switching Angles**

Corresponding switching angles $\theta_1$, $\theta_2$ and $\theta_3$ are calculated using the relation (4).

### *B. RMS Output Voltage*

RMS value of the output voltage is calculated using the switching angles of each output step. For the seven level output three switching angles are generated. From results RMS value of output voltage can be calculated using the equation (5)

$$V_{rms}= \sqrt{(\frac{2}{\pi})(V_1{}^2(\theta_2-\theta_1)+V_2{}^2(\theta_3-\theta_2)+V_3{}^2(\frac{\pi}{2}-\theta_3))} \quad (5)$$

RMS value of the fundamental output voltage component can be calculated using the step voltage and switching angle as shown in equation (6)

$$V_{1rms}= \frac{V_1}{\sqrt{2}} \quad (6)$$

$$=\left(\frac{2\sqrt{2}}{\pi}\right)(V_1\cos\theta_1+(V_2-V_1)\cos\theta_2+(V_3-V_2)\cos\theta_3)$$

### *C. FFT Spectrum*

Figure 19 shows the FFT spectrum of output voltage using the Alternative Phase Opposition Disposition technique with a modulation index $m_a = 1$. Here %THD is calculated by considering 30 cycles of output voltage with a fundamental frequency of 50Hz.

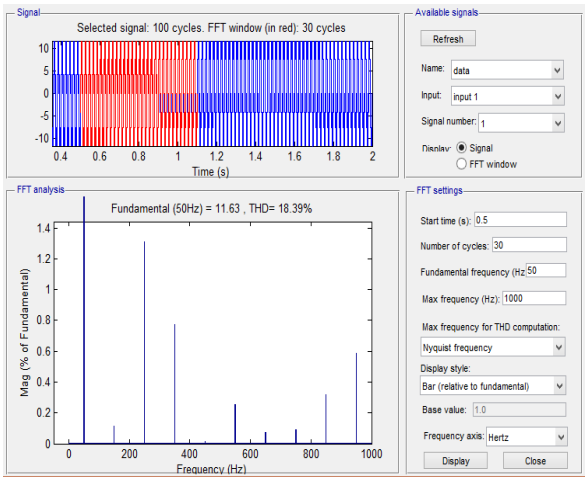



**Fig *19: FFT Spectrum Output Voltage***

### *D. Total Harmonic Distortion*

The main criterion for assessing the quality of the voltage delivered by an inverter is the Total Harmonic Distortion (THD). The THD is a ratio between the Root Mean Square (RMS) of the harmonics and the fundamental signal.

$$THD = \sqrt{\left(\frac{V_{rms}^2}{V_{1}^2{}_{rms}}-1\right)} \quad (7)$$

From the above two analysis substitute the values of output RMS and fundamental RMS value to find the THD.

In this work, %THD of the seven level inverter is studied using different modulation Techniques like sinusoidal and trapezoidal PWM with same circuit components.

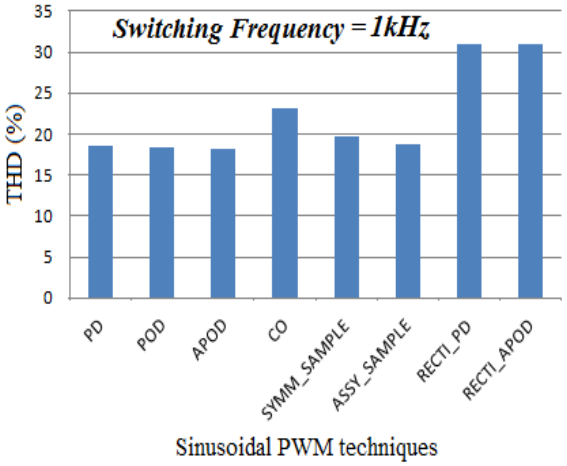



**Fig 20: %THD Vs Modulation Techniques**

Figure 20 shows the variation in %THD with different sinusoidal PWM techniques. From this graph Alternative Phase Opposition Disposition (APOD) shows minimum %THD compared to other techniques for a 1kHz switching frequency.

Figure 21 shows the %THD using different sinusoidal PWM techniques. Using the sinusoidal PWM techniques, Alternative Phase Disposition techniques (APOD) shows the minimum THD for all switching frequency between 1 kHz and 50kHz.

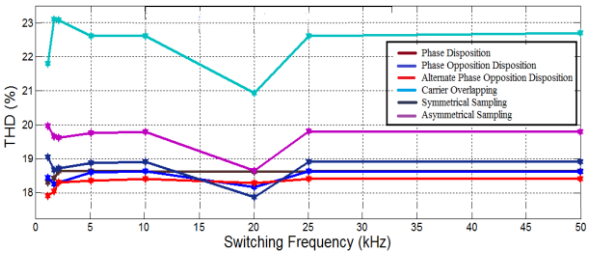



**Fig 21: %THD Vs Switching Frequency for Sinusoidal Modulation**

Figure 22 shows the %THD using different Trapezoidal PWM techniques. Using the trapezoidal PWM techniques, Phase Disposition (PD) techniques shows the minimum THD for all switching frequency. But its THD value is higher than that obtained from the sinusoidal APOD PWM.

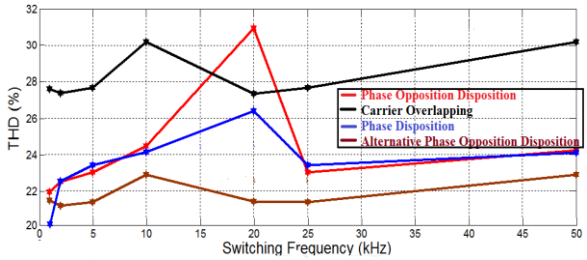



**Fig 22: %THD Vs Switching Frequency for Trapezoidal Modulation**

Figure 23 shows the THD with different switching frequency for Alternative Phase Opposition Disposition (APOD) PWM techniques. From the graph minimum %THD occur at lower switching frequency (in kHz). Above 25kHz %THD almost constant.

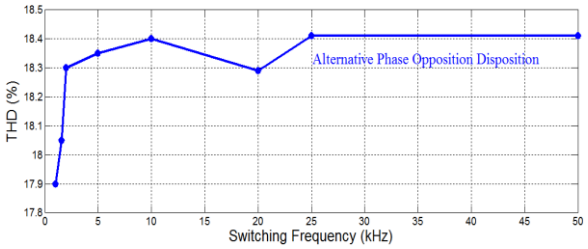



**Fig 23: %THD Vs Switching Frequency for APOD Technique**

From all the analysis Sinusoidal APOD is the best suited PWM technique and 1kHz is the optimum switching frequency.

## VII. EXPERIMENTAL SETUP AND RESULTS

Figure 24 shows the experimental setup of switched capacitors seven level inverter. For the hardware prototype, 1000µF capacitor and 100Ω, 5W load resistor is used.

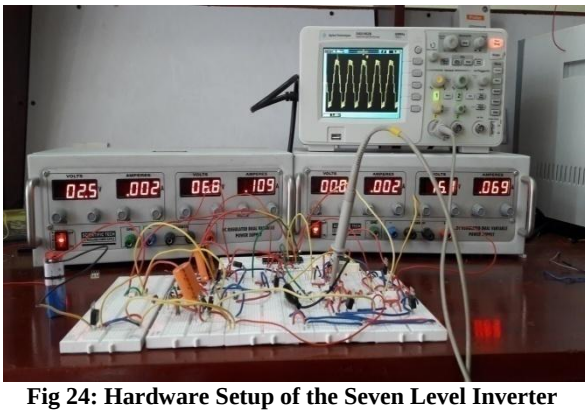


**Fig 24: Hardware Setup of the Seven Level Inverter**

To control MOSFET (IRF540), pulses are created using PIC16F877A microcontroller based on Alternative Phase Opposition Disposition (APOD) modulation technique, because APOD gives less %THD for all switching frequency. These control pulses are amplified using an optocoupler TLP250 Driver/Optocoupler IC. Figure 25 shows the seven level output voltage of the proposed inverter.

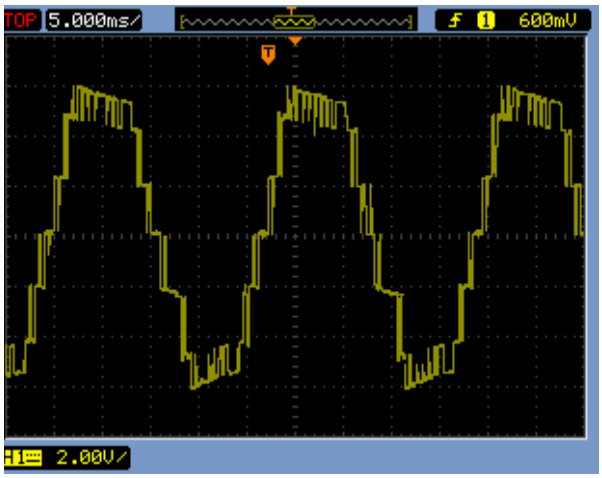



**Fig 25: Experimental Result of Seven Level Inverter**

## VIII. CONCLUSIONS

In this paper, step up switched capacitor multilevel inverter is studied, which is a combination of DC – DC converter and a full bridge inverter. DC – DC converter comprises of several cascaded switched capacitor cells. This SC multilevel inverter uses very less number of switching devices compared to conventional inverters and existing switched capacitor multilevel inverters. Simplified method to generate simulation model for multicarrier PWM techniques based on various carrier signals and modulating signals are presented. Alternative Phase Opposition Disposition technique produces less THD among all the multicarrier PWM techniques. Operation and performance analysis of proposed inverter are studied with seven level inverter prototype. From the study, control strategies with unity modulation index generate lower percentage of total harmonic distortion using Sinusoidal Alternative Phase Opposition Disposition technique.

## ACKNOWLEDGEMENT

Fore mostly, I would like to express my sincere gratitude to our Principal Dr. Soosan George T and HOD Prof. Acy M Kottalil for imparting fundamental idea, which helped me a lot for my project. I express my deep sense of gratitude to Prof. Beena M Varghese and Dr. Bos Mathew Jos for the valuable guidance as well as timely advice which helped me a lot in completing the paper successfully.

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