An Investigation of THD in 5-level NPC Multilevel Inverter Based on Multicarrier PWM Techniques

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Abstract

This paper presents an investigation of the Total Harmonic Distortion in 5-level neutral point clamped multilevel inverter using 4 strategies of multicarrier PWM techniques; Phase Disposition, Phase Opposition Disposition, Phase Opposition Disposition with different frequencies, and Alternative Phase Opposition Disposition. The signals of the controlled switches of the multilevel inverter based on 4 strategies of multicarrier PWM techniques created by a TMS320F28335 DSP controller are proposed in this paper. Experimental results by varying the modulation index (m_a) in the range of 0.4 to 1, the lowest percentage of the THD of the system is produced when the multilevel inverter is controlled by the PD modulation technique. The %THDv and the %THDi are 9.3 and 9.6, respectively, when the prototype of the multilevel inverter with a resistive load 50 Ω and an inductive load 8 mH is controlled by the PD modulation technique using $m_a = 0.9$.

Keywords — Neutral point clamped multilevel inverter, Multicarrier PWM techniques, Total harmonic distortion.

I. INTRODUCTION

Multilevel inverters are power conversion systems made to synthesize a desired AC voltage from several levels of DC link voltages. The numbers of levels of the multilevel inverter is defined as the number of steps which can be generated between the output terminal and the reference node denoted by n. The inverter with the number of voltage levels equals to three or above which is known as the multilevel inverter. The number of voltage levels increases, there is a low Total Harmonic Distortion (THD) for the output voltage.

The multilevel inverter has high efficiency because the devices can be switched at a low frequency. The topologies of the neutral point clamped, flying capacitor, and cascades multilevel inverters have the potential for applications in high power systems [1-3]. This paper mainly focuses on the neutral point clamped multilevel inverter topology since the modularity of the neutral point clamped multilevel inverter can be stacked easily for high power and high voltage applications.

The advantages of the Sinusoidal Pulse Width Modulation (SPWM) technique are the real time control, good transient response, and constant average switching frequency [4]. However, the elimination of lower order harmonics of this technique will increase the next higher level harmonics. There are four alternative SPWM strategies with different phase relationships; Phase Disposition (PD), Phase Oppo-sition Disposition (POD), Phase Opposition Dispo-sition with different frequencies (PODf), and Alterna-tive Phase Opposition Disposition (APOD). The PD modulation technique, the significant harmonics are concentrated at the carrier frequency. This method is generally accepted that gives rise to the lowest harmonic distortion in higher modulation index [5]. The POD modulation techniques, the significant harmonics are located around the carrier frequency [6]. The PODf technique is same as the POD method, but the frequency modulation for top and bottom bands is less than the frequency modulation for intermediate bands [7]. The APOD modulation technique, the significant harmonics are centered as side bands around the carrier frequency [8].

In this paper, 4-alternative SPWM signals; PD, POD, PODf, and APOD, created by a TMS320F28335 DSP controller are presented. These signals are used to control the 5-level full-bridge neutral point clamped multilevel inverter (FNPCMI) for investigation the THD by varying the amplitude modulation index in the range of 0.4 to 1.

II. 5-LEVEL NEUTRAL POINT CLAMPED MULTILEVEL INVERTER

The diode clamped multilevel inverter is well known as the neutral point clamped multilevel inverter. The staircase output voltage of the diode clamped multilevel inverter depends on several levels of DC voltages developed by DC capacitors. If *m* is defined as the number of level, the number of capacitors are (*m*-1), the number of power electronic switches per phase are 2(*m*-1), and the number of diodes per phase are 2(*m*-2). The DC bus voltage is split into five levels using four capacitors is shown in Fig. 1. The voltage across each capacitor is $V_{dc}/4$ and the voltage stress across each switch is limited to one capacitor voltage through clamping diodes. The switching sequence of a single-phase full-bridge five-level neutral point clamped multilevel inverter (FNPCMI) is shown in Table I.

Output Voltage	Switch State							
V _{An}	S_1	<i>S</i> ₂	S ₃	<i>S</i> ₄	<i>S</i> ₁ '	<i>S</i> ' ₂	<i>S</i> ' ₃	<i>S</i> ' ₄
V _{dc} / 2	1	1	1	1	0	0	0	0
V _{dc} /4	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_{dc}$ / 4	0	0	0	1	1	1	1	0
– V _{dc} / 2	0	0	0	0	1	1	1	1

TABLE I. OUTPUT VOLTAGE LEVEL OF 5-LEVEL FNPCMI

In Fig. 1, the phase output voltage V_{An} has five states: $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/4$, and $-V_{dc}/2$. Fig. 2 shows the topology of two phase legs of the 5-level FNPCMI that the sinusoidal pulse width modulation signal used to control the multilevel inverter consists of two sinusoidal signals displaced at mutually 120°.



Fig 1: One-phase leg of 5-level FNPCMI



III.MULTICARRIER PWM TECHNIQUES

For the conventional Multilevel Inverter (MI), the popular control technique is sinusoidal pulse width modulation (SPWM) method because it can be simply implemented for MI. The frequency modulation index m_f is the ratio of carrier signal frequency f_c and modulation signal frequency f_m [9] and it is expressed by

$$m_f = \frac{f_c}{f_m} \tag{1}$$

In this paper, the multicarrier PWM techniques are used for investigation THD in the 5-level FNPCMI composed of PD, POD, PODf, and APOD. Phase Disposition is shown in Fig. 3 where all carriers are in phase across all the bands. Phase Opposition Disposition is depicted in Fig. 4 where all the carriers above the zero reference point are in phase and the carriers below the zero reference point are phase shifted by 180°. Phase Opposition Disposition with different frequencies is shown in Fig. 5 where the phase of the carrier signals is same as POD but the carrier band for bottom and top is less than the intermediate band. Alternative Phase Opposition Disposition Disposition Disposition (APOD) is described in Fig. 6 where carriers in adjacent band are phase shifted by 180°.



frequencies



Fig. 6: Alternative Phase Opposition Disposition

IV.DSP BASED ON SPWM FOR 5-LEVEL FNPCMI

PWM signal for controlling the power electronic switches of FNPCMI, the modulation or reference signals is continuously compared with each of the carrier signal. Comparison results, the power electro-nic switch is closed when the reference signal is greater than the carrier signal, and the switch is opened when the reference signal is less than the carrier signal. The modulation technique [10] used in this paper is sinusoidal pulse width modulation technique. The method is to produce the gate signal by comparing a triangular carrier signal with two reference signals as shown in Fig7.



Fig. 7: Switching signal generation for 5-level multilevel inverter

The amplitude modulation index is given as

$$m_a = \frac{A_{ctrl}}{A_c} \tag{2}$$

where A_{ctrl} and A_{c} are the amplitude of the control signal and the carrier signals, respectively, and

$$\theta_{1} = \sin^{-1} \left(\frac{A_{C}}{A_{curl}} \right)$$
$$\theta_{2} = \pi - \theta_{1}$$
$$\theta_{3} = \pi + \theta_{1}$$
$$\theta_{4} = 2\pi - \theta_{1}.$$

Pulse width modulation period can be given as

$$T_{PWM} = \begin{cases} m_a T_c \sin \theta & : 0 < \theta < \theta_1, \theta_2 < \theta < \theta_3, \theta_2 < \theta < 2\pi \\ m_a T_c (2\sin \theta - 1) & : \theta_1 \le \theta \le \theta_2, \theta_3 \le \theta \le \theta_4 \end{cases}$$
(3)

where T_c is Time-Base Period Register (TBPR) of DSP controller.

Simulation results based on PSCAD program using model (3), Figs. 8-11 show the SPWM signal of PD, POD, PODf, and APOD, respectively, where the amplitude modulation index, reference frequency, and carrier frequency are 0.9, 50Hz, and 3.6kHz (PODf : 2.7kHz, 3.6kHz), respectively.



Fig. 8: PD-SPWM signal







Fig. 10: PODf-SPWM signal





 $s_1 - s_4$ and $s'_1 - s'_4$ in the 5-level FNPCMI based on the digital process. The input signals of the process digital are composed of the *SPWM*, D_0 , and D_{30} . The D_0 and D_{30} represent the digital reference signals in during $\theta_1 \le \theta \le \theta_2$ and $\theta_3 \le \theta \le \theta_4$, respectively.



Fig. 12: Digital circuit of $s_1 - s_4$ and $s'_1 - s'_4$



Fig. 13: Prototype of the switch controller of $s_1 - s_4$ and

$$s'_1 - s'_4$$



Fig. 14: Flow chart diagram for creating the PWM control signals with different modulation techniques

Fig. 13 shows the prototype of the switch controller of $s_1 - s_4$ and $s'_1 - s'_4$ used in the 5-level FNPCMI.

In this paper, a TMS320F28335 DSP is used as a processor. Fig. 14 shows the flowchart diagram for creating the PWM control signals of PD, POD, PODf, and APOD. And Figs. 15-18 show 4 types of the control signals of the $s_1 - s_4$ based on PD, POD, PODf, and APOD, respectively.



Fig. 15: Control signals of based on PD-SPWM



Fig. 16: Control signals of based on POD-SPWM



Fig. 17: Control signals of based on PODf-SPWM



Fig. 18: Control signals of based on APOD-SPWM

V. SIMULATION AND EXPERIMENTAL RESULTS

The prototype of the 5-level FNPCMI is shown in Fig 19. The IGBT CM75DU-12H is used as the controlled switches. The diode RURG8060 is used as the clamped diode. 48V DC voltage (12Vx4) is used as the DC link voltage of the inverter. A step-up transformer 30/220V is used to boost output voltage of 5-level FNPCMI to 220V. The load is composed $R = 50\Omega$ and L = 80mH. The configuration of the 5-level FNPCMI without the step-up transformer is shown in Fig 20.



Fig. 19: The prototype of 5-level FNPCMI



Fig. 20: Configuration of the 5-level FNPCMI without the step-up transformer



Fig. 21: Phase voltage and phase current with POD technique

The PD, POD, PODf, and APOD modulation techniques are used to control the 5-level FNPCMI for investigation of the THD. The phase voltage and phase current waveforms of the 5-level FNPCMI using POD modulation technique obtained the measurement are shown in Fig. 21. The phase voltage shape has 5-level, the rms phase voltage is 212V, the rms phase current is 3.87A, and the frequency of the system is 50.92Hz. Output power is 820.44W.





b: Digital process





In the paper, the configuration of the 5-level FNPCMI as shown in Fig. 20 is used to measure the THD of the system. Fig 22 shows the model of 5-level FNPCMI based on PSCAD which consists of the models of D_0 , D_{30} , and *SPWM*, digital process, and 2-phase 5-level FNPCMI.

Based on simulation and experiment, Figs 23-26 show the output waveforms and THD of the 5-level FNPCMI with $m_a = 0.9$ using SPWM technique of the PD, POD, PODf, and APOD, respectively.





a: Line to line of current and voltage obtained from the simulation (top) and the experiment (bottom)



b: THD of line to line voltage based on the simulation (top) and the experiment (bottom)



c: THD of line to line current based on the simulation (top) and the experiment (bottom)

Fig. 23. Output waveforms and THD of the 5-level FNPCMI using PD modulation technique





a: Line to line of current and voltage obtained from the simulation (top) and the experiment (bottom)



b: THD of line to line voltage based on the simulation (top) and the experiment (bottom)



c: THD of line to line current based on the simulation (top) and the experiment (bottom)

Fig. 24: Output waveforms and THD of the 5-level FNPCMI using POD modulation technique





a: Line to line of current and voltage obtained from the simulation (top) and the experiment (bottom)



b: THD of line to line voltage based on the simulation (top) and the experiment (bottom)



- c: THD of line to line current based on the simulation (top) and the experiment (bottom)
- Fig. 25: Output waveforms and THD of the 5-level FNPCMI using PODf modulation technique





A: Line To Line of Current and Voltage Obtained from The Simulation (Top) And The Experiment (Bottom)



B: THD of Line to Line Voltage Based on the Simulation (Top) and the Experiment (Bottom)





Fig. 26: Output waveforms and THD of the 5-level FNPCMI using APOD modulation technique

The PD, POD, PODf, and APOD modulation techniques used to control the 5-level FNPCMI by varying the amplitude modulation index in the range of 0.4 to 1. Experimental results, Fig. 27 shows the percentage of the total harmonic distortion with different amplitude modulation indices. The lowest percentage of the THD is produced when the multilevel inverter is controlled by the PD modulation technique. Fig. 28 shows the line to line voltage V_{AB} versus different amplitude modulation indices.



Fig. 27: % THD Versus Amplitude Modulation Index



Fig. 28: Line to Line Voltage Versus Amplitude Modulation Index

VI.CONCLUSIONS

This paper presents an investigation of the THD in 5-level full-bridge neutral point clamped multilevel inverter by using SPWM techniques of the PD, POD, PODf, and APOD. The control signals of the multilevel inverter based on the PSCAD program and TMS320F28335 DSP controller are presented. These signals are used to control the multilevel inverter for comparative the percentage of the THD by varying the amplitude modulation index in the range of 0.4 to 1. The prototype of the multilevel inverter with a resistive load 50 Ω and an inductive load 8 mH is used for experiment. Regarding to the results, the lowest percentage of the THD of the system is produced when the multilevel inverter is controlled by the PD modulation technique.

REFERENCES

- Y. Xiaoming, I. Barbi, "Fundamentals of a new diode clamping Multilevel Inverter", IEEE Transactions on Power Electronics, vol. 15, no. 4, pp. 711–718, July 2000.
- [2] J. Rodriguez, J.S. Lai, and F.Z. Peng, N. Janjamraj, "Multilevel inverters: a survey of topologies, controls, and applications", IEEE Transactions on Industrial Electronics, vol. 49, no. 4, pp. 724–738 August 2200.
- [3] A. Oonsivilai, "Review of Multilevel Converters/Inverters", International Review of Electrical Engineering (IREE), vol. 8 no. 2, pp. 514–527, April 2013.
- [4] S. Kjaer, J. Pedersen and F. Blaabjerg, "A Review of Single Phase Grid-Connected Inverters for Photovoltaic Modules," IEEE Trans. on Industry Applications, vol. 41, no.5, pp. 1292-1306, Sep 2005.

- [5] A. Radan, A.H. Shahirinia, and M. Falahi, "Evaluation of carrier-based PWM methods for multi-level inverters", The International Conference on Industrial Electronics, pp. 389-394, 2007.
- [6] R. Naderi and A. Rahmati, "Phase-Shifted Carrier PWM Technique for General Cascaded Inverters", IEEE Transactions on Power Electronics, vol. 23, no.3, pp. 1257-1269, May 2008.
- [7] J.J. Mane, S.P. Muley, and M.V. Aware, "Performance of 5level NPC inverter with multi-multicarrier multi-modulation technique", The International Conference on Power Electronics, Drives and Energy Systems, pp. 1-5, 2012.
- [8] C.R. Balamurugan, S.P. Natarajan, and R. Bensraj, "Performance evaluation of unipolar PWM strategies for three phase five level diode clamped inverter", The International Conference on Emerging Trends in Science, Engineering and Technology, pp. 443-449, 2012.
 [9] H. Zheng, B. Zhang, and L. Chen, "Carrier overlapping-
- [9] H. Zheng, B. Zhang, and L. Chen, "Carrier overlappingswitching frequency optional PWM method for cascaded multilevel inverter," International Conference on Electrical and Control Engineering, pp. 3450-3453, 2010.
- [10] N.A. Yusof, N.M. Sapari, H. Mokhlis, and J. Selvaraj, "A comparative study of 5-level and 7-level multilevel inverter connected to the grid", International Conference on Power and Energy, pp. 542-547, 2012.