Survey on Multilevel Inverter with Less Number of Switches for Different Loads

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Abstract

Multi-level inverter (MLI) is become more popular emerging in recent years and very efficient power electronic device suited for medium high power utilities and industrial drives. Multi-level inverters are power semiconductor sources which are connected properly and controlled to generate a multi-step voltage waveform with variable and controllable frequency, phase and amplitude. This study deals with performance of a 5 level, 7 level, 9 level and 13 level inverter model. The harmonic analysis is examined for different levels with the different palm techniques. The harmonic analysis introduced to study the reduced total harmonic distortion (THD) level and depends on the gating of signals for different units an MLI. The various implement/analyze PWM techniques with different levels of multi-level inverter decreases switching loss and improves the output power and efficiency. It has been found that with increasing levels of multi-level inverter with less number of switches satisfies the required limits of harmonics. PWM control techniques is applied to the power pleesonic switches at appropriate conducting angles with regular intervals of delays. A recent / present technique called SHE (selective harmonic elimination) is also studied in order to decrease specific harmonics.

Index terms - *Multi Level Inverter (MLI), Total Harmonics Distortion (THD), DSTATCOM, Reversing voltage, Solar Power Utilities, Selective Harmonics (SHE), Elimination, and PWM Methods.*

I. INTRODUCTION

A multi-level converter has more advantages compared to a conventional two- level converter.Switching frequencies: Multi level converters can work at both fundamental frequency and high frequency PWM. It should be identified/observed that lower switching frequency usually means lower switching loss and high efficiency. Stair case wave form quality: Multi level invertors not only generate common mode voltage, therefore the stress in a bearing of motor connected to a multi-level inverter can be reduced. Input current: Multi level converters can draw input current with low distortion. The series connection of two or more single phase H-bridge inverters formation is known as cascaded H-bridge multi-level inverter. Multi-level inverter has levels of 3, 5, 7, 9, 11, 13 etc.

(i). Topology of inverter: (b)

A 5-level inverter, represented in figure shown below. The circuit consists of a full bridge inverter, an auxiliary circuit and two capacitors as voltage divider.

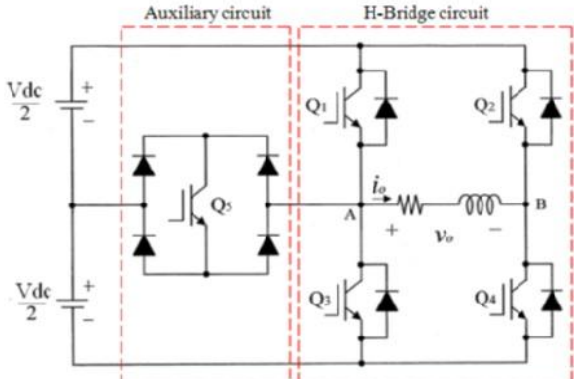

Fig 1. Topology of 5-level multilevel inverter

(ii). 7-level multi-level converter: (b)

The circuit representation of 7-level inverter is similar to 5-level circuit diagram, only the auxiliary circuit now was added with an additional circuit. 7-level inverter consists of a full bridge inverter, two bi directional switches and three capacitors as voltage divider.

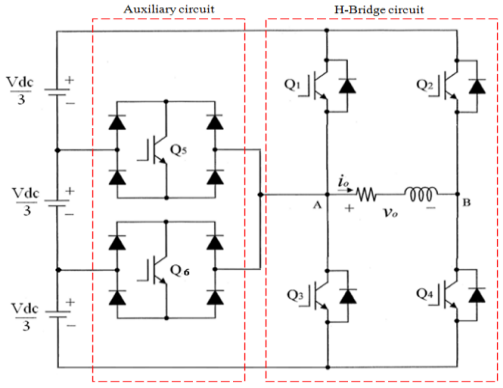

Fig 2: Topology of 7-level multilevel inverter.

9-Level inverter:

The circuit configuration of a general cascaded H-bridge nine level inverter is shown in fig 4. Each H-bridge module has an independent DC voltage source. Every output terminal of H-bridge cell is connected in series.

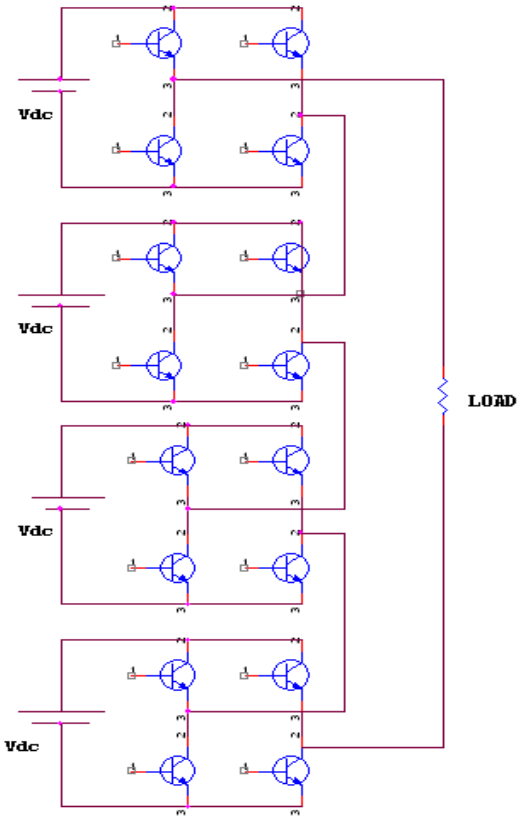

Fig 3. Block diagram of Cascaded Nine Level Inverter.

Basic definitions:

(THD) Total Harmonic distortion:

It is the measurement of harmonic distortion. It is defined as the ratio of the sum of the powers of all harmonic components to the power of fundamental frequency. As per IEEE standard of THD limits, total harmonic current distortion shall be less than 5% of the fundamental frequency current at rated inverter output.

POWER FACTOR:

Power factor is defined as the ratio between real power and apparent power in a circuit model.

$$\text{Power factor} = \frac{\text{Real power}}{\text{Apparent power}} = \frac{P}{S}$$

The bad with high power factor will draw less current, hence decrease the lost in distribution system therefore wastage of energy will be less. The unity power factor is the best.

EFFICIENCY:

In general, efficiency is measurable concept, quantitatively determine by the ration between output and input.

$$\text{Efficiency} = \frac{\text{Output}}{\text{Input}}$$

Pulse width modulation techniques:

- *Phase Disposition(PD) Technique:*
  The disposition technique as one of the carrier based PWM method is based on the comparison of sinusoidal reference waveform with carrier signals in phase with each other.

- *Phase Opposition Disposition (POD) Technique:*
  In the POD-PWM method the carrier signals above the zero axes are in phase. The carrier signals below zero are also in phase, but 180 phase shifted to the above carrier signals.

- *Alternate Phase Oppose Disposition (APOD) Technique:*
  In case of APOD modulation, every carrier waveform is out of phase with its neighboring carrier waveform by 180 degrees.

II. LITERATURE SURVEY

A. Modeling and simulation of 13-level cascaded hybrid multilevel inverter with less number of switches

In recent years, the multi-level inverter plays an important role for medium power applications. It is simple in construction and produces small amount of harmonics. And also it has less switching losses, Switching stresses and high dv/dt rating.

- The three commercial topologies of multi-level inverters are:
- Neutral point clamped (NPC), diode clamped multi-level inverter (DCMLI)
- Flying capacitor multi-level inverter (FCMLI)
- Cascaded H bridge (CHB) multi-level inverter.

Compared to DCMLI and FCMLI the CMLI doesn't require voltage balancing capacitor and voltage clamping diodes. This literature review paper studied particularly on cascaded multi-level inverter which require independent DC source. For 'n' number DC sources the (2n+1) number of levels will be generated. The CHB multi-level inverter is further divided into two configurations namely Symmetric and Asymmetric inverters. In symmetric configuration all the voltage source valves are equal. In symmetric configuration the number of output voltage levels increased then it results in increase in number of switching devices.Therefore to

increase the output voltage levels with less number of switches, the different value of DC source voltages are selected it is known as asymmetric configuration.So in this review paper asymmetric configuration with three different voltage sources are selected to generate the levels. The specified harmonics are distorted using SHE-PWM method.The CMLI requires 'n' DC sources to generate (2n+1) levels, But it is problem to use separate DC sources for many applications.

Fig 4 represents CMLI having two H-bridges each H-bridge is consists of separate values of DC source as V'dc for bridge 1 and V'dc/2 for bridge 2. The output of bridge 1 denoted by V1(t) and another one represented as Vc(t).

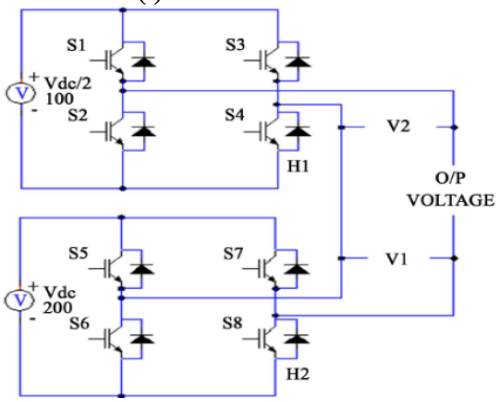

Fig 4. CMLI with unequal dc sources

The output phase voltage is obtained by

$$Vo = V1(t) + V2(t)$$

SHE method is used in medium and high power applications where switching frequency is low enough to minimize the switching losses. The performance of this method is totally depends upon switching angles. The main objective of SHE is to obtain lower order harmonics at the output side. The asymmetric inverter is shown in **fig 5.** The switching stages and voltage levels shown in **Table 1**.

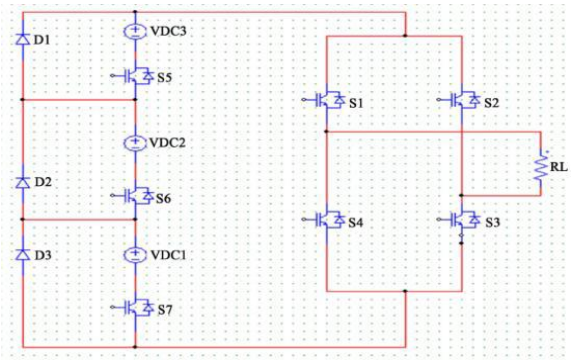

Fig 5: Proposed circuit for Cascaded 13-level Inverter-Asymmetric Topology.

Switching states							Output voltage
S1	S2	S3	S4	S5	S6	S7	vd
1	0	1	0	0	0	1	+vd
1	0	1	0	0	1	1	+vd/6
1	0	1	0	0	1	1	+vd/3
1	0	1	0	1	0	0	+3vd/6
1	0	1	0	1	0	1	+2vd/3
1	0	1	0	1	1	1	+4vd/5
0	0	0	0	0	0	0	0
0	1	0	1	0	0	1	-vd
0	1	0	1	0	1	1	-vd/6
0	1	0	1	0	1	1	-vd/3
0	1	0	1	1	0	0	-3vd/6
0	1	0	1	1	0	1	-2vd/3
0	1	0	1	1	1	1	-4vd/5

Table 1: Switching states and voltage levels of 13-level inverter

- Here 3 DC sources are connected with seven switches. Three flywheel diodes are used to prevent the back emf from triggering.
- To generate a 13 level output, the proposed modulation method carries six carrier signals with one modulating signal. The carrier waveform of proposed method is shown in Fig 6.

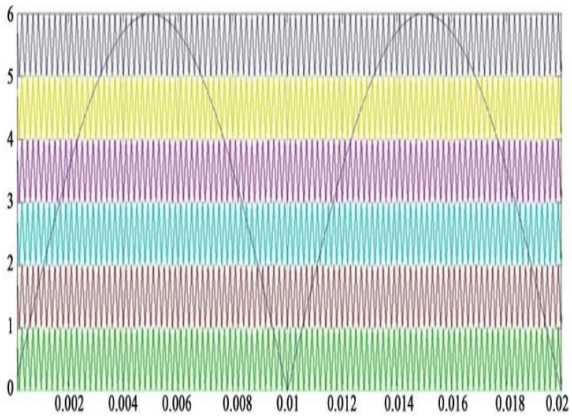

Fig 6: Carrier waveform for SPWM technique.

B. Analysis of reduced switch topology multilevel inverter

The reduced switch count multilevel inverter diagram o, includes of a conventional H bridge with bidirectional switches in it to get required voltage level with a single dc source and with voltage dividing capacitors.

The 11-level RSCMLI single phase design configuration shown in fig.7

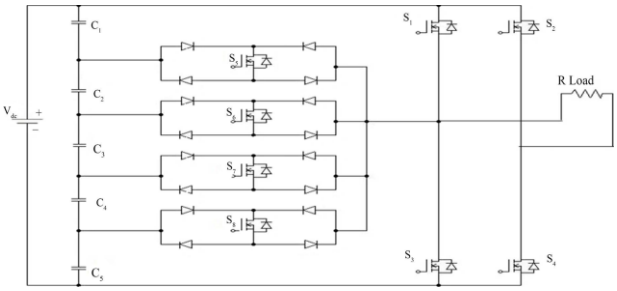

Fig 7: Single phase structure of eleven level Reduced Switch Count Multilevel (RSCMLI) Inverter.

The RSCMLI design for N-levels it requires [(N-1)/2+3] switches.

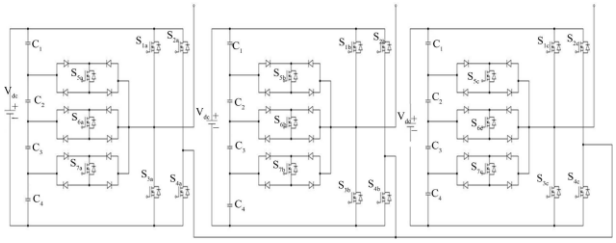

Fig 8: Three phase structure of nine level RSCMLI inverter.

For five level inverter it has single H-Bridge with a bidirectional switch and require three voltage dividing capacitors with single de source.The required switches for four level will be five switches for such level it requires seven switches and for eleven it requires eight switches.Therefore compared to cascaded bridge MLI the number of switches required will be less for RSCMLI. For example for a 1-Eleven inverter of CHBMLI requires twenty switches with five separate dc sources and for 11-level RSCMLI design requires eight switches with single dc source and with five voltage dividing capacitors.

PWM method is the important part in the multilevel inviter to trigger the switches at the regular instant to get required level of output voltage. In this review paper following PWM techniques are implemented to get the required level of output voltage and harmonic analysis.

1. Multi carrier alternate phase opposition disposition9APOD) PWM method.

2. Multi carrier in phase disposition (IPD) PWM method.

3. Multi reference pulse width modulation.

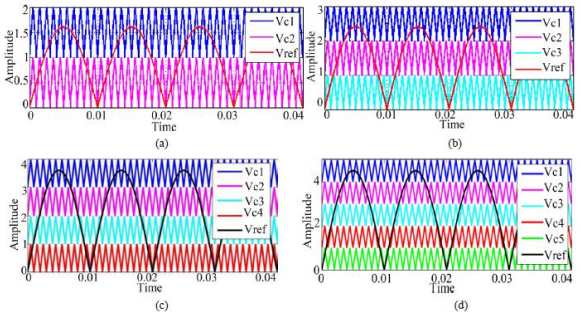

Fig 9: Three phase structure of nine level RSCMLI.

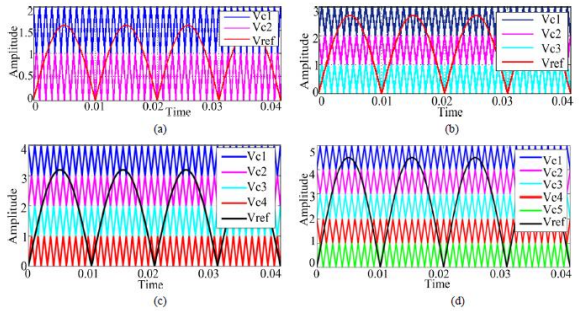

Fig 10: Carrier Alignment of IPD PWM method for RSCMLI inverter of (a) Five Level; (b) Seven Level; (c) Nine Level; (d) Eleven Level.

The nine level of reduced switch count multilevel invert is used for the application of DSTATCOM in the VSI.For power factor improvement to improve PF and harmonic level,DSTATCOM is connected to system at PCC point through coupling transform.

C. Performance comparison of seven level inverter and nine level inverter with minimum devices

This review paper describes the reversing voltage strategy for a multi-level inverter to enhance the power quality of induction motor by reducing the THD with required number of switches.The reversing voltage multilevel inverter consists of two parts, namely level generation group and polarity generation group. This concept divides output voltage into level generation and polarity generation devices.In this method, the polarity generation group requires low frequency switches and the level generation group needs high frequency switches at line frequency.The main objective of this method is to utilize both high frequency switches and low frequency switches.The main advantage are lags stress on the switches, greater efficiency and decreased total harmonic distortion (THD).This review paper describes a seven level & a level inverter using reverse voltage strategy.Seven level reversing voltage MLI: a seven level inverter requires the reversing voltage multi-level inverter for three phase phased connected to R-L load shown in below fig 11

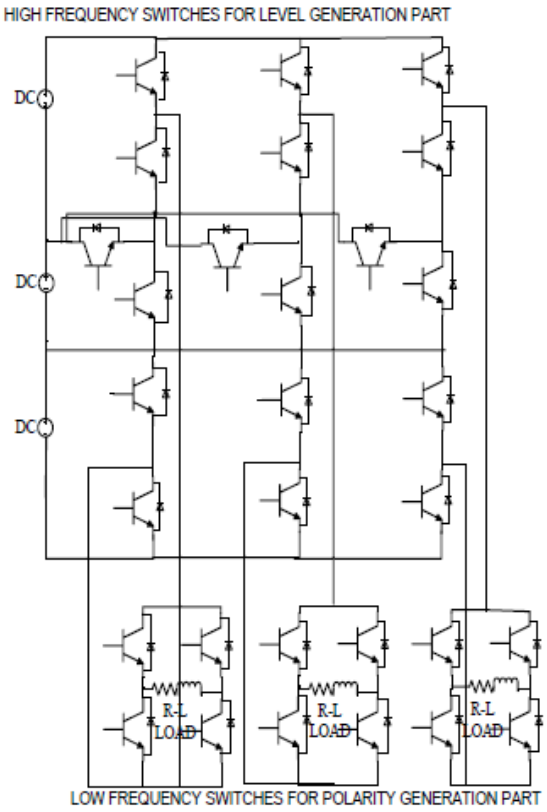

Fig 11:Reversing voltage multilevel inverter for three phases connected to the R-L load.

DC Voltage Level	Mode-1 operation	Mode-2 operation
0	2,3,4	
1	2,3,5	2,4,6
2	1,4	2,6,5
3	1,5	

Table2: Switching function for voltage output seven level generation

The different voltage levels are obtained by following operating modes.

- When switches 2.3.4 is on, output waveform produces a voltage level or DC.
- WhenNine level reversing multi-level inverter:

A nine level inverter needs 12 switches and 4 dc source. The circuit diagram of 3-phase reversing voltage multi-level inverter with R-L load shown in fig—

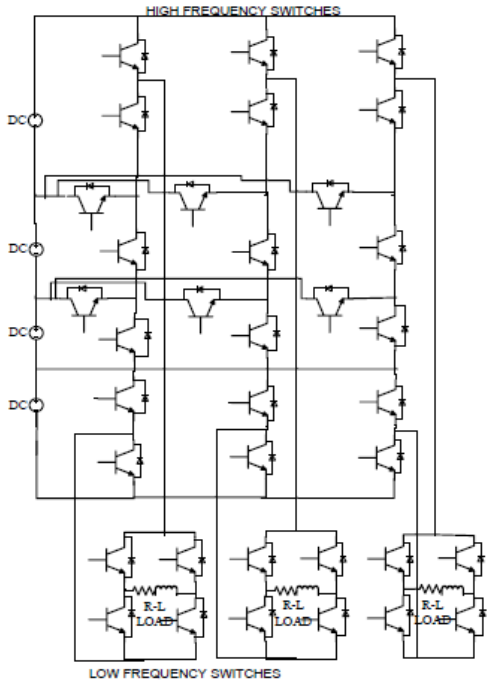

Fig 12: Reversing voltage multilevel inverter for three phases connected to the R-L load.

Switching modes of voltage output 9-level generation.

DC Voltage Level	Mode-1 operation	Mode-2 operation
0	2,3,4,5	
1	2,3,4,6	
2	2,3,6,8	2,7,5
3	1,5	2,7,6
4	1,6	

Table3: Switching function for voltage output 9- level generation

Operation:

The switching modes to obtain different voltage levels are:

The advantage of SPWM methods are:

- Less harmonic content
- Lower switching loses
- Simple methodology in implementation.

In this review paper to obtain the required controllable gate pulses, phase disposition method is used.

The frequency modulation index

MF=FC/FM

The reverse voltage multi-level inverter with 7 level for different loads like R, RL&induction motor voltage,current,frequency & speed output waveform are shown in below fig.

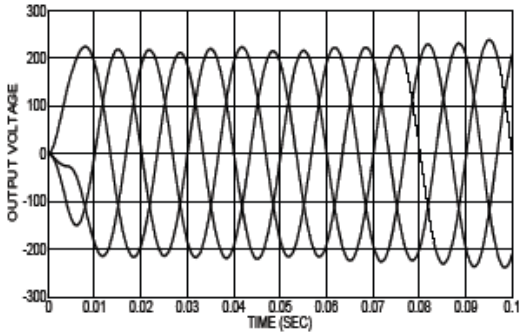

Fig 13: (a) Voltage Output waveform for 7-Level R-L load and for induction motor

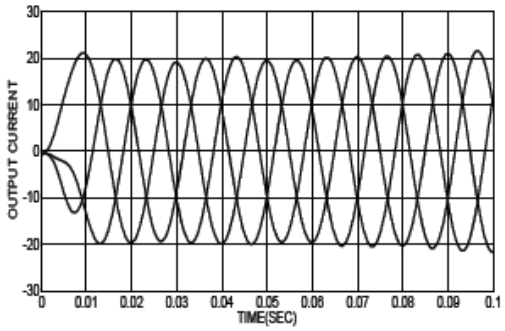

Fig 14: (b) Current output waveforms for 7-Level R-L load and for induction motor.

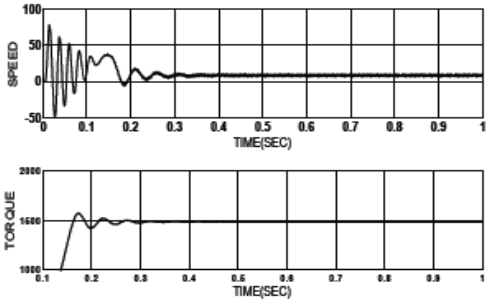

Fig 15: Torque and Speed structures waveform.

It may be observed that from a level RVMLI is greater reduction in THB values when compared to seven level reversing voltage inverter.

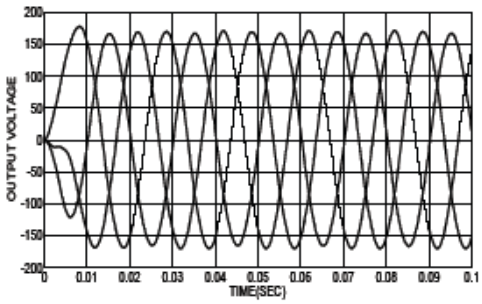

Fig 16: (a) Voltage Output waveform for 9-Level R-L load and for induction motor

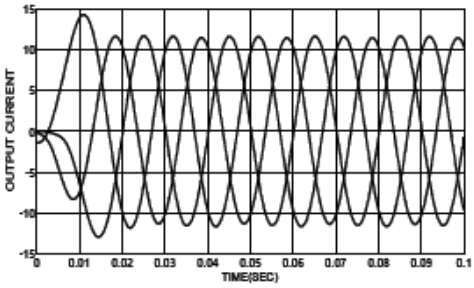

Fig 17: (b) Current output waveforms for 9-Level R-L load and for induction motor

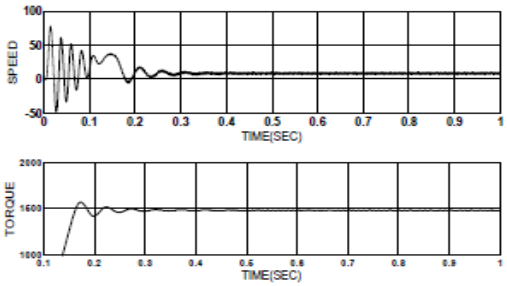

Fig 18: Torque and Speed structures waveform

RVMLI	OUTPUT VOLTAGE(V)	THD(%)	OUTPUT CURRENT(I)	THD(%)
7-Level	298	18.10	28.81	2.00
After Filter 7-Level	286.1	2.00	28.62	2.00
9-Level	391.3	16.30	36.02	1.64
After Filter 9-Level	361.2	1.64	36.02	1.64

Table4: Voltage Output and current output THD for R-Load before and after a filter.

RVMLI	OUTPUT	THD(	OUTPUT	THD(

	VOLTAGE (V)	%)	CURRENT(I)	%)
7-Level	298	18.09	23.48	0.67
After Filter 7-Level	274.5	13.80	23.24	0.67
9-Level	391.5	16.17	30.97	0.77
After Filter 9-Level	340.4	11.17	30.8	0.77

Table5: Voltage Output and current output THD for Induction motor before and after a filter.

D. Analysis of asymmetrical cascaded 7-level and 9-level multilevel inverter design for asynchronous motor

In this review paper asymmetrical cascaded multi-level inverter with 7 and 9 level using multi carrier based level shifted pulse width modulation method is used as load of induction motor. The asymmetrical multi-level inverter increases the number of level in the output and decreases the number of input DC voltage sources. IGBT used as semiconductor switch for implementing the inverter mode. It has high power rating, low switching losses and less conduction loss. Asymmetrical DC source has unequal magnitude of voltage conversely. Symmetrical DC source has equal magnitude of voltage.

In 7 level multi-level inverter two unequal DC source and 8 switches are used. In case of 9 level multi-level inverter 3 unequal DC sources and 12 switches are used. The basic representation of asymmetrical cascaded MLI with 7 level and 9 level shown in below Fig 18 and Fig 19 respectively.

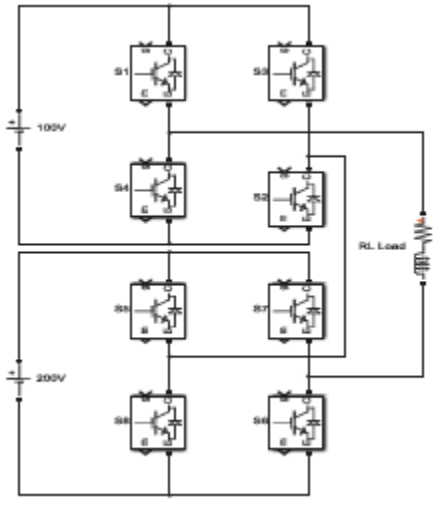

Fig 18: Asymmetrical 7 level inverter

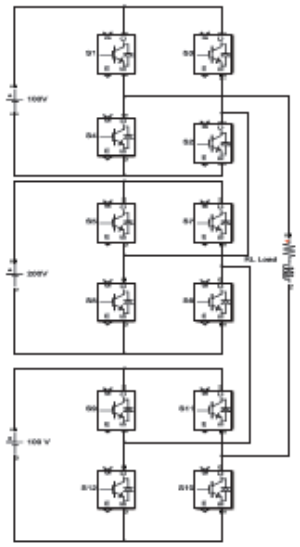

Fig 19: Asymmetrical 9 level inverter

Operation of cascaded 9 level topology:

The asymmetrical cascaded 9 level multi-level inverter consists of three DC sources and 12 switches. The three sources are connected to form Three H Bridge units which are cascaded in single phase. The individual H Bridge the output voltages are +Vdc or –Vdc. Therefore the required output voltage for 9 level asymmetric cascaded multi-level inverter are +4 Vdc, +3 Vdc, +2 Vdc, +Vdc, 0 , -Vdc, -2 Vdc, -3 Vdc and -4 Vdc. Switching pattern and voltage levels described by below Table 2.

OUTPUT	4V	3V	2V	V	0	-V	-2V	-3V	-4V
S1	1	1	0	1	0	0	0	0	0
S2	1	1	1	1	0	0	1	0	0
S3	0	0	0	0	0	1	0	1	1
S4	0	0	1	0	0	1	1	1	1
S5	1	1	1	0	0	0	0	0	0
S6	1	1	1	1	0	1	0	0	0
S7	0	0	0	0	0	0	1	1	1
S8	0	0	0	1	0	1	1	1	1
S9	1	0	0	0	0	0	0	0	0
S10	1	1	1	1	0	1	1	1	0
S11	0	0	0	0	0	0	0	0	1
S12	0	1	1	1	0	1	1	1	1

Table 6: Switching pattern for asymmetrical cascaded 9 level inverter.

The output voltage and current waveforms of seven level and nine level with capacitor start induction motor is shown in below Fig 20 and Fig 21 respectively.

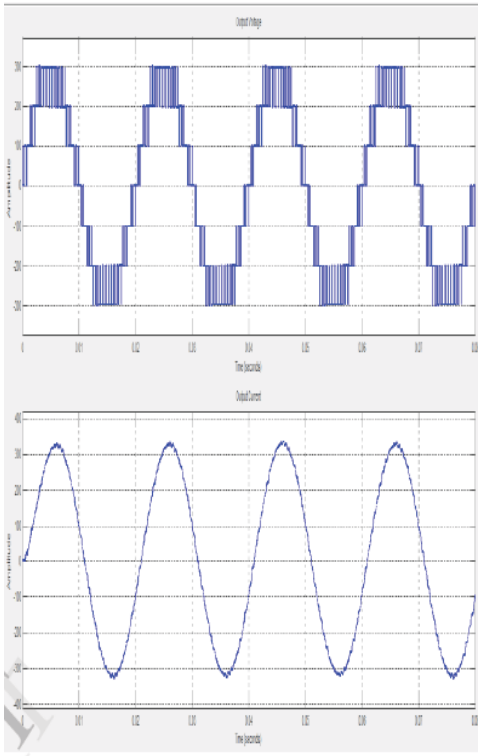

Fig 20: Output voltage and phase current of symmetrical 7 level multi-level inverter

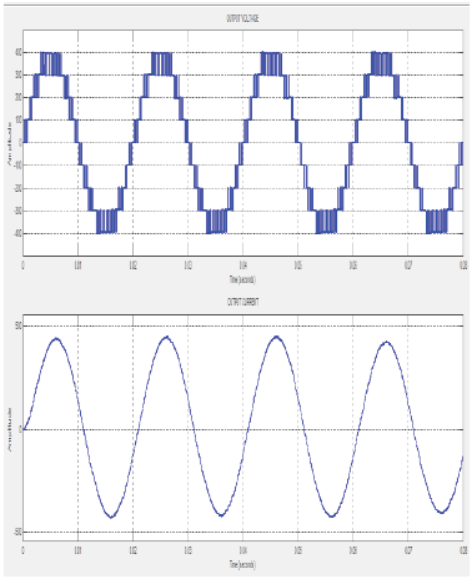

Fig 21: Output voltage and phase current of asymmetrical 9 level multilevel inverter

The performance characteristics of single phase induction motor and asymmetric inverter are studied. The steady state and variation of motor parameter with required levels formed in below Table 2 and Table 3 respectively.

MLI	Main winding current	Rotor speed	Electromagnetic Torque	THD(%)
7 Level	0.18 sec	0.2 sec	0.18 sec	4.65
9 Level	0.13 sec	0.15 sec	0.13 sec	1.18

Table 7: Steady state value for induction motor

MLI	Main winding current(AMP)	Rotor speed(rad/sec)	Electromagnetic Torque(Nm)
7 Level	+7 to -7	158	+5 to -3
9 Level	+8 to -8	158	+7 to -7

Table 8: Variation of induction motor parameters

Therefore the 9 level asymmetric cascaded multi-level inverter gives approximate sinusoidal output voltage with decreased total harmonic distortion and required motor output.

E. Design of 7 & 9 level inverter & dc-dc converter with less switches for solar power utilities

In the review paper 7 level and 9 level multi-level inverter and DC-DC converter for solar utilities is studied. The circuit diagram configuration of designed circuit of 7 level inverter with DC-DC power converter shown in below fig 22.

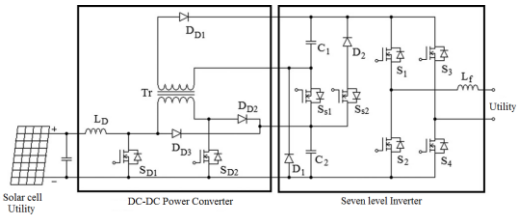

Fig 22: Proposed System

The solar cell is converted to convert output power into two voltage sources which are supplied to the inverter and the converter is a boost converter with transformer consists of 2:1 turn's ratio. The seven level inverter includes capacitor and full bridge converter. The capacitor selective circuit gives output of three level DC output and further the full bridge converter converts this three level output to seven level AC output. The fig 13 contains a DC-DC power converter combine's converter and current fed converter. The boost converter and current fed converter includes diode, inductor and a switch which charges the capacitor C2 and C1.

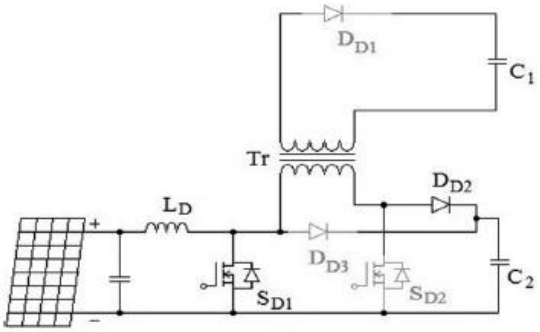

Fig 23: When the Switch (SD1 is ON)

The fig 23 contains operating circuit of converter when Sd1 off and Sd2 on, the capacitor C1 is connected to the capacitor C2 in parallel with transformer.The energy of the inductor and capacitor through diode Dd3 and charge capacitor C1 through transformer, diode Dd1 during the off state of switch Sd1.The boost converter is operated in the continuous conduction made.

The voltage in capacitor C2 is:

$$Vc2 = \frac{Vs}{1-D}$$

The voltage in capacitor C1 is:

$$Vc1 = \frac{Vs}{2(1-D)}$$

The operation is divided into positive cycle and negative cycle.

The operation of multi (seven) level inverter in the positive half cycle further divided into four modes as shown in fig 24.

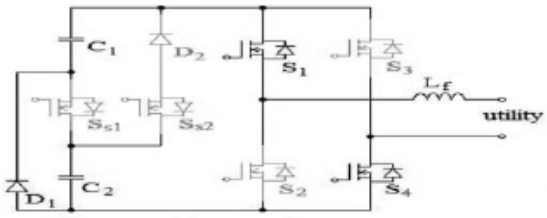

Fig 24: In Positive half cycle (Mode 1)

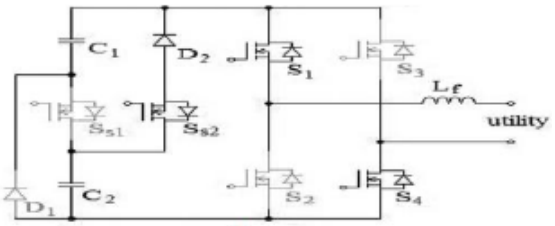

Fig 25: In Positive half cycle (Mode 2)

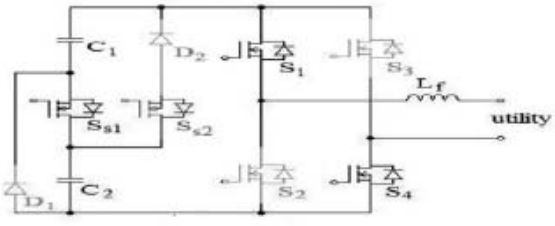

Fig 26: In positive half cycle (Mode 3)

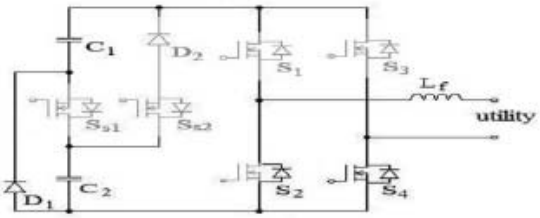

Fig 27: In positive half cycle (Mode 4)

The fig 26 and fig 27 shows the output voltage of 7 level inverter and 9 level multi inverter

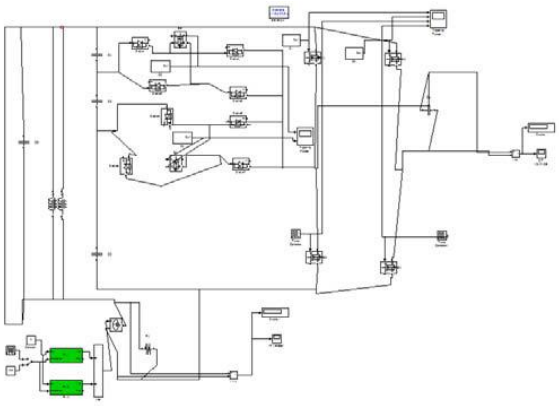

Fig 28: Output voltage of seven level multi inverter

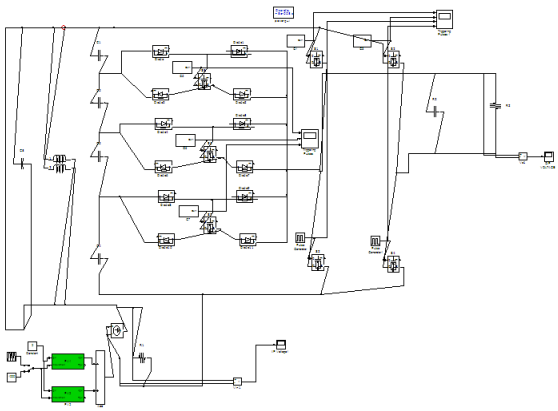

Fig 29: Output voltage of nine level multi-level inverter

Comparison of THD in multi-level inverter:

PHASE	LEVEL	THD (%)
Single	Single	18.79%
Single	Seven	18.79%
Single	Nine	10.80%

Table9:Comaprison of THD in MLI

Here the proposed inverter has minimum number automatic voltage balancing capacitors.

III. CONCLUSION

This survey has discussed about different levels of multi-level inverters for different applications. The SHE method has developed to reduce the specific harmonic for multi-level inverter. The odd number of conducting angles are (choose/V2) for decreasing the order harmonics. Initially, the higher power takes with improved power quality have been the important major market drive and trigger study for development of multi-level converters.The reversing voltage method enhances the output voltage, decrease the utilization of number of semiconductor switches and compensating the hazards. The cast and Centro/system are more reliable. The complexity of PNM techniques is low because of it need to generate the required gate pulses.The use of multi-level inverter in industrial drives and power applications accepted, because it gave more number of advantages. With more number of levels of multi-level inverter will give better performance in terms of power factor, THD and efficiency. Multi-level converter can achieve an effective increase in overall switch frequency with the elimination of lowest order switching frequency parts.

REFERENCES

[1] Modeling and Simulation of 13-level Cascaded Hybrid Multilevel Inverter with less number of Switches- G.Vidhya Krishnan1, M.Valan Rajkumar2, C.Hemalatha3 1, 2, 3Department of Electrical and Electronics Engineering, Gnanamani College of Technology, Namakkal-637018, Tamilnadu, India

[2] Analysis of Reduced Switch Topology Multilevel Inverter with Different Pulse Width Modulation Technique and Its Application with DSTATCOM-Sambasivam Rajalakshmi*, Parthasarathy Rangarajan Department of Electrical and Electronics Engineering, R.M.D. Engineering College, Anna University, Chennai, India

[3] Three Phase 7-Level and 9-Level Reversing Voltage Multilevel Inverter- G. Vijaykrishna* and O. Chandra Shekhar KL University - 522502, Guntur, Andhra Pradesh, India

[4] Analysis of Asymmetrical Cascaded 7 Level and 9 Level Multilevel Inverter Design for Asynchronous Motor- Nayna Bhargava- Dept. of Electrical Engineering, SATI, Vidisha, Madhya Pradesh, India.

[5] Design Of 7 & 9 Level Inverter & DC-DC Converter With Less Switches for Solar Power Utilities- P.Sathyanathan, Dr. P.Usha Rani#2, Electrical and Electronics Engineering#1, Electrical and Electronics Engineering#2 Vel Tech, Avadi, Chenai-62#1. R.M.D. Engineering College, Kavarapettei, Chenai- 601 206#2.

[6] Rodriguez, J., Lai, J.-S. And Peng, F.Z. (2002) Multilevel Inverters: A Survey of Topologies, Controls, and Applications. IEEE Transactions on Industrial Electronics, 49, 724-738.

[7] Malinowski, M., Gopakumar, K., Rodriguez, J. and Perez, M.A. (2010) A Survey on Cascaded Multilevel Inverters. IEEE Transactions on Industrial Electronics, 57, 2197-2206.

[8] M.Valan Rajkumar, P.S.Manoharan, Modeling and Simulation of Three-phase DCMLI using SVPWM for Photovoltaic System, Springer Lecture Notes in Electrical Engineering, under the volume titled “Power Electronics & Renewable Energy Systems", Vol-326, Chapter No.5January 2015, Pages 39-45.