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Power System Faults Mitigation using Generalised Unified Power Quality Conditioner

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ABSTRACT:

In power system, faults are considered to be abnormal electric current parameter. Numbers of factors are responsible for the fault occurrence in a distribution system. Thus, Power electronics and advanced control technologies can be used to addresses the power system faults in order to detect and interrupt different types of faults in power system. Major problems dealt in this paper are the current harmonics caused by non-linear loads and voltage quality is another aspect that will cause several sensitive electronic equipments malfunctioning. Distribution static compensator (DSTATCOM) is used to compensate current harmonics, connected in series with the network. In order to improve voltage quality, Dynamic Voltage Restorer (DVR) is a solution, is connected in series with the network. The combination of a DSTATCOM and two DVR one can obtain Generalised Unified Power Quality Conditioner (GUPQC). This paper presents modelling, analysis and simulation GUPQC with three bus/feeder system with nonlinear and sensitive loads. Simulation results of GUPQC under different fault conditions are discussed in this paper. The simulation results of the GUQPC to compensate current harmonics and voltage quality improvement show clearly its performance.

KEYWORDS: *Unit vector template (UVT), Generalised unified power quality conditioner (GUPQC), Distribution static compensator (DSTATCOM) and Dynamic voltage restorer (DVR).*

I. INTRODUCTION

During operation, in power system electrical apparatus, grids and machineries and equipments are often subjected to different faults. Once a fault occurs, the typical values (such as impedance) of the machineries may change from current values to different values until the fault is cleared. The faults may happen due to lighting, equipment failure, wind, tree dropping on lines. Abnormality of the system occurs due to fault in electrical power grid, due to that failure of electrical equipments, such as transformers, generators, busbars, etc. Due to faults, equipments insulation failures and short circuiting of conductors due to conducting path failures. Some customers demand an honest quality of power above the standard offered by existing electricity networks, which is why an enormous made to satisfy the needs of customers. Flexible AC transmission (FACTS) instruments such as static synchronous series compensator (SSSC), static synchronous compensator (STATCOM), interline power flow controller (IPFC), unified power flow controller (UPFC) etc. have been used to provide clean and pure power. FACTS systems are typically equipped for transmitting and these machineries are adapted to be employed and called as Custom Power Devices in the distribution system.

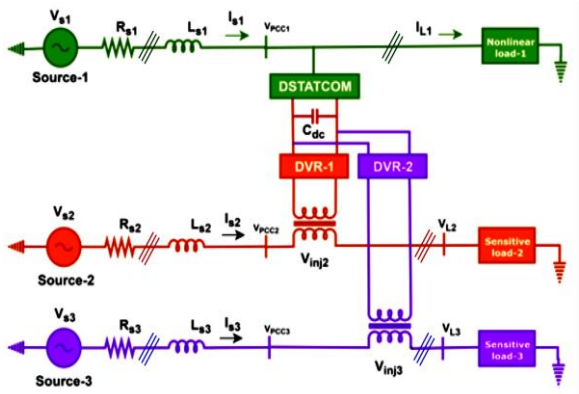

Figure-1: Generalised Unified Power Quality Conditioner

II. CONTROL STRATEGY OF DVR

The Unit vector theory is used to control strategy is used for the DVR. The definition of the unit vector template suggested in [4] is used to extract the UVT from distorted supply. Fig.2 shows the UVT control strategy. DVR injects opposite to the unbalance and / or distortion present within the Supply voltage in order to keep this out & these voltages cancel each other, due this cause a balanced voltage with magnitude as required by the load-side voltage [6].

UVT control strategy shown in Fig.2, compares the load voltage signals with load side reference voltage, resulted obtained from this, and is therefore given to hysteresis controller to produce series inverter gating signal. Hysteresis controllers have been used as mentioned in [5].

Switching pattern within the inverter is determined by the hysteresis band regulations. Hysteresis controller function depends on the error signal produced during the load side reference voltage comparison and thus the instantaneous voltage signals of the load side.

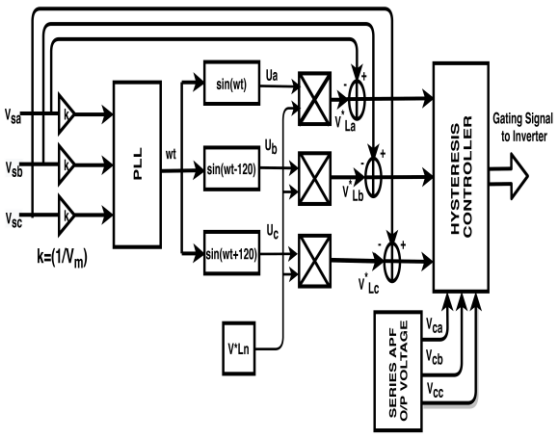

Figure-2: UVT Control Strategy of DVR

III. CONTROL STRATEGY OF DSTATCOM

Fig. 3 describes the control strategy of the shunt APF. According to P-Q theory, the 3-Φ voltages and currents are determined instantaneously and translated to α-β-0 co-ordinates [3] by using the equations (1) and (2).

$$\begin{bmatrix} V_{in\_0} \\ V_{in\_\alpha} \\ V_{in\_\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{in\_a} \\ V_{in\_b} \\ V_{in\_c} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} i_{in\_0} \\ i_{in\_\alpha} \\ i_{in\_\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{in\_a} \\ i_{in\_b} \\ i_{in\_c} \end{bmatrix} \quad (2)$$

Equation (3), gives the load drawn true power (Ps), reactive power and the zero sequence components. Instantaneously true & reactive powers are measured. Equation (4), gives existence of instantaneous power in terms of average and oscillating components.

$$\begin{bmatrix} P_0 \\ P_s \\ q_s \end{bmatrix} = \begin{bmatrix} V_{in\_0} & 0 & 0 \\ 0 & V_{in\_\alpha} & V_{in\_\beta} \\ 0 & -V_{in\_\beta} & V_{in\_\alpha} \end{bmatrix} \begin{bmatrix} i_0 \\ i_{in\_\alpha} \\ i_{in\_\beta} \end{bmatrix} \quad (3)$$

$$p_s = \overline{p_s} + \widetilde{p_s}\ ;\ q_s = \overline{q_s} + \widetilde{q_s} \quad (4)$$

Where $\overline{p_s}$ direct true power component; $\widetilde{p_s}$ fluctuating true power component; $\overline{q_s}$ direct reactive power component; $\widetilde{q_s}$ fluctuating reactive power component. To compensate the harmonic and reactive power, net reactive power and fluctuating portion of real power are used to generate the power and current reference signals as per the equation (5). As the load is assumed to be balanced, P_0 will be no zero.

$$\begin{bmatrix} i^*_{Co\alpha} \\ i^*_{Co\beta} \end{bmatrix} = \frac{1}{V^2_{in\_\alpha}+V^2_{in\_\beta}} \begin{bmatrix} V_{in\_\alpha} & -V_{in\_\beta} \\ V_{in\_\beta} & V_{in\_\alpha} \end{bmatrix} \begin{bmatrix} -\widetilde{P}_s + \overline{P}_{loss} \\ -q_s \end{bmatrix} \quad (5)$$

The $\overline{P}_{loss}$, signal is got from the voltage regulator and is used as the actual power average. It can also be defined as the active instant power corresponding to the UPQC's resistive loss and switching loss [6 & 7]. The error obtained when comparing the true DC-link capacitor voltage with the reference value is processed by the voltage control loop in the proportional-integral controller (PI), as it minimises the steady state error of the voltage through the DC connection.

Equation (5) shows the compensating currents ($i^*_{Co\alpha}$, $i^*_{Co\beta}$) needed as per the load power demand. In α-β coordinates, these currents are represented. Equation (6) is used to obtain the phase current needed for compensation (i^*_{Coa}, i^*_{Cob}, i^*_{Coc}). The compensating currents in a-b-c axis are got from α-β coordinates, reflects these phase currents.

$$\begin{bmatrix} i^*_{Coa} \\ i^*_{Cob} \\ i^*_{Coc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i^*_{Co\alpha} \\ i^*_{Co\beta} \end{bmatrix} \quad (6)$$

P-Q theory based control strategy used for shunt compensator is valid for non-ideal mains voltage of 3-phase systems. Under non-ideal voltage conditions, $V^2_{in\_\alpha} + V^2_{in\_\beta}$ is inconsistent and in the instantaneous true and reactive powers, current and voltage harmonics will be added. As a consequence, the shunt APF will not produce a compensation current which are equal to the current harmonics [6].

Instantaneous reactive and active powers have to be measured after filtering of mains voltages to address these limitations. As shown in Fig.4, the Voltage harmonic filters is used. Equation (7), shows the instantaneous voltage transformation into d-q co-ordinates using park transformation.

$$\begin{bmatrix} V_{in\_d} \\ V_{in\_q} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \sin(\omega t) & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} V_{in\_a} \\ V_{in\_b} \\ V_{in\_c} \end{bmatrix} \quad (7)$$

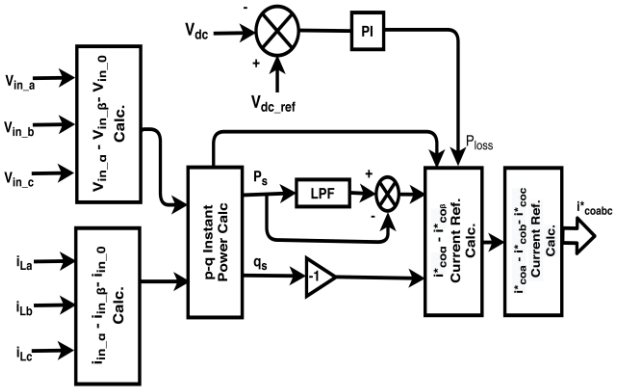

Figure-3: P-Q Control strategy of DSTATCOM

The low pass filter with 5th order having 50 Hz cut-off frequency filters influences of d-q voltages. The α-β coordinates are obtained from filtered components, as shown in equation (8). In d-q coordinates Low pass filter is used to convert the dissimilar supply voltages to sinusoidal shape.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \sin(\omega t) & \cos(\omega t) \\ -\cos(\omega t) & \sin(\omega t) \end{bmatrix}\begin{bmatrix} V_{in\_d} \\ V_{in\_q} \end{bmatrix} \qquad (8)$$

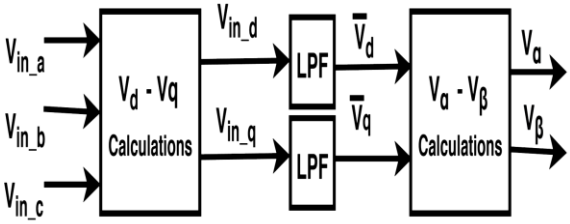

Figure- 4: d-q to α-β Coordinates conversion

The reference currents are generated by control algorithm, in order to provide the switching signals in the inverter. The hysteresis controller creates the switching pattern of the VSI by PWM by comparing instantaneous line currents with reference currents. The basis for the current hysteresis controller is the Error signals of the injected current and the shunt APF reference current.

IV. SIMULATION RESULTS

As seen in Figure-5, the above proposed control schemes are built in the MATLAB / SIMULINK environment. A 3-Φ diode bridge with RL load on the dc side is used for the application of nonlinear load. The findings of the simulation showed compensation for three-phase faults.

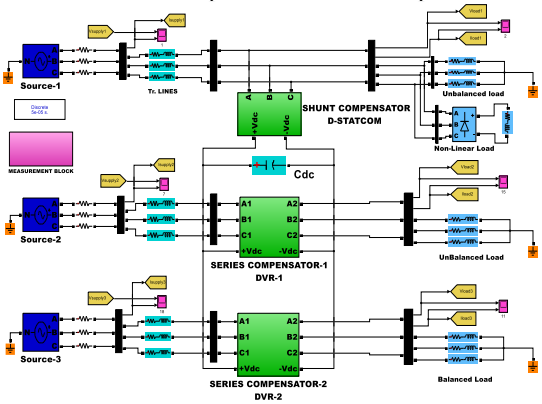

Figure-5: Simulink Model of GUPQC

Series Compensator with UVT Control Strategy Delivery of voltage within defined limits is generally expected by DS consumers, as the performance and operational characteristics of most consumer devices vary due to the deviation of the distribution supply voltages from the prescribed RMS values. The most critical PQ issues encountered by electrical DS utilities are either the voltage sags or the total failure of the supply system. Normally, the fault in the DSs triggered voltage sag or interruption of the supply system. In three-phase four-wire DS, there are five major fault types listed below [7-11]. 1. Single line-to-ground fault (LG) 2. Double line-to-ground fault (DLG) 3. Double-line fault (DLF) 4. Three line-to-ground fault (3LG) 5. Three-line fault (3LF).

In this section, the simulation studies for the compensation of voltage sag / swell and all of the above mentioned DS faults on the proposed GUPQC under the sinusoidal supply voltage conditions of bus-2 and bus-3 are discussed.

Case-1: LG fault at bus-1and DLG fault at bus-3

LG and DLG faults responsible for 80 % of overall distribution line faults [7,8]. The response of the proposed GUPQC to these two types of distribution line faults was carried out in this case study by applying a LG fault on bus-2 and a DLG fault on bus-3 during time intervals from t=0.05 sec to t=0.15 sec as seen in Figs. 6.1 (a) to (c) and Fig. 6.2 (a) to (c) respectively. Due to the fault in bus-2, the phase "a" voltage decreased by 35 % from the nominal value during the time interval from t=0.05 sec to t=0.15 sec as shown in Fig. 6.1 (a). As soon as the controller sensed a decrease in the supply voltage, the compensation voltage signals were produced automatically. As a result, the bus-2 series compensator injected the necessary compensation voltage as seen in Fig. 6.1 (b) to keep the sensitive load-2 insensitive to changes in the supply voltage. It was also observed that this injected voltage reduced the effect of the fault, while the terminal voltage of the sensitive load-2 was seen in Fig. 6.1 (c) has been held at the desired level.
Similarly, the "a" and "c" phases in the bus-3 supply voltage decreased by 35% from the nominal value during the time intervals from t=0.05 sec to t=0.15 sec due to system faults. The bus-3 series compensator reacted quickly to the decrease in the supply voltage and the corresponding correction voltage was injected as shown in Figs 6.2 (b). The resulting side load voltage waveforms were found to be at the desired level as seen in Fig 6.2 (c). The effects of DS fault on customers in bus-2 and bus-3 for this case study is summarized in Table-1.

Table-1: Measured voltages of GUPQC during LG fault at bus-2 and DLG fault at bus-3

Bus	Phase	Supply Voltage	Injecting Voltage	Load Voltage
2	Phase-a	275	155	393
	Phase-b	415	12	408
	Phase-c	415	12	408
3	Phase-a	274	153	406
	Phase-b	274	153	406
	Phase-c	415	6	410

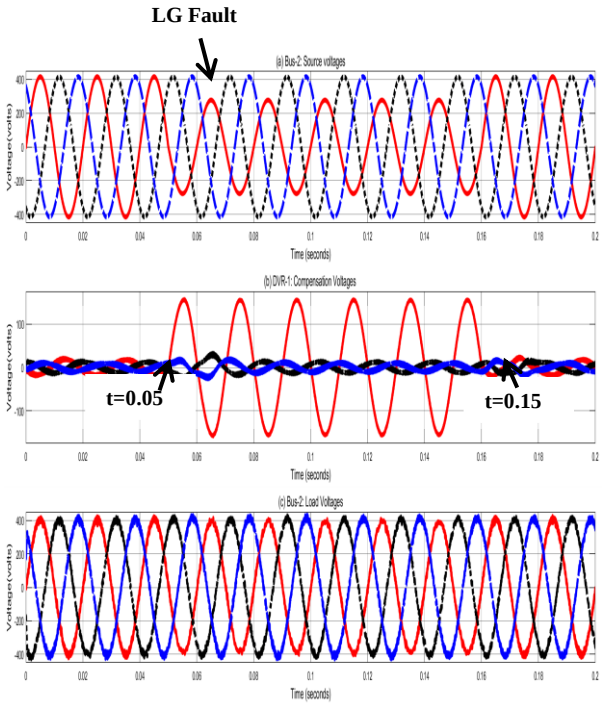

Figure 6.1: LG fault compensation of bus-2, (a) Supply voltages,
(b) DVR-1 compensation voltages and (c) Load voltages

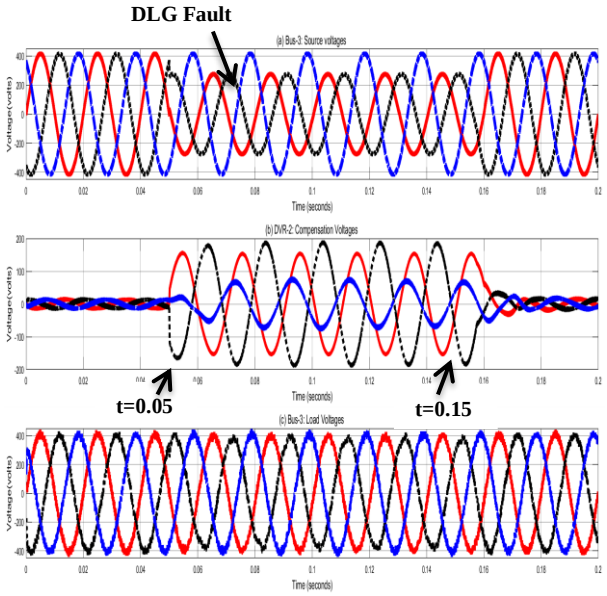

Figure 6.2: DLG fault compensation of bus-2, (a) Supply voltages,
(b) DVR-2 compensation voltages and (c) Load voltages

Case-2: 3LG fault at bus-2 and LG fault at bus-3

The response of the proposed GUPQC for applying a 3LG fault on bus-2 and a LG fault on bus-3 during time intervals from t=0.05 sec to t=0.15 sec as seen in Figs. 6.3 (a) to (c) and Fig. 6.4 (a) to (c) respectively. Due to the fault in bus-2, all three phases voltage decreased by 50 % from the nominal value during the time interval from t=0.05 sec to t=0.15 sec as shown in Fig. 6.3 (a). As soon as the controller sensed a decrease in the supply voltage, the compensation voltage signals were produced automatically. As a result, the bus-2 series compensator injected the necessary compensation voltage as seen in Fig. 6.3 (b) to keep the sensitive load-2 insensitive to changes in the supply voltage. It was also observed that this injected voltage reduced the effect of the fault, while the terminal voltage of the sensitive load-2 was seen in Fig. 6.3 (c) has been held at the desired level.

Similarly, the "a" phase in the bus-3 supply voltage decreased by 25% from the nominal value during the time intervals from t=0.05 sec to t=0.15 sec due to system faults. The bus-3 series compensator reacted quickly to the decrease in the supply voltage and the corresponding correction voltage was injected as shown in Figs 6.4 (b). The resulting side load voltage waveforms were found to be at the desired level as seen in Fig 6.4 (c). The effects of DS fault on customers in bus-2 and bus-3 for this case study is summarized in Table-2.

Table-2: Measured voltages of GUPQC during 3LG fault at bus-2 and LG fault at bus-3

Bus	Phase	Supply Voltage	Injecting Voltage	Load Voltage
2	Phase-a	207	223	385
	Phase-b	207	223	385
	Phase-c	207	223	385
3	Phase-a	310	116	408
	Phase-b	415	7	410
	Phase-c	415	7	410

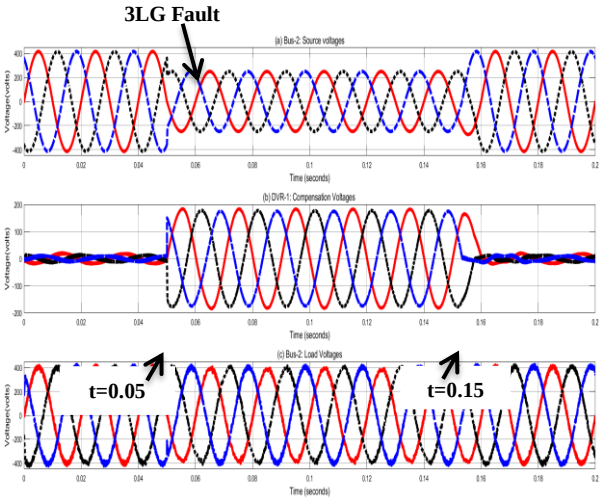

Figure 6.3: TLG fault compensation of bus-2 (a) Supply voltages,
(b) DVR-1 compensation voltages and (c) Load voltages

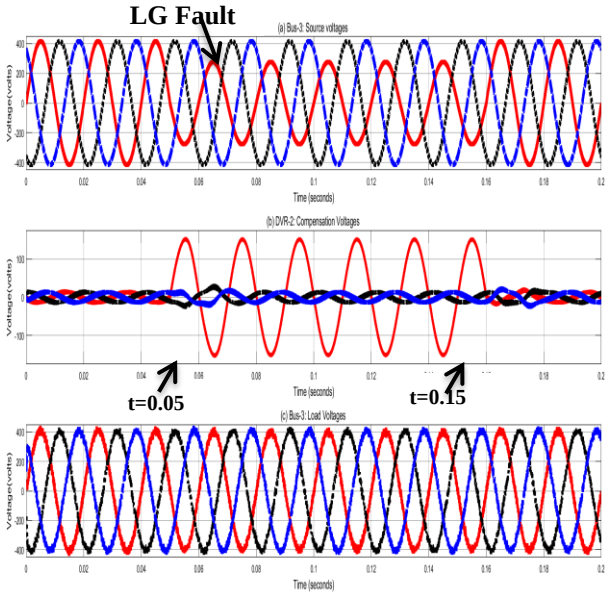

Figure 6.4: LG fault compensation of bus-2 (a) Supply voltages,
(b) DVR-1 compensation voltages and (c) Load voltages

Case-2: 3L fault at bus-2 and 2L fault at bus-3

The response of the proposed GUPQC for applying a 3L fault on bus-2 and a DL fault on bus-3 during time intervals from t=0.05 sec to t=0.15 sec as seen in Figs. 6.5 (a) to (c) and Fig. 6.6 (a) to (c) respectively.

Due to the fault in bus-2, all three phases voltage decreased by 50 % from the nominal value during the time interval from t=0.05 sec to t=0.15 sec as shown in Fig. 6.5 (a). As soon as the controller sensed a decrease in the supply voltage, the compensation voltage signals were produced automatically. As a result, the bus-2 series compensator injected the necessary compensation voltage as seen in Fig. 6.5 (b) to keep the sensitive load-2 insensitive to changes in the supply voltage. It was also observed that this injected voltage reduced the effect of the fault, while the terminal voltage of the sensitive load-2 was seen in Fig. 6.5 (c) has been held at the desired level.

Similarly, the "a" & “b” phases in the bus-3 supply voltage decreased by 30% from the nominal value during the time intervals from t=0.05 sec to t=0.15 sec due to system faults. The bus-3 series compensator reacted quickly to the decrease in the supply voltage and the corresponding correction voltage was injected as shown in Figs 6.6 (b). The resulting side load voltage waveforms were found to be at the desired level as seen in Fig 6.6 (c). The effects of DS fault on customers in bus-2 and bus-3 for this case study is summarized in Table-3.

Table-3: Measured voltages of GUPQC during 3LG fault at bus-2 and LG fault at bus-3

Bus	Phase	Supply Voltage	Injecting Voltage	Load Voltage
2	Phase-a	201	219	395
	Phase-b	201	219	395
	Phase-c	201	219	395
3	Phase-a	298	128	409
	Phase-b	298	128	409
	Phase-c	415	2.8	415

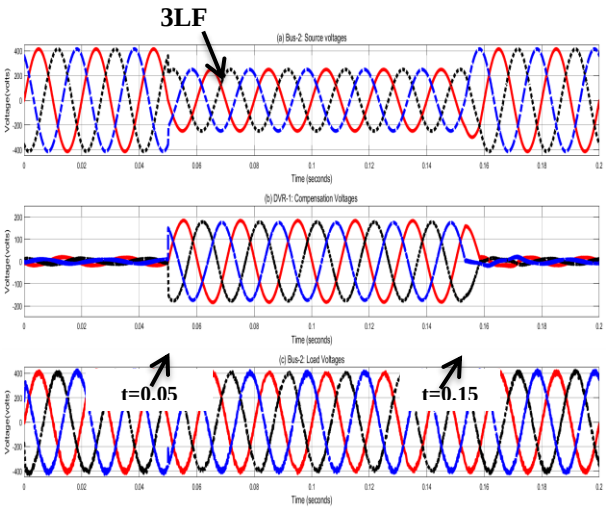

Figure 6.5: 3L fault compensation of bus-2, (a) Supply voltages,
(b) DVR-1 compensation voltages and (c) Load voltages

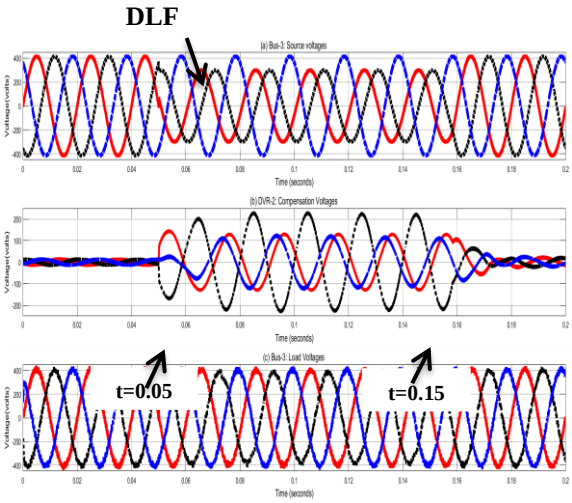

Figure 6.6: DLG fault compensation of bus-3 (a) Supply voltages,

(b) DVR-2 compensation voltages and (c) Load voltage

V. CONCLUSION

In this paper, the simulation of a GUPQC is done using SIMULINK software. The performance of GUPQC under different fault conditions for large distribution network is easier analyse. Voltage quality due to faults in the distribution system is affected in terms sag creation in one phase or other based on the fault. DVR is improving the quality of voltage and DSTATCOM compensate the current harmonics effectively, it can clearly show in the simulation results. GUPQC forms the quick and efficient custom power device has shown the performance and effectiveness on power quality improvement The proposed work showed that GUPQC can able to compensate upto 60% magnitude of voltages of three phase faults at bus-2 and bus-3 simultaneously.

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