SSRG International Journal of Electrical and Electronics Engineering
ISSN: 2348 – 8379 /doi:10.14445/23488379/IJEEE-V7I11P102

Volume 7 Issue 11, 8-13, November 2020
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Converter Design Advanced Output Voltage Stability

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Abstract

The paper introduces the structure diagram and the pulse transducer's operation with the intermittent current mode sensor (CBDGD) to determine when the transducer switches to the intermittent current mode and part of the switching cycle of a transistor when the transducer is in interrupting current mode. The converter's feedback diagram and the interrupt current sensor generates the converter's corresponding feedback signal to ensure stability for the output voltage in the intermittent current mode. Since then, there is an additional solution to improve the pressure reducer's voltage output stability, improving the reliability and stability of electrical and electronic systems.

Keywords — *Inverter, converters, pressure reducers, turbochargers.*

I. INTRODUCTION

One of the criteria for evaluating pulse converters is the stability of the output voltage when adjusted across the load's entire variable region. The pulse converter can operate in both continuous and interrupt current modes depending on whether the inductor current reaches zero after one switching cycle. In constant current mode, the converter output voltage is independent of load and is set for the buck converter . For boost converters $U_{out} = U_{in}/(1-D)$, where U_{out}, U_{in} are the converter's output and input voltage, D - is the pulse fill factor.

In summary, the output voltage stability of the converter in the continuous current mode is sufficiently large. In practice, the pulse converter's output voltage instability in continuous current mode needs to be zero because the output voltage is independent of the load. However, there is an increase in real converters' load, a small drop in output voltage due to some imprecise parameters [4], [7]. In the current interrupt mode, the output current is not large enough to prevent the inductor current from falling to zero after one switching cycle. DC voltage converters operating in the interrupt current mode have a small fill factor compared to the continuous current mode for the same input and output voltage. This difference in magnitude of the pulse fill factor increases its output voltage, which reduces its stability. In converters containing an error amplifier, this amplifier's amplification allows the converter to interrupt current mode with small output voltage variations. The application of an error amplifier in a pulse converter complicates controller design because it needs to compensate for changes in load and temperature simultaneously.

Additionally, the error amplifier greatly increases the current consumption of the power converter driver [1]. Hence, in small battery-operated devices, it is often not desirable to contain error amplifiers. In these converters, the output voltage is directly compared to the jagged voltage, from which to change the pulse fill factor, the output voltage needs to change more. The larger the difference between the output voltage and the jagged voltage, the more the converter is affected by its instability.

II. CONVERTERS DESIGN

Two factors that play an important role in determining at what load the converter switches from continuous to interrupted current are the switching frequency and inductance value of the inductor [1], [4], [5]. Once these parameters are defined, it will not be possible to adjust the load area where the converter enters the interrupt current mode, thereby eliminating high output voltage instability. The block diagram of the pressure reducing unit is shown in Figure 1. This block is made up of a control and force circuit that contains transistor VT1, inductor L, reverse diode VD, complementary transistor VT2 acts as a set synchronous rectifier, and a capacitor C. Transistors VT1 and VT2 are controlled by driver [2], [6]. The interrupt diagram is similar to that used in the synchronous rectifier control scheme to block conduction in the current interrupt mode and capacitor C's discharge.

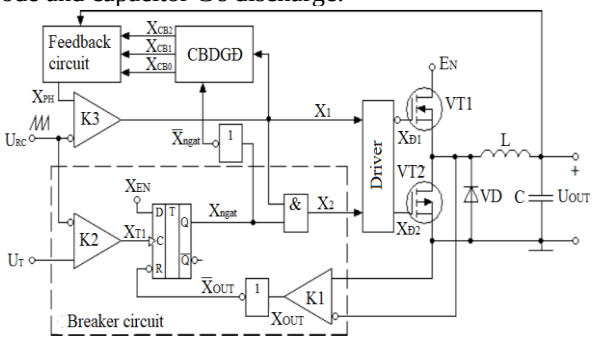

Figure 1: Function diagram of the pressure reducer

The comparator K1 generates a X_{OUT} signal, supplied to the input of the inverter. The $\overline{X}_{OUT}$ signal from the output of the inverters feeds the trigger input R (trigger). The X_{T1} clock signal for the trigger is generated by a K2 comparator that compares the U_{RC} input jagged signal with a quasi-U_T voltage. On the trigger, data input (D - input) is provided with pin voltage X_{EN}. When the voltage on the reverse diode drops to 0 when the inductor current drops to

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0, the K1 comparator switches, this signal is used by a synchronous rectifier that prevents current from passing through the synchronous transistor in current interrupt mode to prevent capacitor C's discharge to the ground. The signal on the logic element "AND" input and the low transition of the control signal X_{D2} will result in the lockout of transistor VT2 synchronously. When the $\overline{X}_{ngat}$ signal level, which is the input signal of the intermittent current mode sensor, is low and fixed at the pin, the negative current stops flowing through the synchronous rectifier. This signal remains fixed in the pin until the clock signal is synchronized with signal X_1 will not take a value of 1, and the circuit will again not start monitoring the inductor's current. The U_{RC} jagged signal is fed to the K3 comparator, compared with the X_{PH} feedback signal, while the output is fed to the driver that drives transistors VT1 and VT2. The signal X_1 is fed to the intermittent current mode sensor; the sensor's output will generate X_{C0}, $X_{C1,}$ and X_{C2} signals for the feedback circuit. The converter output voltage is also fed to the feedback circuit. When the voltage across the reverse diode VD and complement transistor VT2 is 0, the comparator K1 will generate the X_{OUT} signal to generate $\overline{X}_{OUT}$ the signal. This signal will reset the trigger's R-value, returning the signal value equal to 0. Then the output signal of the interrupt circuit will be 0. The signal form of the interrupt diagram is shown in Figure 2.

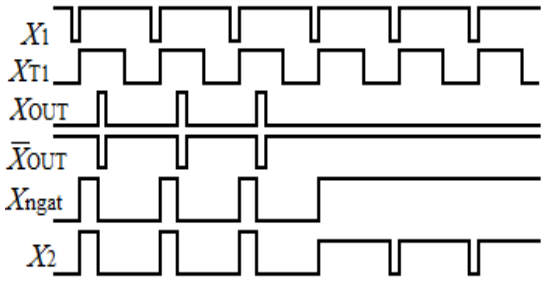

Figure 2: Signals generated by interrupt diagram

The X_{ngat} signal is kept low until the K2 comparator generates the next XT1 clock. The schematic diagram for determining the inductor current disruption is shown in Figure 3. In the diagram, the converter's period has been saved in interrupt current mode with resolutions within the range 1/4 cycle of the clock signal. Increasing the resolution of this schematic can be done with any number of triggers. 1/4 cycle resolution level requires 3 DD1 DD2 and DD3 triggers. X_{T2} signal - a series of pulses with a frequency 4 times higher than the converter's switching frequency.

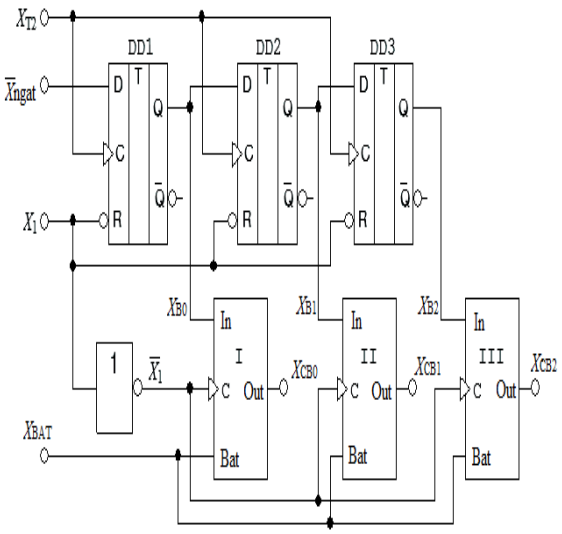

Figure 3: Diagram of intermittent current mode sensor

Each front side of the X_{T2} signal changes $\overline{X}_{ngat}$ signal state, which alternately shifts the sequence of DD1, DD2, and DD3 triggers. Because the frequency of X_{T2} is four times greater than the converter's switching frequency, on each switching cycle of the converter, there are four front sides of the X_{T2} signal. Hence each of the first front sides of the X_{T2} signal is positioned concurrently with the front sides of the X_1 and X_2 signals, and there are only three front sides before which it can begin to increase the signal. If the signal rises to the second front-side X_{T2}, the boundary signal will be completely shifted through the three triggers. If it rises behind the second front side but before the 3rd front side of the XT2, the signal only passes through actives 2 and 3. If the signal increases after the 3rd front side but before the 4th front side, it is only moved by the first trigger. Each trigger from triggers Q1, Q2, and Q3 will be assigned to the inputs I, II, and III devices, respectively. This second trigger is used to confirm that the transducer's inductor current disruption is stable but is not caused by the transition. The output devices I, II, and III are used to calibrate the feedback circuit (Figure 1). Signal X_1 is fed to the inverter, whose output will produce the clock signal. X_{BAT} - is the enable signal for Bat inputs of devices I, II, and III. The timing graph showing the working diagram in Figure 3 is shown, as shown in Figure 4. The output of the first trigger DD1 (X_{B0}), second DD2 (X_{B1}), and third DD3 (X_{B2}) shows the dependence of the inverse input state X_2 on the $\overline{X}_{ngat}$ signal corresponding to the part of the cycle where the inductor is in the current interrupt mode. The X_{T2} signal is approximately 4 times the clock frequency of the system when comparing this signal with signal X1, which after reversing in the schematic, it is fed to transistor VT2 in the form of signal X_{D2}.

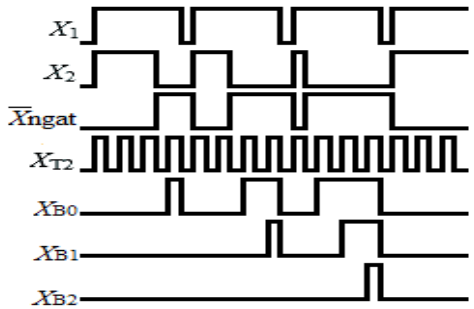

Figure 4: Time charts of the intermittent current mode sensor

Each device I, II, III in Figure 3 has a schematic diagram, as shown in Figure 5. Its function is to ensure that the interrupt mode of interrupting currents has been established without the lose some control in the process. Each of these devices is made up of triggers DD1, DD2,…, DDN. The number of triggers will determine the time during which the signal needs to be kept constant. Input D of the first trigger of blocks I, II, and III will be connected corresponding to the outputs of the triggers DD1, DD2, and DD3 in Figure 3. In Figure 3, it is denoted X_{Bi} (where i is the natural numbers).

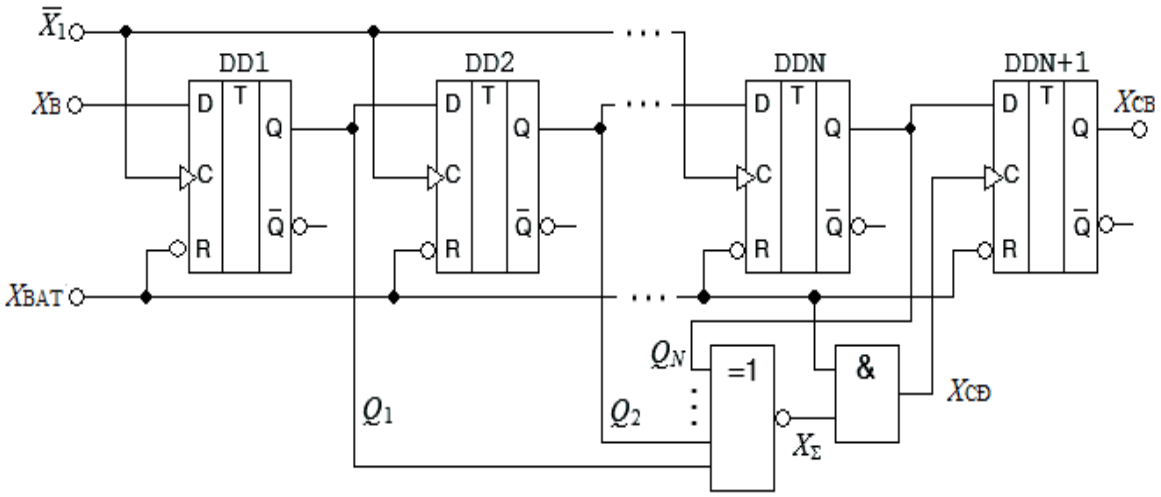

Figure 5: Structure diagram of blocks I, II, and III

The trigger chains of these blocks will be fed the $\overline{X}_1$ clock signal, so when the X_{Bi} output is sequential in all N switching cycles, the outputs of all triggers have the front ribs of the signal brand. If the output of all triggers is the same, then the output of the XOR element. NOR will be the high-level signal. When the on signal keeps high, the part output from AND repeats the XOR.NOR element output state. The AND element output - which is a fixed signal ($X_{CĐ}$) - is connected to the pulse input of the trigger DDN + 1. Input D of trigger DDN+1 is connected to the output of trigger DDN. This allows keeping the output state (X_{Bi}) of one of the DD1, DD2 or DD3 triggers (Figure 3) fixed for about N cycles when the output state is held constant and held until one of The output states of the DD1, DD2 or DD3 triggers change to store this new state. The time chart explaining the operation of the diagram in Figure 5 is shown in Figure 6.

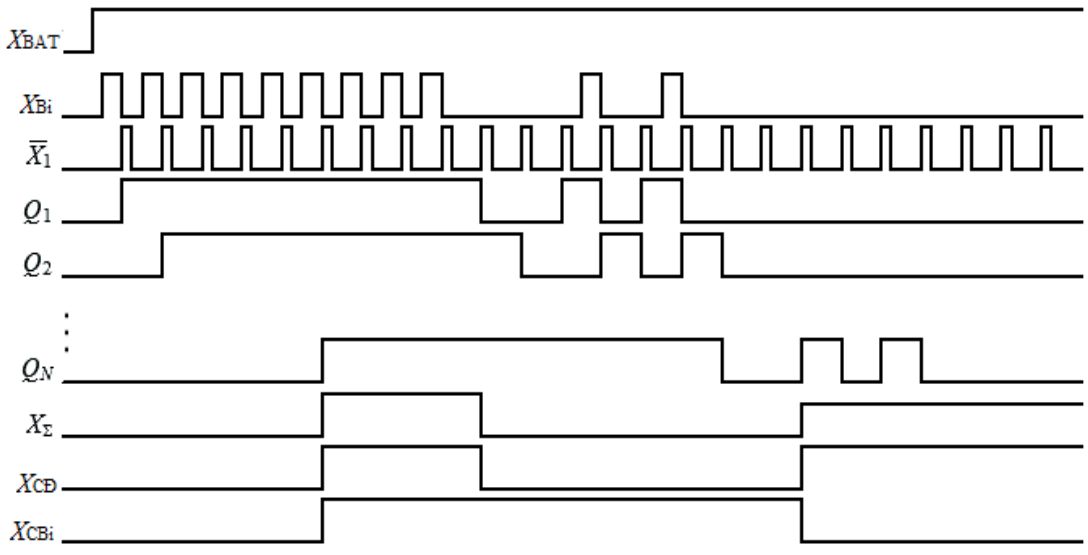

Figure 6: The timing diagram of the corresponding signals with the figure 5 schematic

The signal X_{Bi} - is one of the X_{B0}, $X_{B1,}$ or X_{B2} signals (Figure 3). As soon as the signal level turns on X_{BAT} is high, the chain of triggers DD1, DD2, ..., DDN will shift this signal by signal $\overline{X_1}$. At the end of the N cycles, if the output states of all triggers are denoted Q_1, Q_2, ..., Q_N are the same. With the help of signal, X_Σ will generate the signal X_{CD}, the signal This will pass the output state of trigger N to DDN+1 to generate a signal X_{CBi}, which is one of the signals X_{CB0}, X_{CB1} or X_{CB2} in figure 3. The outputs of all blocks I, II, III are used to calibrate the converter feedback circuit. The feedback circuit diagram is shown in Figure 7.

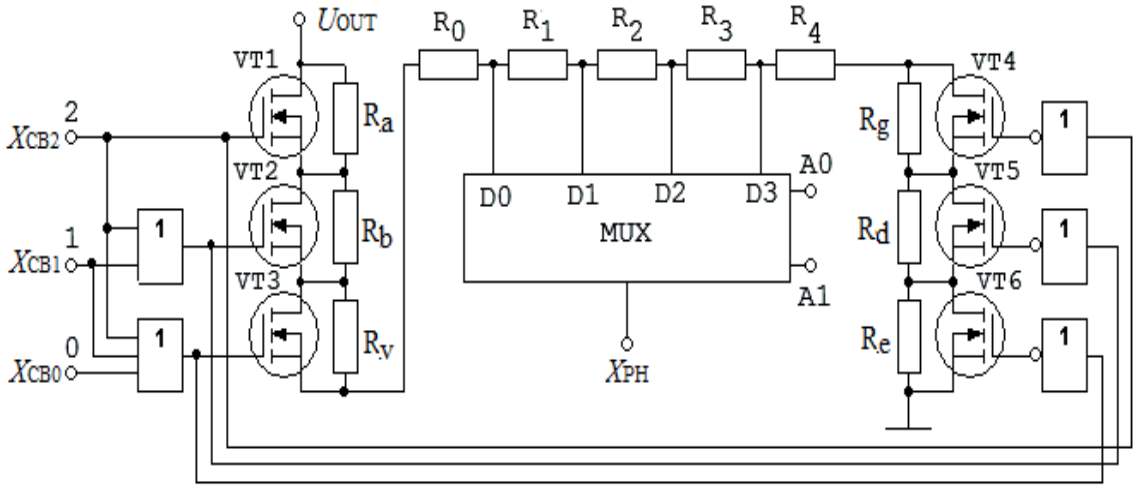

Figure 7: Diagram of the pressure relief feedback circuit

The feedback circuit comprises a resistor divider consisting of resistors R_a, R_b, R_v, R_0, R_1, R_2, R_3, R_4, R_g, $R_{d,}$ and R_e, connected between the output terminal (U_{OUT}) of the converter and land. Resistors R_1, R_2, $R_{3,}$ and R_4 are used to guarantee different levels of the converter's adjustable output voltage. The taps of a voltage divider R_0, ..., R_4 are connected to a multiplexer (MUX). The multiplexer uses signals A0 and A1 to select one of the divider coefficients guaranteed by the resistors R_1, ..., R_4. The select output is connected to the multiplexer's output, where the X_{PH} feedback signal is formed. On inputs 0, 1, and 2 are fed the output signals from the intermittent current mode sensor X_{CB0}, $X_{CB1,}$ and $X_{CB2,}$ respectively. The signal X_{CB2} on input 2 is fed to the base terminal of the transistor VT1 connected in parallel to the resistor R_a. This signal also passes through a rectifier and is fed to the base terminal of the transistor VT4 connected in parallel with the resistor R_g. The signal X_{CB1} is fed to the input of a two-input element OR, on its second input is fed by the signal X_{CB2}. The output of the 2OR element is connected to the base terminal of the transistor VT2 connected in parallel to the resistor R_b. This signal also passes through an inverter and then to the base terminal of VT5 connected parallel to the resistor R_d. The signal X_{CB0} is applied to the 3rd input of the 3OR element. The remaining inputs of this element are supplied by the signals X_{CB2} and $X_{CB1,}$ respectively. The output of the 3OR element is connected to the base terminal of the transistor VT3 connected in parallel with the resistor R_v. It also passes through an inverter and then the transistor's base terminal VT6 is connected in parallel with the resistor R_e.

The signals X_{CB0}, $X_{CB1,}$ and X_{CB2} are used to reduce the pulse converter's output voltage when operating in the current interrupt mode. When the 0, 1, or 2 inputs appear on the inputs due to the intermittent current mode, they turn on transistors VT1, VT2, and VT3 to short the resistors R_a, $R_{b,}$ or R_v. Transistors VT4, VT5, and VT6 are then switched off, and resistors R_g, $R_{d,}$ and R_e are added to the splitter's series of resistors. This will increase the feedback signal, leading to a drop in the converter's output voltage. If the pulse converter is actually in intermittent current mode, the signals X_{CB2}, X_{CB1} and X_{CB0} will be high and turn on transistors VT1, VT2, and VT3, they will short-circuit the resistors R_a, $R_{b,}$ and R_v. Also, in This time, transistors VT4, VT5, and VT6 will be switched off, and resistors R_g, $R_{d,}$ and R_e will be added to the sequence of resistors of the splitter. This will maximize the feedback signal, which will maximize the transformer output voltage drop. If the pulse converter is close to the continuous and intermittent current mode, the X_{CB0} signal will be high, just opening the transistor VT3 will short the resistor R_v. Transistors VT2 and VT3 will be switched off. Also, during this time, transistors, VT6 will be turned off, resistor R_e is added to the sequence of resistors of the splitter. This maximizes the increase in the feedback signal, leading to a minimal drop in the converter's output voltage. In a nutshell, the structure of this dc voltage reducer improves the output voltage stability of the converter when working in intermittent current mode and improves the system's working stability.

III. EXPERIMENTAL RESULTS

To verify the results, the experimental model is built, as shown in Figure 8 below. The model is built to ensure that when the input voltage changes in the 15V to 60V range, the output voltage remains 12 V. The output voltage pattern of the low-voltage converter when the input voltage changes from 0 to 60V shaped like Figure 9.

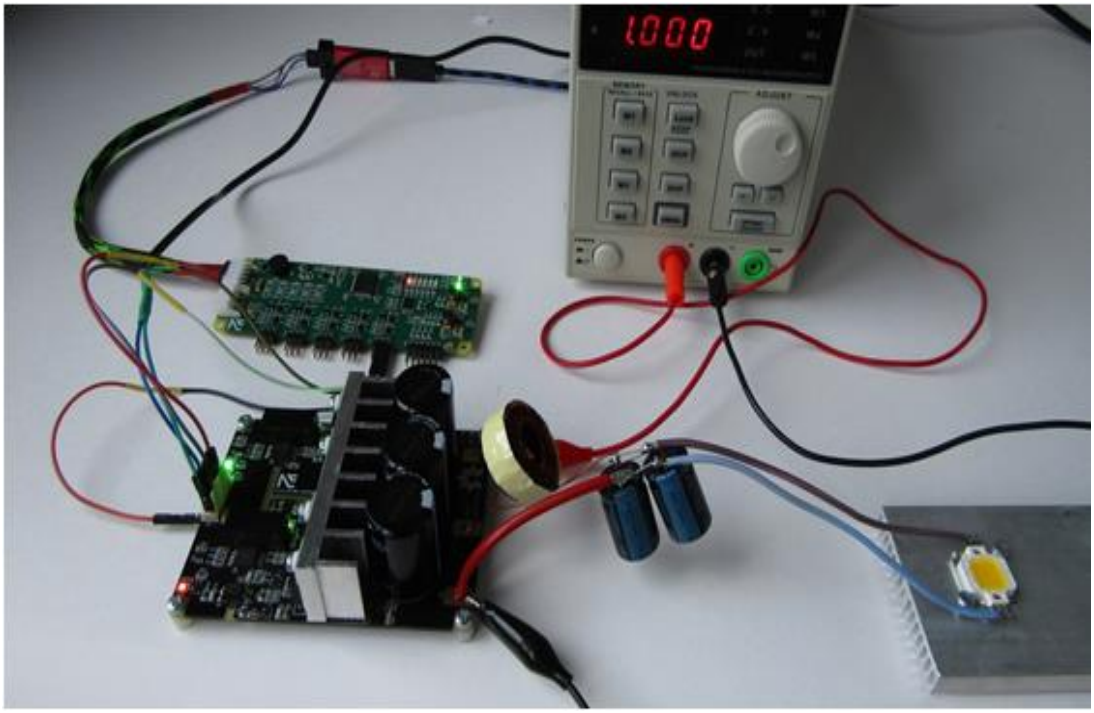

Figure 8: Experimental model of the feedback low-voltage set

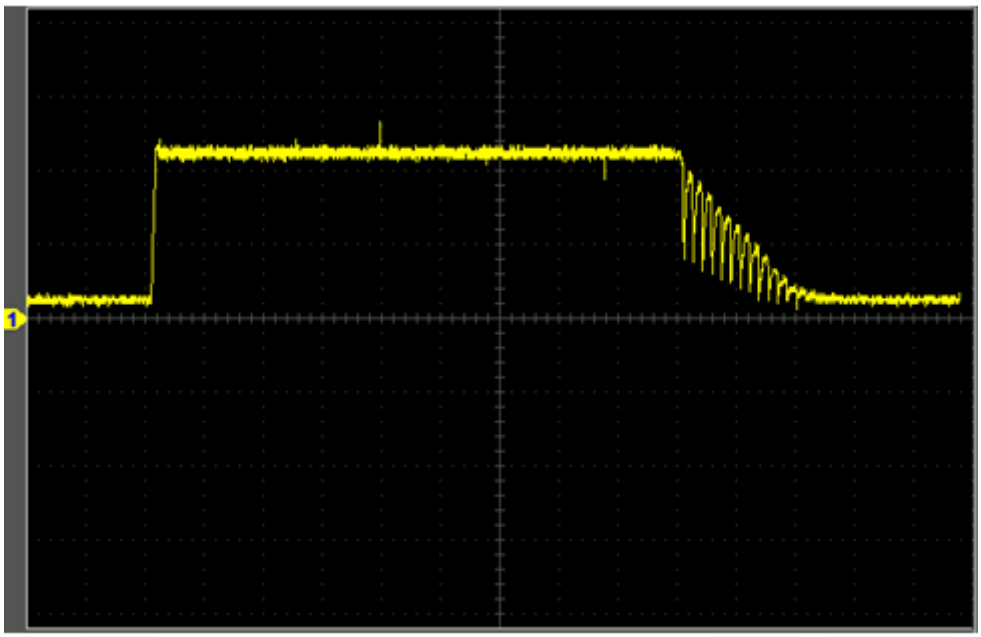

Figure 9: Low voltage output voltage pattern

From the measured output voltage results in figure 9, it is found that when the voltage changes from 0 to 15V, the output voltage does not increase when the input voltage is greater than 15V and less than 60V, the output voltage remains at the 12V level with small fluctuation noise, when the input voltage drops below 15V, the output voltage drops to as low as originally. This reduction takes place longer than increment. This depends on the mach capacitor specifications. However, the experimental model's purpose was achieved when it was to show the stability of the output voltage when changing input voltage values.

IV. CONCLUSIONS

The paper questioned the stability of the output voltage of the converters, outlined the disadvantages of using an error amplifier to regulate the output voltage, at the same time give a schematic diagram of a low voltage converter with an intermittent current mode sensor to create a feedback signal contribute to stabilizing the output voltage value. The content presented the blocks' operating principles in the low-voltage converter diagram, the formation principle, and time diagrams describing the operation of each element. The DC voltage reducer scheme's construction is given, allowing the output voltage

of the low voltage converter to be stabilized when working in intermittent current mode.

ACKNOWLEDGMENT

This study was supported by the University of Economics - Technology for Industries, Viet Nam; http://www.uneti.edu.vn/.

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