A Chirality Based Noise Margin Analysis of Carbon Nanotube FET Devices

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Abstract *— Carbon nanotubes have shown great promises in the field of nano-electronic devices by the enhancement of overall performance matrices compared to traditional silicon-based devices. The goal of this paper is to seek for ways how to influence the performance of digital devices by varying the property of the carbon nanotubes. Our work focuses on the chiral property of the nanotubes and its impact on the noise margin of the inverter. We have designed a 6T SRAM to analyze the relation between N-curve stability parameters and the chirality of the channel. Simulation and analysis using CNTFET show promising results in enhancing the robustness and stability of digital devices.*

Keywords *— CNTFET, chirality, threshold voltage, noise margin, SRAM, N-curve.*

I. INTRODUCTION

For the last couple of decades, the trend of scaling in the semiconductor industry has been accurately predicted by Moore's Law [1]. Scaling down the feature size to fit more and more transistors in a single chip has been a major research interest for a very long time. The channel length of transistor has shrunk from several microns to a few nanometers for improved functionality and to lower down the cost. The extreme scaling of the silicon-based transistor has resulted in several drawbacks over the years such as reduced gate control, higher leakage current, threshold voltage roll-off, process variations, etc. Researchers have been looking for alternative to silicon technology to keep up with the increasing need for smaller transistors. As we are reaching the limits of scaling in silicon-based devices, the necessity to find alternative technology is now more than ever. In that case, carbon nanotube transistors are very promising. Replacing the silicon channel with carbon nanotubes can offer unique and promising features. With ultralong (~1μm) mean free path for elastic scattering a ballistic or near-ballistic transport can be obtained to improve performance under low voltage [2]. The one-dimensional band configuration of carbon nanotubes smothers backscattering effect and makes quasi-ballistic transport a practical chance. [3]. Carbon nanotubes (CNTs) are very large molecules made up of single (SWCNT) or multi-layer (MWCNT) rolled-up walls of carbon atoms. SWCNT is formed by rolling up a cut out of carbon lattice along one of the Bravis lattice vectors [4]. The electronic property of a CNT depends on how the graphene sheet is rolled which is referred to as chirality [5]. Nanotubes can be chiral or achiral. The chiral property of an SWCNT is denoted by a single vector, $\mathbf{C} = \mathbf{ma_1}+\mathbf{na_2}$. The chiral angle, $\boldsymbol{\theta}$ determines the twisting of the nanotube which is the angle between **C** and $\mathbf{a_1}$. Nanotubes can be chiral or achiral. Chiral nanotubes have $0^{\circ} < \theta < 30^{\circ}$ and they are expressed as **(m, n)** when $n \neq 0$. Achiral nanotubes have two types such as zigzag nanotube structure (m,0) with $\theta = 0^{\circ}$ and armchair nanotube structure (m, n) with $\theta = 30^{\circ}$. For, n = m, CNT is metallic. CNT is quasi-metallic, if (n-m) is a multiple of 3 ($n \neq m$ & $nm \neq 0$). If (n-m) is not a multiple of '3', CNT is moderately semiconducting [6]. This kind of configuration in the channel region ensures improved electrostatic control than three dimensional CMOS or two dimensional SOI devices [7].

CNTFET is a very promising option to complement the long tradition of silicon technology to design faster devices and reduced cost of power as it avoids many of the fundamental limitations of silicon-based transistors. This work is intended to explore the possibility of performance improvement for carbon nanotube-based devices. Simulation results shows the impact of channel CNT chirality on the robustness of digital logic devices such as inverter and SRAM. This study was conducted using zigzag type, semiconducting carbon nanotubes as a channel material to investigate the impact of chirality on CNTFET performance.

II. LITERATURE REVIEW

In 1991, both Iijima & Ichihashi and Bethune *et al.* independently reported the discovery of single wall carbon nanotube with diameter in nanometer range [4, 8]. Three kinds of nanotubes have been found according to their chiral properties: armchair, chiral, and zigzag. Chiral features are responsible for the structural and electrical properties of carbon nanotubes. The thinnest free-standing SWCNT is 0.43nm in diameter [9]. In CNTFET, the best way to control the channel properties is to change the physical properties of a carbon nanotube. The threshold voltage of a CNTFET was found to depend on the chiral vector of the nanotube by Sinha and Chaudhury in 2015 [10]. Again, De Vusser *et al.*

found that the noise margin of the OTFT inverter is related to the threshold voltage of the transistors [11]. These studies reveal a promising concept regarding the noise margin of digital logic devices. Variation of the chiral properties of channel materials can contribute to the improvement of the noise margin and overall stability of CMOS devices and SRAM cells. A comparison between multiple SRAM cells by Lin *et al.* in 2006 shows both SNM and write time have higher values for higher chirality CNT [12]. But Static Noise Margin (SNM) graph cannot perform the measurement with automatic inline testers and also unable to study SRAM stability fails with statistical data which is major drawback of SNM [13]. Even with the big promises, CNTFET related researches have been tackled by the obstacles in the production of CNTs. Carbon nanobelts (CNB) have been receiving a great deal of attention since they partially represent the structure of CNT and can play a major role in the proper synthesis of CNT. Though both chiral CNB and armchair CNB synthesis were reported previously, zigzag CNBs synthesis has been reported by Cheung *et al.* in 2020 [14]. X-ray crystallography confirms that obtained zigzag CNB has the sidewall CNT with (18,0) chiral index. These results greatly increase the possibility of precise chiral vector selective synthesis and isolation of CNT in near future for their application in the semiconductor industry.

III. METHODOLOGY

A. Carbon nanotube

Carbon nanotubes are very large molecules made from single or multi-layer rolled-up walls of carbon

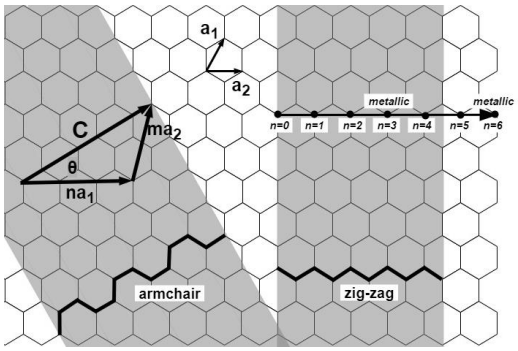

Fig 1: CNT structure and chiral vector

atoms. The diameter and the chiral angle of a nanotube are given with the following equations [15].

$$D_{CNT} = \left(\frac{\sqrt{3}a_0}{\pi}\right)\sqrt{n^2 + \mathrm{mn} + n^2} \quad (1)$$

$$\theta = tan^{-1}\left(\frac{\sqrt{3}m}{2n+m}\right) \quad (2)$$

Where inter molecule distance, a_0 = 0.142 nm and 'D_{CNT}' is the diameter of CNT in nanometer. The diameter and the chiral angle determine the structural and electrical properties of the nanotube. The relation between diameter and threshold voltage is given by the following

$$V_{th} = \frac{E_g}{2e} = \frac{aV_\pi}{\sqrt{3}qD_t} \quad (3)$$

Where, a = 2.49 Å, is the lattice constant, Vπ = 3.033 eV, is the carbon to carbon π bond energy and q is electronic charge. The threshold voltage here is inversely proportional to the diameter of the nanotube [10]. Thus, varying the chiral vector of the channel nanotubes can provide an excellent opportunity to control the threshold voltage of carbon nanotube transistor.

B. The CNTFET Inverter

The inverter is one of the most important aspects of digital design. The electrical behavior of many intricate devices such as complex gates and microprocessors can be derived by extrapolating the results obtained from a detailed study of the inverter. In ideal cases, an inverter has a high noise margin.

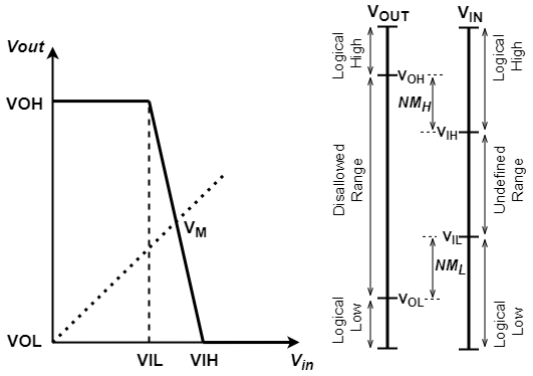

Fig 2: VTC and noise margin of inverter

Taking $I_{ds,n} = I_{ds,p}$ and solving for input voltages of both transistors gives the desired transfer characteristic for CMOS inverter. The transfer curve shows that an inverter has high gain in the switching region and that results in a narrow transition zone, while both nMOS and pMOS are in saturation. CMOS inverter uses a ratio of 3:1 or 2:1 of pMOS and nMOS width to account for the higher carrier mobility in nMOS. Similar current operating capabilities for CNT based transistors enables this inverter design to take the transistor ratio as 1 in our work. To guarantee the unwavering quality of a digital circuit, one needs to think about some proportion of reliability. Noise margin is often used as parameter to measure the robustness of a CMOS inverter. In 1960s Hill defined it as "the maximum allowable spurious signal that can be accepted by a device when used in a system while still giving correct operation" [16]. Following a piecewise linear approximation for the voltage transfer curve, the switching region can be estimated by a straight line shown in figure 2. It has same gain 'g' as the gain at

switching threshold, V_M. In case of an inverter, $V_{IN} < V_{IL}$ produces 'logic 0' in the output and slope, $\frac{dV_{OUT}}{dV_{IN}} = -1$. If $V_{IN} > V_{IH}$, it produces 'logic 1' in the output and slope, $\frac{dV_{OUT}}{dV_{IN}} = -1$. The width of the transition region is V_{IH} - V_{IL}. An inverter circuit has both high and low noise margin. The measurement of noise margin gives the following relations. These

$$V_{IH} - V_{IL} = -\frac{V_{OH} - V_{OL}}{g} = \frac{-V_{DD}}{g} \quad (4)$$

$$V_{IH} = V_M - \frac{V_M}{g} \quad (5)$$

$$V_{IL} = V_M + \frac{V_{DD} - V_M}{g} \quad (6)$$

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH} \quad (7)$$

$$NM_L = V_{IL} - V_{OL} = V_{IL} \quad (8)$$

expressions make it very obvious that high noise margin is always desirable. To investigate further the drain current equations are used. When $V_{IN} = V_{IL}$, the nMOS is in saturation region and the pMOS is in linear region.

$$I_{D,p} = \frac{k_P}{2}\left[2(V_{GS,p} - V_{T,p})V_{DS,p} - V_{DS,p}^2\right] \quad (9)$$

$$I_{D,p} = \frac{k_P}{2}\left[2(V_{IN} - V_{DD} - V_{T,p})(V_{OUT} - V_{DD}) - (V_{OUT} - V_{DD})^2\right] \quad (10)$$

$$I_{D,n} = \frac{k_n}{2}(V_{GS,n} - V_{T,n})^2 = \frac{k_n}{2}(V_{IN} - V_{T,n})^2 \quad (11)$$

$$I_{D,p} = I_{D,n} \quad (12)$$

$$\frac{k_n}{2}(V_{GS,n} - V_{T,n})^2 = \frac{k_P}{2}\left[2(V_{IN} - V_{DD} - V_{T,p})(V_{OUT} - V_{DD}) - (V_{OUT} - V_{DD})^2\right] \quad (13)$$

Differentiating with respect to V_{IN} and substituting produce the following equations.

$$V_{IN} = V_{IL}, \frac{dV_{OUT}}{dV_{IN}} = -1 \quad (14)$$

$$k_n(V_{IL} - V_{T,n})^2 = k_P\left[(V_{IN} - V_{DD} - V_{T,p})\frac{dV_{OUT}}{dV_{IN}} + (V_{OUT} - V_{DD}) - (V_{OUT} - V_{DD})\frac{dV_{OUT}}{dV_{IN}}\right] \quad (15)$$

$$k_n(V_{IL} - V_{T,n})^2 = k_P\left[(V_{IN} - V_{DD} - V_{T,p})(-1) + (V_{OUT} - V_{DD}) - (V_{OUT} - V_{DD})(-1)\right] \quad (16)$$

$$V_{IL} = \frac{2V_{OUT} + V_{T,p} - V_{DD} + k_R V_{T,n}}{1 + k_R} \quad (17)$$

Where, $k_R = \frac{k_n}{k_p}$, $k_n = \mu_n C_{ox}\frac{W}{L}$ & $k_p = \mu_p C_{ox}\frac{W}{L}$.

Again, when $V_{IN} = V_{IH}$; the nMOS is in linear region and the pMOS is in saturation region. Similar analysis as done for V_{IL} produces the following equation for V_{IH}. For standard CMOS inverter operation $V_{OH} = V_{DD}$

$$V_{IH} = \frac{V_{DD} + V_{T,p} + k_R(2V_{OUT} + V_{T,n})}{1 + k_R} \quad (18)$$

& $V_{OL} = 0$. This analysis reveals that both V_{IH} and V_{IL} clearly depends on $V_{T,n}$ and $V_{T,p}$, threshold voltages of the nMOS and pMOS. Which results in the dependency of noise margin on transistor threshold voltage.

However, the transistor threshold voltage did not scale as fast as the supply voltage which left normalized headroom for analog operation [17]. As a result of this the application of conventional technologies (i.e., cascode) to amplify gain is getting increasingly harder [18]. Noise margin calculation for inverter reveals the possibility of high gain in the transition region. For $V_{in} = V_M$ the CMOS inverter gain around the switching threshold can be approximated using the following equation. [19]

$$g = \frac{1 + r}{\left(V_M - V_{Tn} - \frac{V_{DSATn}}{2}\right)(\lambda_n - \lambda_P)} \quad (19)$$

C. SRAM

The SRAM is a type of volatile memory unit which uses the concept of the bi-stable flip flop. 6T SRAM has two cross-coupled inverters with 4 transistors forming the storage cell and 2 transistors as access transistors. For proper operation, the pull-down to access transistor ratio should be kept above 1.28 and pull-up to access transistor ratio should not

be greater than 1.6 [20]. In this work, CNTFETs with two nanotubes are used as access transistors. In this work, p-type transistors having single nanotube are utilized as pull up transistors and n-type transistors having three tubes as channel are utilized as pull-down transistors resulting in pull-down to access transistor ratio = 1.5 and pull-up to access transistor ratio = 0.5. The channel length for both p-type and n-type CNTFETs used in our work is 32nm. Since the distance between two adjacent nanotubes is 20nm, the dimension of pull up transistors, pull-down transistors, and access transistors are 20/32nm, 60/32nm and 40/32nm respectively. In this work, the stability of an SRAM cell as a memory unit is measured by the merit of figure called N-curve.

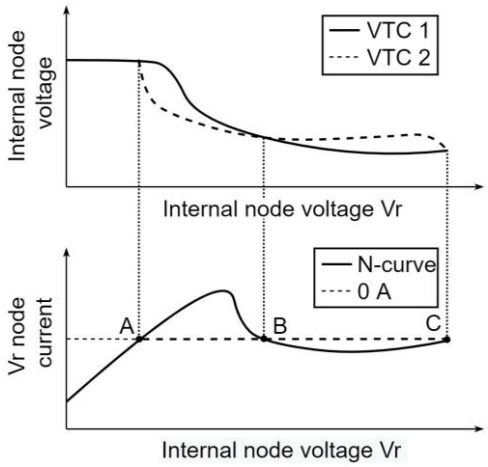

Fig 3: N-curve of an SRAM cell

A voltage sweep is performed in the internal node ‘q’. The current flowing into this node is plotted against the voltage to generate the N-curve. The linear correlation of N-curve with SNM was demonstrated by La Rosa *et al.* in 2006 [21]. N-curve allows a complete functional analysis of an SRAM cell with only one curve as it provides information on both read stability and write ability. The following are the four parameters studied by the N-curve.

1)-The Read Ability of SRAM: 'Static voltage noise margin (SVNM)' refers to the highest allowable DC voltage at the inverter input without altering the output. This is indicated by voltage difference between points A and B. The highest tolerable value for current is called 'static current noise margin (SINM)' and this is the maximum current between points A and B. It is important to note the supremacy of N-curve over SNM from the butterfly curve as two distinct SRAM cells might exhibit equal values for SNM and SVNM, but this should not imply that they are similarly stable. In this case, the one with improved SINM will provide a more stable performance [22]. Larger values of SVNM and SINM will indicate greater read stability.

2)-The Write Ability of SRAM: The maximum voltage needed on the bitline to flip the cell center is the ‘write-trip point’. The 'write trip voltage (WTV)' is measured while keeping both bitline high. This is the limiting value of the voltage drop required to alter the data in the cell. Minimum value of current between B and C while both BL and BLB is kept high is called 'write trip current (WTI)'. This is the margin of current to change the content of the cell. To ensure better write stability, the values of WTV and WTI should be large.

IV. RESULTS & DISCUSSIONS

A. Inverter Delay

In the case of any digital logic device power consumption and delay are two of the most important considerations. The average power consumed by a device is directly related to the supply voltage. Again, in MOS or MOS-like transistors propagation delay is often related to bias voltage. This simulation results

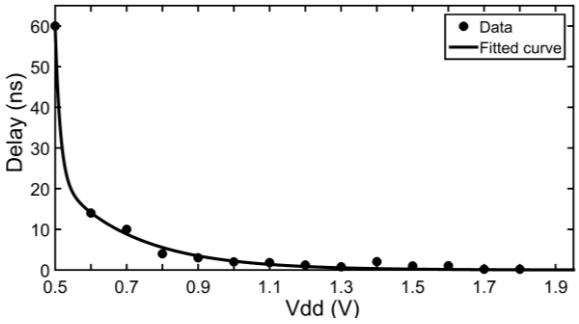

Fig 4: Propagation delay vs supply voltage

here show that the change of propagation delay of CNTFET inverter against the supply voltage. A voltage sweep was performed on a CNTFET inverter with 32nm channel length to reveal the inverse relationship between the delay and supply voltage. Analyzing the results with a curve fitting mechanism provides the following exponential relation.

$$f(x) = ae^{bx} + ce^{dx} \quad (20)$$

Co-efficients with 95% confidence bounds -

a = 5.611^{16} (-4.058^{19}, 4.07^{19})

b = -69.88 (-1519, 1379)

c = 230.2 (-69.26, 529.6)

d = -4.657 (-6.341, -2.973)

B. Inverter Noise Margin

As mentioned before, nMOS and pMOS carbon nanotube transistors have similar carrier mobility and that results in a symmetric design of the inverter. In this study both nMOS and pMOS devices have one CNT as channel and 32nm channel length. Another feature of a symmetric inverter is that the threshold voltage will always be exactly half of the supply voltage. Thus, both the high noise margin and the low

noise margin will be equal. Supply voltage of 0.9V for the inverter results in the threshold voltage, V_M to be at 0.45V. The simulation results summarized in the graph shows the noise margin against the CNT diameter. Simulations were performed using semiconducting armchair carbon nanotubes with various chirality to show the effect on inverter noise margin. It is evident from the results that the diameter of CNTs has an inverse relationship with the noise margin. The chiral vector of CNT has a linear relation

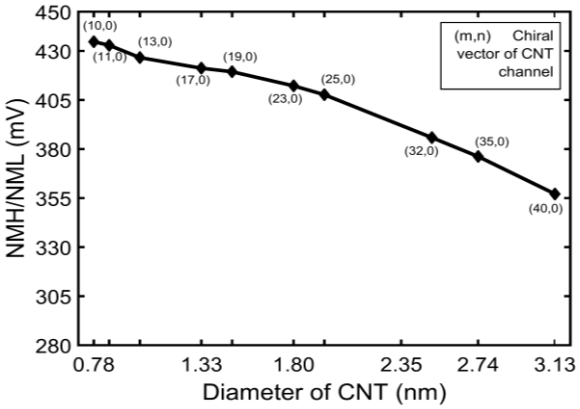

Fig 5: Inverter noise margin as a function of CNT diameter

with D_{CNT} and a higher value of chiral vector (m, n) results in a larger diameter. Again, D_{CNT} is inversely related to nMOS and pMOS threshold voltage according to equation no. 4. It is apparent from the equation (17) and (18) that lower values of $V_{T,n}$, and $V_{T,p}$ causes smaller values of V_{IL} and V_{IH} which results in lower noise margin. An inverter designed with carbon nanotube (10, 0) of 0.783nm diameter has a 21% higher noise margin than the inverter designed with carbon nanotube (40, 0) of 3.132nm diameter.

C. Inverter Gain

Apart from the uses in digital circuit, an inverter also has analog application since it has considerably large value of gain in the switching region of VTC curve. This simulation result shows the gain taken as dV_{out}/dV_{in} of the CNTFET inverter which has a very high value in the transition region. This inverter shows maximum gain in V_M (0.45V).

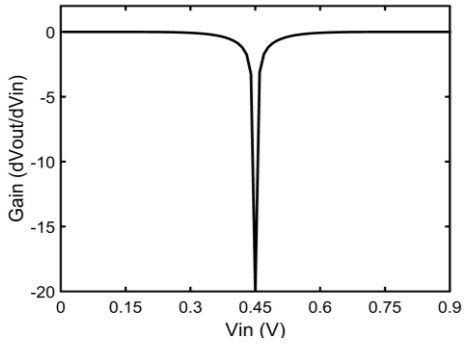

Fig 6: Voltage gain of CNTFET inverter

D. SRAM

In this study, we used N-curve to measure the stability of a 6T conventional SRAM cell. Standard 6T SRAM cells were designed with different chiral vector (m, n) CNTs. The parameters derived from N-curve were plotted against the chiral vectors of channel CNTs to analyze the impact CNT diameter**.** Read stability of an SRAM cell is appropriately analyzed by using both SVNM and SINM. A small SVNM with a large SINM will result in a somewhat stable cell as the magnitude of noise required to hamper the cell stability is generally large. The simulation results show that SVNM decreases with increasing diameter of CNT. Though higher chiral vector results in lower SVNM, SINM of cells with (17,0), (19,0), (23,0), (25,0) chiral

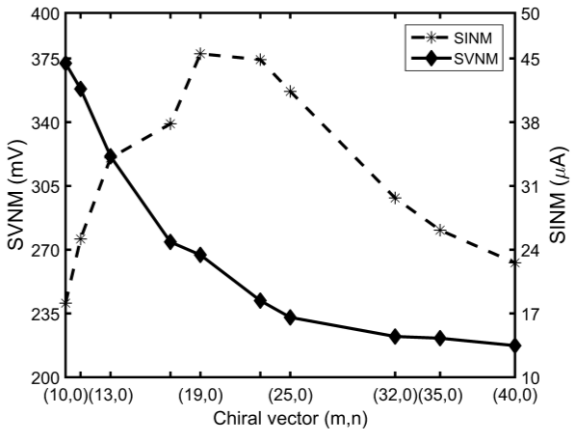

Fig 7: SVNM and SINM of 6T SRAM vs chiral vector of CNT

vector nanotubes have a higher value. Read stability metric, SPNM is defined as the product of mean value of SVNM and mean value of SINM. For good stability of SRAM cell SPNM should be large. The highest value of SPNM was 12.16μW and it was found in the cell with (19,0) CNT. The write ability of a SRAM cell also relies on both current and voltage. For better write ability WTV and WTI metrics should have low value. Simulation results shows that larger diameter causes WTV to increase at first but cells with higher than (25, 0) CNTs do not have much effect of diameter on WTV.

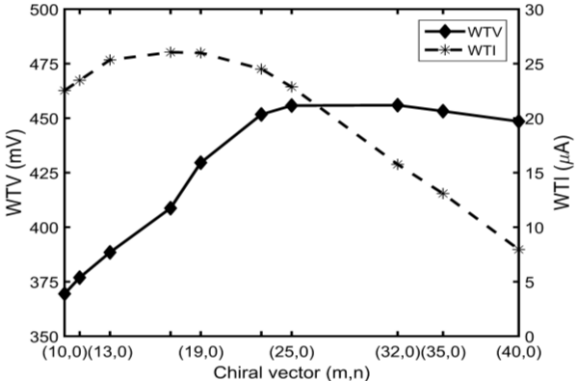

Fig 8: WTV and WTI of 6T SRAM vs chiral vector

On the other hand, smaller diameter does not show much impact on WTI but large CNT diameter causes WTI to fall rapidly. Write ability depends on WTP which is defined as the product of mean value of WTV and mean absolute value of WTI. WTP should be low to ensure good performance form a SRAM cell. The lowest value found in this study was 1.8 µW and it was found for cell with (10, 0) chirality nanotube. As maximum SPNM and minimum WTP does not happen for same chirality of channel CNT, an optimum choice should be made for efficient SRAM cell design.

V. CONCLUSION

This study shows that the chiral property of channel CNT has a considerable impact on the robustness of the device. The noise margin of the device can be improved by using a higher chiral vector CNT. Using semiconducting zigzag CNTs from (10,0) to (40,0) chirality, 21% improvement in noise margin was found. This work has found an exponential relationship between the bias voltage and the propagation delay of the inverter. Simulation data also shows a considerable gain of the CNTFET inverter for analog applications. We also investigated the N-curve of a CNTFET-based 6T SRAM. Simulation results of four N-curve parameters show that the highest read stability and write ability do not happen for the same chiral property. Best read ability was found with (19,0) CNT and best case write ability occur for (25,0) CNT.

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