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Original Article

5-Level Dual Output Active Buck PFC HPUC Rectifier

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Abstract *- This work introduces a novel topology of active buck power factor corrector rectifier operating in continuous conduction mode and producing a voltage wave with multiple levels across the rectifier. The offered redesigned packed U-cell rectifier structure eliminates the grid side capacitor and load side inductor for filtering due to CCM operation. The suggested rectifier provides two separate outputs that can link two specific loads at various switching options. The two output ports are helpful to have a 5-level voltage wave shape across the contacts of the rectifier. The voltage harmonics are reduced when different voltage levels are produced, directly influencing the grid current harmonic contents. The suggested rectifier's low switching frequency distinguishes it from further buck converters that considerably reduce switching losses and excessive switching frequency-related concerns. From an AC supply perspective, the rectifier boosts the voltage, but the output DC voltage can be divided into two parts, leading to the functioning in buck mode. The MATLAB Simulink outcomes are given and examined to validate the suggested five-level buck rectifier's effective operation and good dynamic performance.*

Keywords — *Buck rectifier, CCM, Multi-level converter, PFC operation, Phase-locked loop, THD.*

I. INTRODUCTION

Active rectifiers are being developed through developing power semiconductors. As a result of enhanced power quality, it made its way into the power electronics sector. Low THD (Total Harmonic Distortion) in AC source voltage and current with a unity power factor is acquired by governing the DC voltage having low ripple content using PWM AC to DC converters or PFC (Power Factor Correction) converters which can modulate the AC supply. By controlling the switching of active switches at specified intervals, the current can be converted into a suitable sinusoidal waveform to have low THD. PFC boost type converters create a larger DC voltage than the maximum AC grid voltage. On the other side, buck-type converters can step down the DC voltage to a value less than the maximum grid voltage. Boost-type power factor corrector converters are enticing converters for high-power applications. Whereas the buck convertors are ideal prospects for chargers of batteries, specifically designed for uninterrupted power supplies (UPS), electric automobiles, supplying telecommunication boards, and application in various electronic devices.

Buck converters currently in use have a low output voltage to AC input voltage ratio, prompting the use of bulky LC filters on both the grid and output sides of the converter. The PFC buck rectifier's discontinuous conduction mode (DCM) makes creating the output voltage more complex. Similarly, the output voltage of the boost converter should be sufficiently more significant than the maximum value of supply voltage to reduce source side harmonics and receive the AC source current with a unity power factor. To achieve satisfactory results, large input inductive and capacitive output filters are also required. In addition to the disadvantages of conventional buck and boost type converters already highlighted, both have large switching frequencies capable of causing EMI (electromagnetic interference). Some rectifiers have a two-stage arrangement, with a diode bridge in the first stage to produce DC voltage from the AC supply and the next phase as a chopper to buck or boost the output DC voltage. These multi-stage converters feature fewer semiconductor switches but work at a greater switching frequency compared to one-stage PFC converters that result in consuming more power from the supply.

This work introduces an innovative multilevel converter that can solve most of the concerns stated above. The suggested Hani Packed U-cell (HPUC) multilevel converter works in boost operation. By dividing the DC voltage, yield more than one output with lower power consumption. The HPUC converter topology is the structural modification of the Packed U-Cell (PUC) topology. When more than one output terminal is supplied, a several-level wave shape of voltage is achieved across the rectifier, which minimizes the harmonic distortion from the AC side without using massive inductive filters. A large inductor at the DC side to regulate the output voltage is prevented by operating the convertor in boost mode. The continuous conduction mode operation (CCM) of the HPUC rectifier makes it easy to regulate and maintain DC voltage output.

II. PROPOSED MULTILEVEL MULTI-OUTPUT PFC ACTIVE BUCK RECTIFIER

The 5-level active buck HPUC configuration of the rectifier is represented in Fig. 1. It consists of 6 IGBTs with an antiparallel diode. The DC output voltage is taken from the two output terminals across the capacitors. V_1 and V_2 are the two output voltages across the load resistances $Load_1$ and $Load_2$? The output voltages V_1 and V_2 should be equivalent and equal to the reference voltage, 125 V, to get a 5-level voltage across the rectifier input as V_{ps}. The switching of the 6 IGBTs of the HPUC rectifier is mentioned in Table I.

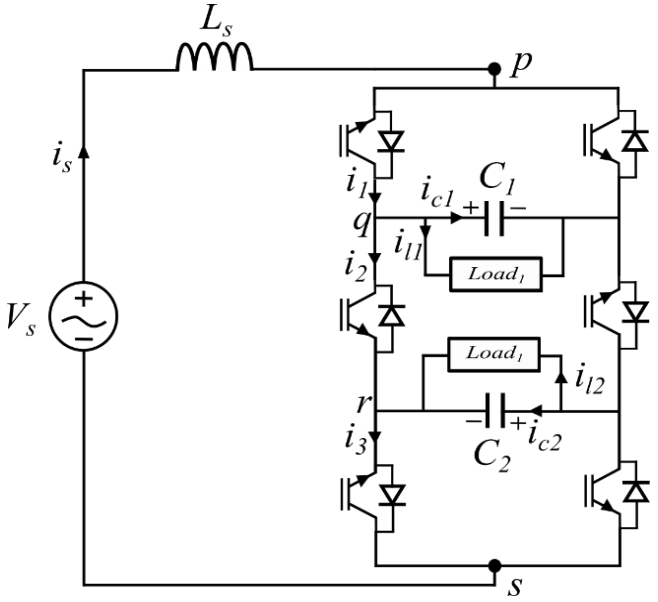


Fig. 1 5-level active buck PFC HPUC rectifier

According to the switching table, Switches S_1, S_2, S_3 will be ON when switches S_4, S_5, S_6 are off, respectively, and vice versa. The voltage level in switching states 2 and 3 or 6 and 7 is the same. A repetitive or recurrent switching state is a name for these types of switching states. Based on both capacitors' charging and discharging, which depends on the current flow direction, one of the states must be chosen. Across the rectifier, 5 voltage levels as 0, $+125$, -125, $+250$, and -250 are to be created.

Table 1. Switching states for HPUC rectifier

Switching States	i_s	S_1	S_2	S_3	S_4	S_5	S_6	V_{ps}
1	> 0	1	0	1	0	1	0	$+2E$
2	> 0	1	0	0	0	1	1	$+E$
3	> 0	0	0	1	1	1	0	$+E$
4	≥ 0	1	1	1	0	0	0	0
5	< 0	0	0	0	1	1	1	0
6	< 0	1	1	0	0	0	1	$-E$
7	< 0	0	1	1	1	0	0	$-E$
8	< 0	0	1	0	1	0	1	$-2E$

Repetitive switching states play a crucial role in maintaining these voltage levels. If the voltage across the load resistance R_1 is lower than the voltage across the load resistance R_2, the capacitor C_1 should be charged to bring both loads' voltages up to the reference voltage level. As a result, switching state 2 is chosen above switching state 3. For the recurrent switching states 6 and 7, the same method has been used. As previously stated, this rectifier is a boost converter from a supply-side perspective since the cumulative voltage at the converter contacts (V_{ps}) is always equals or greater than the maximum voltage of the supply. Distributing DC voltage into two output ports provides each load half of the total voltage magnitude. Ascertaining that their magnitudes are always less than or equal to the maximum voltage of the supply makes it the buck mode converter from the loading perspective. It could be inferred that the converter deceives the grid by using two output terminals.

III. MODELLING AND CONTROLLER DESIGN

Based on figure 1, a comprehensive model of the proposed HPUC rectifier is developed. The following are the switching functions:

$$S_n = \begin{cases} 0 \ if \ S_n \ is \ on \\ 1 \ if \ S_n \ is \ off \end{cases} \qquad \text{n = 1, 2, 3}$$

The voltage across the rectifier can be derived as follows:

$$V_{ps} = V_{pq} + V_{qr} + V_{rs}$$

Figure 1 depicts the points p, q, r, and s. Each of the above voltages can be evaluated using the following functions:

$$V_{pq} = (S_1 - 1)V_1$$

$$V_{qr} = (1 - S_2)(V_1 + V_2)$$

$$V_{rs} = (S_3 - 1)V_2$$

The following equation expresses the voltage across the interface inductor:

$$L_s \frac{di_s}{dt} = V_s - V_{ps}$$

$$\frac{di_s}{dt} = \frac{1}{L_s}[V_s + (S_2 - S_1)V_1 + (S_2 - S_3)V_2] \qquad (1)$$

The equation of switch current is expressed in terms of load current and switching function as one of the switches is ON from the pair of switches in a cell.

$$\begin{cases} i_1 = S_1 i_s \\ i_2 = S_2 i_s \\ i_3 = S_3 i_s \end{cases}$$

The currents that flow through the capacitors can be described in the following way:

$$i_{c1} = i_1 - i_2 - i_{l1}$$

$$\frac{dV_1}{dt} = \frac{(S_1 - S_2)i_s}{C_1} - \frac{V_1}{C_1 R_1} \quad (2)$$

$$i_{c2} = i_3 - i_2 - i_{l2}$$

$$\frac{dV_2}{dt} = \frac{(S_3 - S_2)i_s}{C_2} - \frac{V_2}{C_2 R_2} \quad (3)$$

The optimum configuration of suggested rectifiers is provided by equations (1), (2), and (3). A cascaded PI controller has been constructed using these equations to regulate the output terminal voltages V_1 and V_2 and synchronize the AC source current with source voltage to obtain a unity power factor. The implemented control scheme includes two controllers, as demonstrated in figure 2. The current controller and voltage controller are designed using the above state variables consisting of source current and capacitor voltages.

The phase-locked loop (PLL) evaluates the phase angle of the source voltage. A unit magnitude co-phasor is obtained by generating a sinusoidal reference wave from this angle. The total DC voltage is constantly evaluated and matched with the maximum reference level. The current drawn by the converter with power factor correction is calculated by multiplying the regulated signal generated by the PI controller with the unit magnitude signal in synchronism with the AC grid voltage.

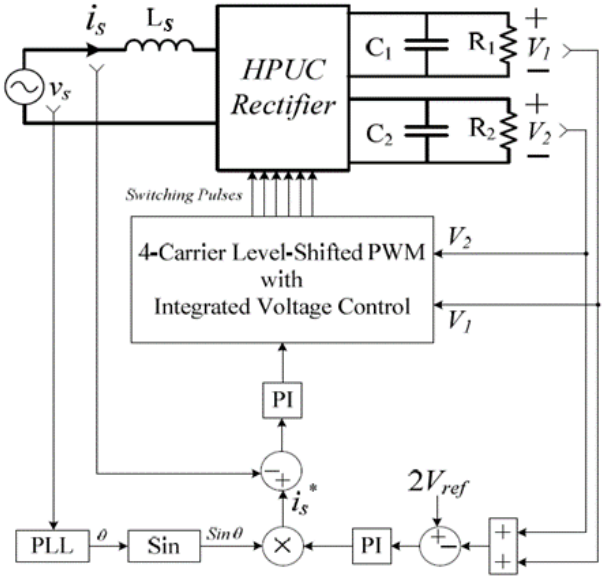


Fig. 2 Block diagram and implemented controller of buck PFC HPUC rectifier

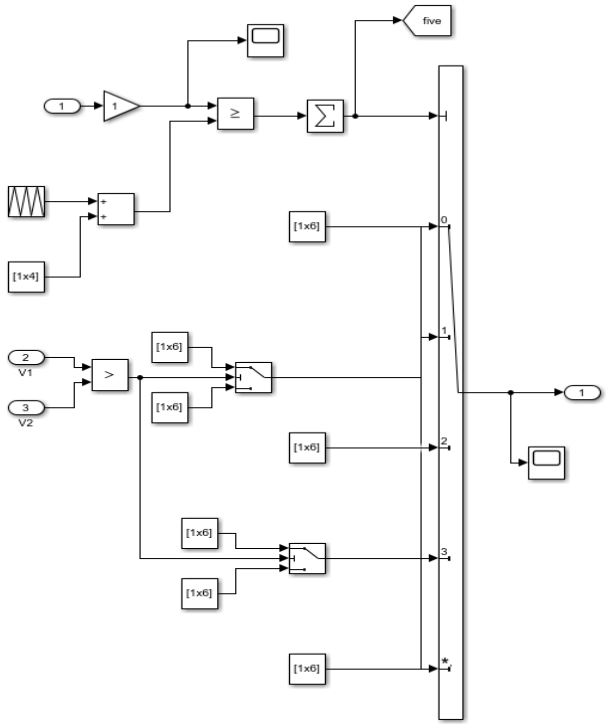


Fig. 3 Technique for voltage balancing with integrated switching

As represented in Fig. 3, the switching states are realized in the voltage balancing mechanism. The magnitudes of the individual output voltages are equivalent to the 125 V reference level. It indicates that the controller is balancing and regulating the voltages at the output terminals. To maintain the dual output voltage, charge and discharge operations of the capacitors are controlled using a switching approach and repetitive switching states. Even in malfunctioning circumstances where switching actions cannot balance capacitor voltages, this detached voltage control aids in balancing capacitor voltages. Individual terminal voltages cannot be regulated in this instance, but the total voltage can be regulated to the reference voltage level. This guarantees that capacitors are not charged to an excessive level.

IV. MATLAB SIMULATION AND ANALYZING RESULTS

The proposed HPUC rectifier is simulated in MATLAB to verify CCM operation, 5-level waveform generation, power factor correction operation, generating dual output voltage, and dynamic performance in regulating the dual output voltage. Table II lists the details of the simulation parameters.

Table 2. Parameters of the simulated system

Source Voltage	120 V
Source Frequency	50 Hz
Interfacing Inductor	2 mH
Output Voltages (V_1 & V_2)	125 V
Capacitors (C_1 & C_2)	2500 μF
DC Load (R_1)	43, 15, 8 Ω
DC Load (R_2)	43 Ω
Switching Frequency	2 kHz
Sampling Time	10 μS
Current PI Controller	$k_p = 0.8, k_i = 0.1$
Voltage PI Controller	$k_p = 0.01, k_i = 5$

When the converter converts the maximum AC voltage of 170 V into 125 V at the two terminals, steady-state results are obtained. The load resistances are maintained at 43 Ω. Figure 4 shows all of the data in steady condition, covering load voltages and currents, supply AC voltage and current, and rectifier input voltage. Fig. 4(a) shows buck mode functioning of the converter with DC load voltages controlled at 125 V with little voltage ripples. Fig. 4(b) shows output current waveforms that are proportional to output voltages and load resistances.

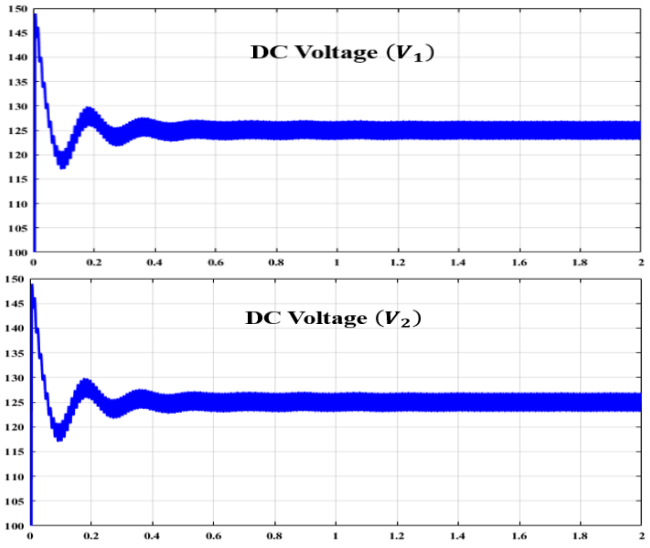
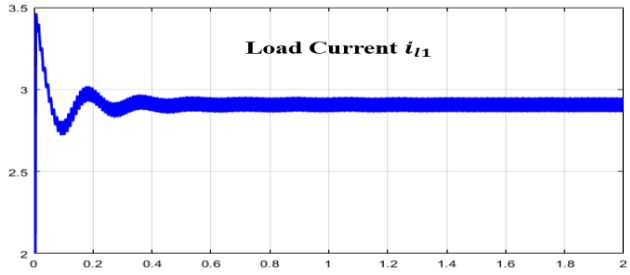


Fig. 4(a) DC output voltages at steady state



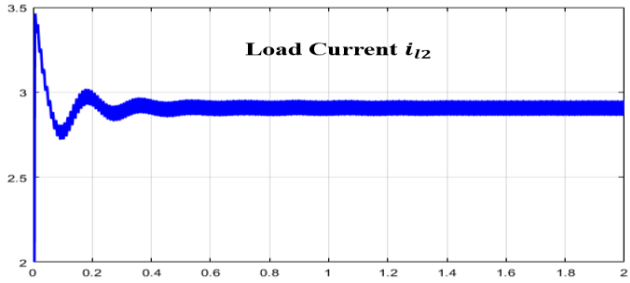


Fig. 4(b) Load currents at steady state

Fig. 4(c) depicts a 5-level voltage wave shape across the converter contacts, with levels of 0, ±125, and ±250. The highest voltage level is 250 V, which is more than the 170 V peak AC voltage. As a result, the entire system is in boost mode. As a buck mode of operation, it is split into two outputs and operates at halved voltage. Low power losses are achieved by keeping the switching frequency at 2 kHz.

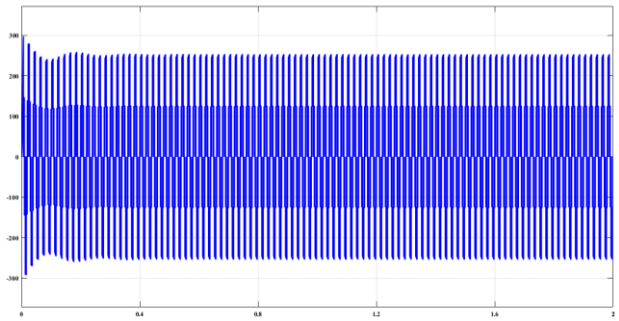


Fig. 4(c) 5-level voltage waveform at rectifier input

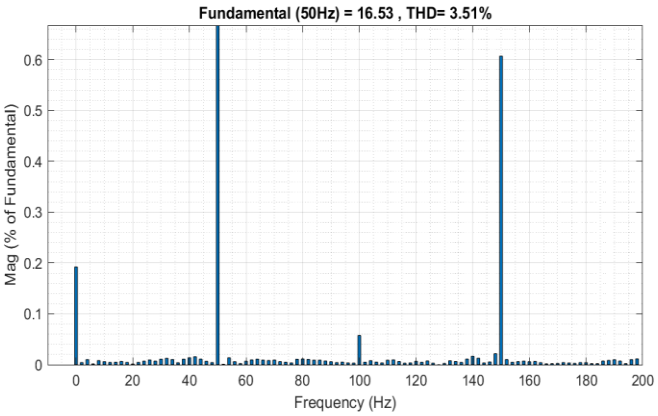


Fig. 4(d) FFT analysis of AC source current

Furthermore, Figure 4-d displays the grid current FFT analysis. The supply current has a maximum value of 16.53 A and an RMS value of 11.69 A checked at 2.5 sec. Where $R_1 \neq R_2$. When 25 cycles and 200Hz maximum frequency are evaluated, total harmonic distortion (THD) is 3.51%, about the fundamental frequency of 50 Hz. The active power consumed by the load is 1411 W, and the power factor is

almost 1, ensuring that the mentioned multilevel active buck rectifier with voltage and current controllers operate as a PFC rectifier.

To follow, load resistance and supply voltage are varied independently to test the dynamic behavior of the voltage modulator incorporated into switching orders and current controller in operating the suggested multilevel PFC converter to feed DC loads with maintaining unity power factor at AC grid. Initially, $load_1$ resistance is modified on purpose. The DC output voltages (V_1, V_2)And load current (i_{l2}) remain unchanged, as shown in Fig. 5; however, the load current (i_{l1}) Shows a significant variation.

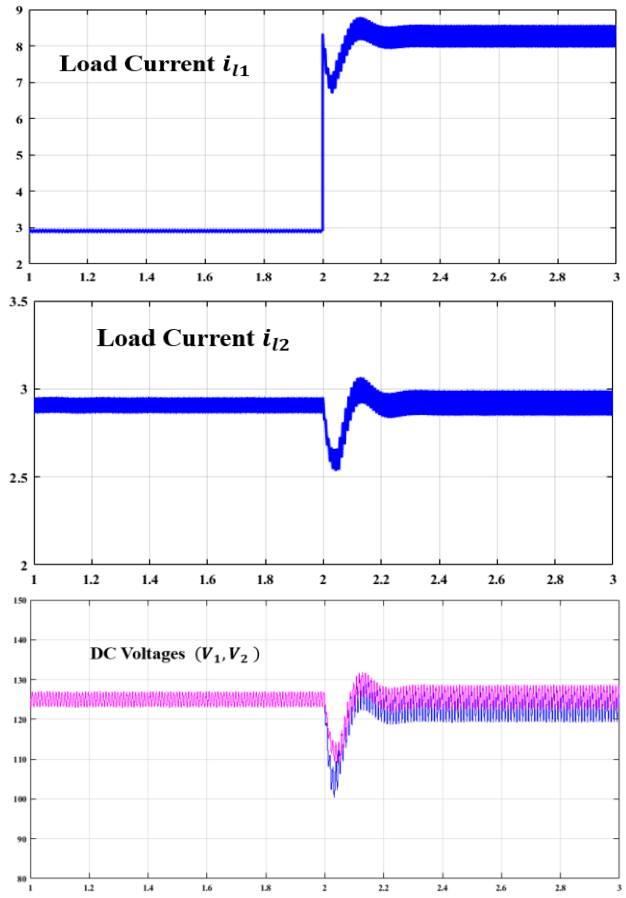


Fig. 5 Simulation results during a change in $Load_1$ from 43Ω to 15Ω

Secondly, a test is performed to confirm the suggested rectifier's good dynamic behavior under an unstable supply condition. The AC supply voltage has been increased by 25%, from 120 V RMS to 150 V RMS. There is no variation in output voltages from 125 V after analyzing the results.

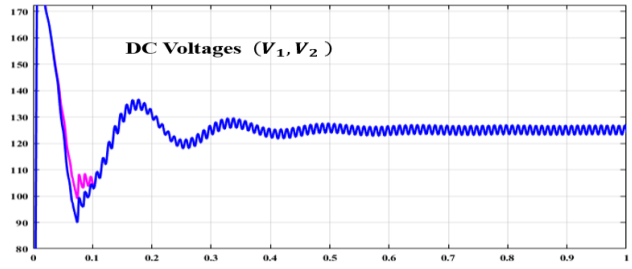


Fig. 6 DC output voltage while supply voltage increased to 150 V RMS

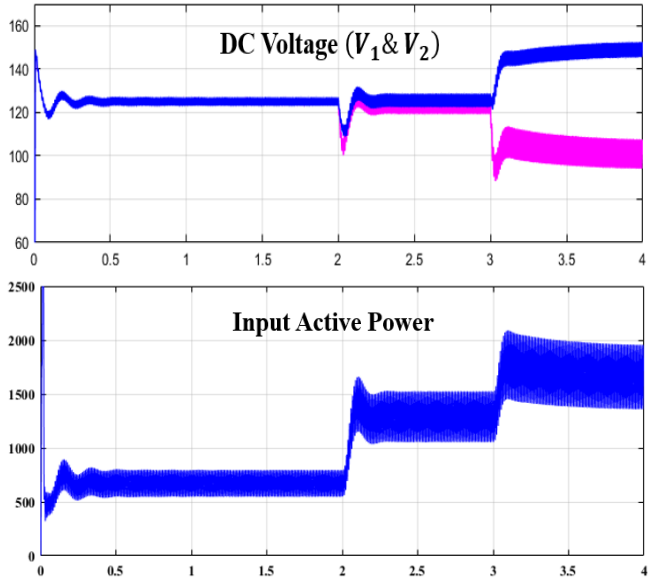


Fig. 7 Simulation results during a change in $Load_1$ resistance leading to a power imbalance

Finally, the $load_1$ resistance is lowered to 8 Ω, forcing the converter to enter a state of instability. The loads require 1808W of power at 4^{th} sec when $R_1 = 8\,\Omega$ and $R_2 = 43\,\Omega$, as shown in Figure 7. The loads will not receive this extra power from the rectifier. The voltage dropped unnecessarily as a result of the increased current demand. As a result of the PI controller's action, the load2 voltage rises unnecessarily to keep the cumulative voltage at a reference voltage level. As a result, the two output voltages cannot be kept constant, causing the rectifier to become unstable.

The results demonstrate that the mentioned HPUC bridge free 5-level active buck power factor corrector converter has satisfying dynamic performance in producing DC power from the AC supply under varying situations. It can be inferred that the HPUC configuration may be used as a unified PFC converter in the buck mode at lower switching frequencies, resulting in improved efficiency and makes it suitable for industrial applications.

V. CONCLUSION

Based on the structural adjustment in the PUC inverter topology, a novel topology of multilevel rectifier (HPUC rectifier) has been developed in this study. The suggested rectifier has been demonstrated to generate 250V DC voltage from a 170V peak AC supply in boost operation while breaking the output voltages to 125V in buck mode. Overall boost and continuous mode operation are beneficial in removing excessive filter requirements. The presence of a 5-level voltage at the rectifier contacts reduces the harmonic distortion of the supply. Low switching frequency reduces power losses and improves efficiency. It requires more semiconductor switches than other buck converters and some restrictions on load power balance. Meanwhile, the integrated controller and HPUC rectifier topology were demonstrated and reviewed in-depth for their excellent dynamic performance, quick reaction, and stable operation.

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