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Original Article

Design and Analysis of Improved Raptor Encoder-based Hybrid Recursive Systematic Convolutional Encoding Technique for 6G Networks

Dasari Ramanna[1], Ganesan V[2]

[1] *Department of ECE, Sathyabama Institute of Science and Technology, Chennai, India.*
[2] *Department, of ECE, Bharath Institute of Higher Education and Research, Chennai, India.*

[2] *corresponding.author: ganesan.ece@bharathuniv.ac.in*

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Abstract *- In modern years, 6G is the upcoming technology suitable for many applications such as autonomous vehicles, augmented and virtual reality, virtual video conferences, holographic beamforming, cell-free communication, unmanned aerial communication, and quantum communication. The 6G application represented required large bandwidth, high data rate, throughput, increased network capacity, and low latency may be obtained by employing Non-Orthogonal Multiple Access techniques (NOMA). It will be obtained by choosing the appropriate error correction encoding and decoding method. So, we proposed an improved raptor encoder-based hybrid Recursive and Non-Recursive Systematic Convolutional Encoding techniques for 6G networks. Here, the raptor encoder method initially consists of a serial connection of polar code and Low-Density Parity Check (LDPC). The LDPC encoded data are multiplexed with the original bit to produce the raptor code word. The raptor code word is fed as input to Recursive Systematic Convolutional (RSC) Encoder technique, which results in fewer code words with lesser weight and better error performance. The proposed encoding process also connects the raptor code and RSC code in parallel form to produce the turbo code. Here, different types of interleaver are designed and connected parallel with Raptor and RSC code to reduce the data bit error rate and achieve a larger channel capacity. Finally, the proposed raptor and RSC-based hybrid encoding process was implemented using different FPGAs such as Vertex 4, Vertex 5 and Vertex 6 and obtained better power, latency, Number of LUTs, product area, time delay, throughput, PSNR and code gain. From the simulation results, it is inferred that the proposed hybrid encoder technique obtained greater throughput and a lesser Bit Error Rate.*

Keywords *- Raptor Code, Polar Code, Low-Density Parity Check, Recursive Systematic Convolutional Encoder, Non-Orthogonal Multiple Access, 6G Networks, Turbo Code, Interleaver.*

1. Introduction

6G communication is the upcoming generation of cellular mobile communication that can connect numerous devices with low latency. Many researchers are putting their effort into developing a more suitable encoder /decoder, modulator/demodulator, channel encoding or decoding method and noiseless channel model. It will be achieved by employing Non-Orthogonal Frequency Division Multiple Access techniques instead of using regular time and frequency-based multiple access techniques. There are numerous channel coding schemes are already available to deliver a higher data rate, a vast amount of data and a lesser Bit Error Rate, such as polar code, turbo code, and LDPC code, but these codes have longer code words [20][21][22][23][24][25]. However, low latency, high reliability, and larger bandwidth are the necessary requirements for the upcoming 6G technologies. It will be achieved by interoperating error correction coding techniques and broadly classified into two types: Block Code and Convolutional Code. In the block coding method, original data bits of size k bits are encoded as n bits by adding the redundant bit of size t bits; as a result, (n, k) bits as the output symbol. Polar code is designed based on the polarization of the channel to offer the proper channel capacity.

On the other hand, convolutional coding involves the linear phase shift register to generate the code word from the message bits. It will be improved by cascading the two encoders and increasing the enactment of the system in terms of BER and throughput by connecting the two encoders in serial and parallel form. Also, instead of orthogonal multiple access techniques, non-orthogonal multiple access techniques have played a vital role in the future 6G technology by allowing multiple users to access the channel bandwidth using the same time or frequency in both the power field and code field[16][17][18][19]. This paper focuses on the design and analysis of relevant error correction codes for a 6G communication system which will give a higher data rate, low latency and allocate more users. In this connection, we proposed a structure consisting of two error correction codes, a raptor code and a recursive systematic convolutional code connected in a serial and parallel mode appropriate for 6G networks. The raptor code comprises inner LDPC code and outer LT code; the resultant output symbol is fed as input to the RSC code to generate the code word.

This paper is organized as follows: the current section introduces orthogonal multiple access and non-orthogonal access along with popular coding techniques such as polar code, convolutional code, turbo code and systematic recursive code. Section 2 shows the related works. Section 3 demonstrates the proposed encoding method for 6G communication. Section 4 exemplifies the simulation results and their discussion. Finally, finalizes the paper with future work.

2. Related Work

A. K. Ahmed [1] introduced Non-orthogonal Multiple Access (NOMA) in a 6G network to sustain better characteristics such as higher data rates, high throughput, and lesser latency. Here, polar codes are connected serially with convolutional code to obtain a 1.5 dB coding gain increase compared with 5G communication. With higher system settings, this performance range varied from 4 to 6.25dB. In mohsen et al. [2], MIMO and Rate Less Digital Fountain Codes design the channel condition for 6G networks by adding the flexible, adaptive interleaved pre-coding process. A novel raptor coding process is introduced along with convolutional code and the chaotic interleaver method.

Ping Zhang et al. [3] proposed the unique 6G architecture to increase the network capacity by merging the networking with the artificial intelligence concept. It also improves hyper-connectivity, reduces bandwidth usage and intelligent connection, and reduces redundant bits and noiseless data transmission. Asha Devi Dharmavaram et al. [6] investigated the low latency reliable 6G communication system by using polar and turbo code and proved that it provides better system performance in terms Signal to Noise Ratio and network capacity. So far, polar codes have been intended to be SNR dependant. In the paper [7], the author examines the enactment of upgraded turbo codes with the help of a decoding list and CRC-supported polar codes.

Yunkai Hu et al. [8] explored techniques in which the original information is transmitted using LDPC code and RIS-supported transmitter device. Monte Carlo simulation is used to cross-validate the research work and proves that bit error probability will be reduced by employing the RIS-assisted transmitter device in a 6G network. Suhas S. Kowshik et al. [26] proposed a suitable framework for finite block length and examined the difficulty of designing the channel condition with low latency and fast computation. This framework uses the random access code for the Rayleigh fading scenario. Vijay Nagarajan et al. [10] & others [11][12][13][14][15] present an efficient, fully parallel implementation of structured LDPC decoders utilizing the Network of Programmable Logic Arrays (NPLA). Standard cell-based design diminishes the routing congestion and provides the circuits with predictable operating power, delay, and chip size.

3. Proposed Encoder and Decorder Technique for 6G Communication System

In order to over the limitation, a hybrid Raptor and RSC encoder was designed and proposed for the 6G network, as shown in Figure 2. Initially, raptor code diminishes interference and safeguards transmitted video signals. Raptor code is a rateless error control method for 6G communication to improve reliability and enhance the system's efficiency.

3.1. Raptor Encoding Process

The raptor encoder comprises two error control methods: Low-Density Parity Check (LDPC) as precoder and outer encoder as LT coding process. The original input data is considered the source symbol encoded by LDPC pre-encoder method to produce input symbol bits. The resultant input symbol bit is encoded by the outer encoder method, such as the LT coding process, as shown in Fig. 1.

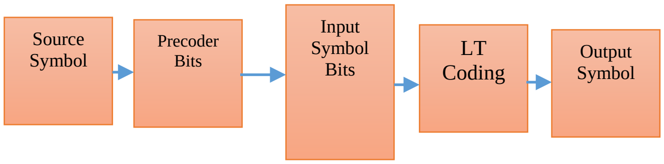

Fig. 1 Raptor coding process

In the second part, message bits are encoded by using the raptor encoding process and the output of the raptor code is given as input to Recursive Systematic Convolutional (RSC) encoder [11] in the form of the cascade as shown in Figure 2. The encoded bit is treated separately as modulating bit for BPSK and QAM modulation process. The trusted channel is used to transmit the modulated waveform, and RSC and raptor decoder method is used on the receiver side. Figure 5 shows the parallel connection between the raptor encoder and the RSC encoder. The raptor and RSC encoder output symbol bits are multiplexed to produce the code word for 6G communication. Figure 3 also shows the parallel connection of both encoders, but an interleaver is introduced between the RSC encoder and the raptor encoder to reduce the error burst. The interleaver's primary responsibility is to ensure that the input sequences are generated in a random order, and it also works to increase the significance of the code words. The improved hybrid Recursive structure In addition to the systematic code, the high-weight code (y1) and the low-weight code (y2) are both outputs of the systematic convolutional encoder (y3). In this case, interleaving prevents the second raptor encoder from producing the low-weight recursive output sequence. As a substitute, it generates high-weighted code to progress the BER enactment of the system. The efficiency of the Raptor code is improved because of the interleaver block, which has a direct impact on the distance attributes of the code, as shown in Figure 4.

3.2. Recursive Systematic Convolutional Encoder

The Recursive Systematic Convolution (RSC) Encoder is seen in Fig. 3, and its construction involves the utilisation of two adders in conjunction with D-Flipflops to achieve a lower Bit Error Rate (BER). It is built on top of the non-recursive systematic convolutional encoder by using the output of one flip-flop as an input to the next flip-flop.

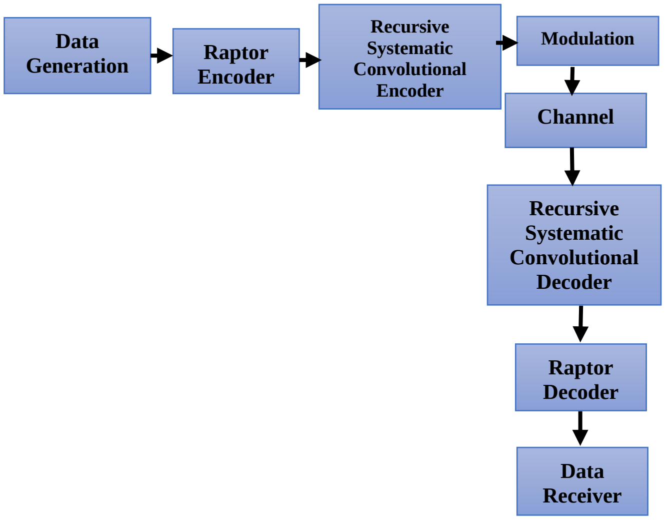

Fig. 2 Serial connection process

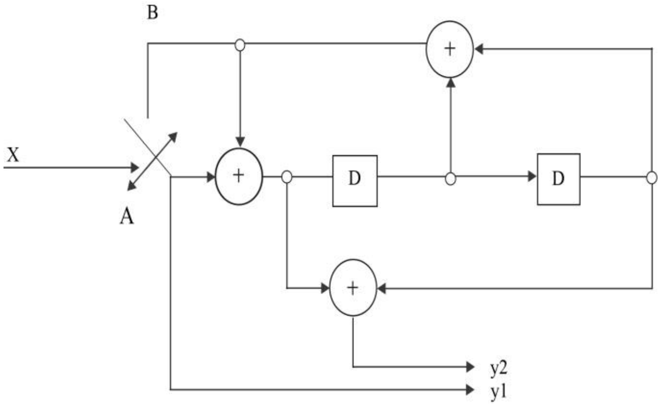

Fig. 3 Recursive systematic convolution (RSC) encoder

4. Result and Discussion

The proposed hybrid raptor and RSC-based encoding method were implemented using various FPGA devices such as Vertex 4, Vertex 5 and Vertex 7. Analyses of the various simulation parameters, such as the number of LUTs and slices, power consumption, processing time, throughput, bit error rate, and signal-to-noise ratio, are demonstrated and evaluated the performance of the proposed hybrid encoder techniques in comparison to the performance of the encoder techniques that already exist.

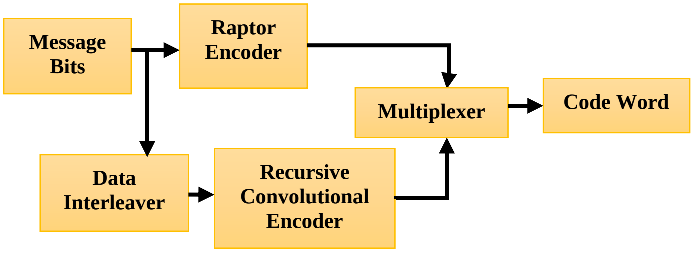

Fig. 4 Parallel connection process –Interleaved

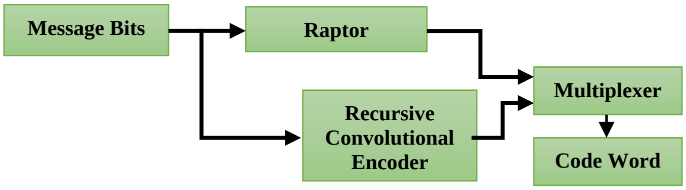

Fig. 5 Parallel connection Process

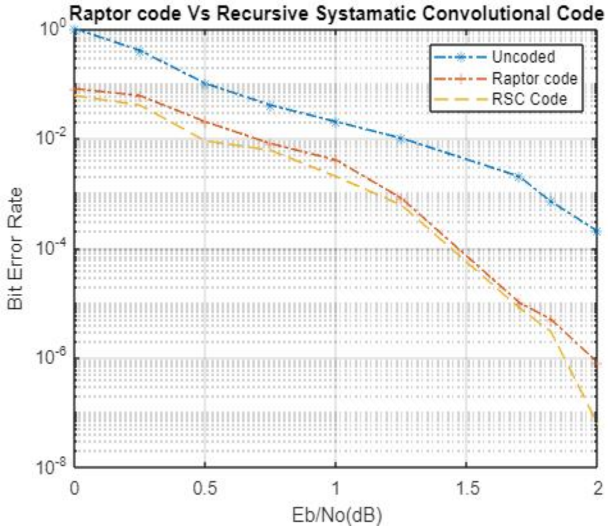

Fig. 6 Comparison of Raptor and RSC Encoder

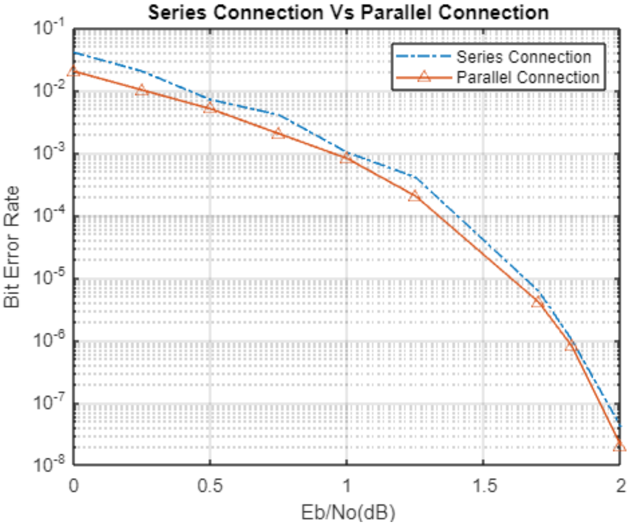

Fig. 7 Comparison of Series and Parallel Connection of Raptor and RSC Encoder

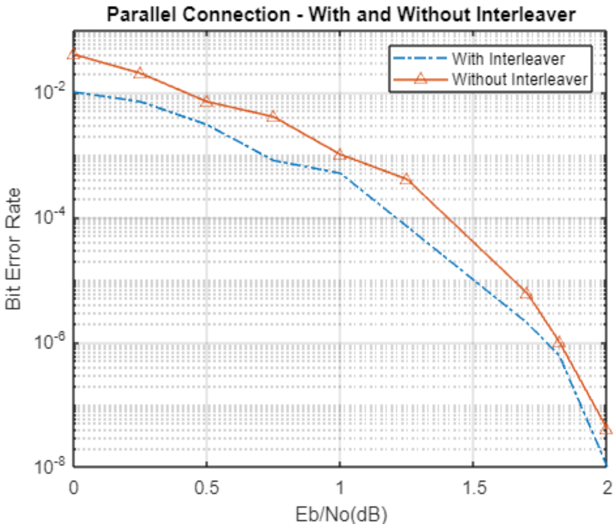

Fig. 8 Comparison of Parallel Connection –Interleaver

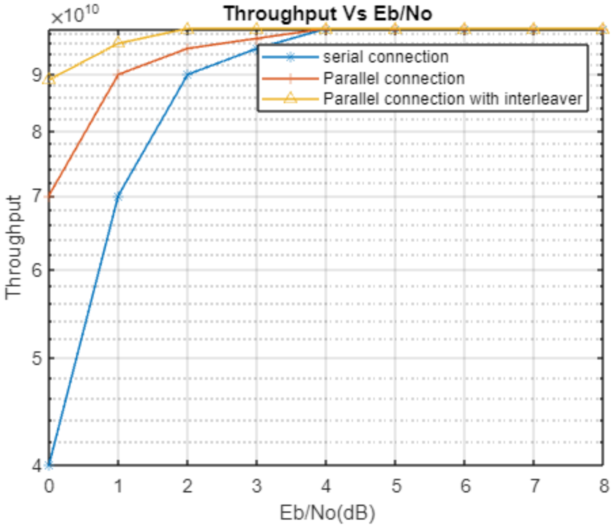

Fig. 9 Comparison of Throughput Vs Eb/No

Fig. 6, 7, & 8 shows the performance analysis of the proposed encoder architecture in terms of Bit Error Rate and Signal Noise Power. The simulation results show that the interleaved-parallel connection of raptor code and recursive systematic convolutional code achieves better BER value than the serial and parallel connection of two error correction codes.

The above Fig. 9 shows the comparison results of all three types of connection in terms of throughput and signal-to-noise ratio. Interleaved parallel connection achieves higher throughput of 8.9 x 10^{10} bits/sec compared with another type of connection.

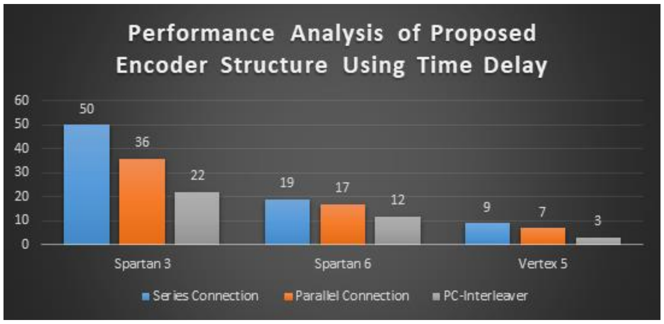

Fig. 10 Enactment analysis of projected Encoder structure using Time Delay

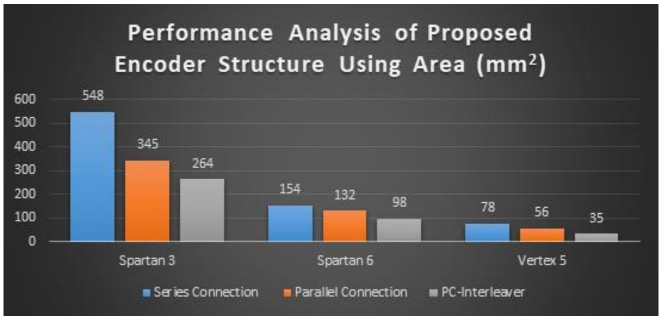

Fig. 11 Enactment analysis of projected encoder structure using area (mm2)

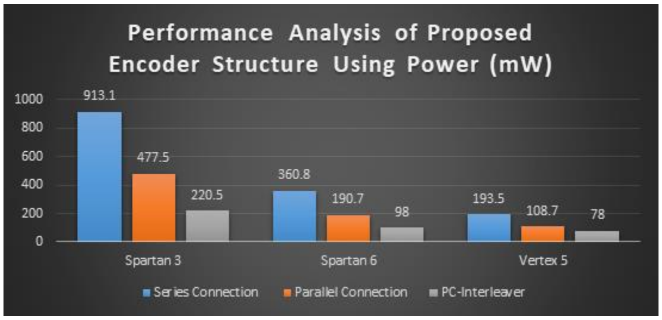

Fig. 12 Performance analysis of projected encoder structure using power (mW)

Fig. 10, 11, and 12 illustrate the performance of serial and parallel connections in terms of power, area and time delay. It proves that vertex 5 requires a low amount of power of 78mW, an area of 35 mm2 and less delay of 3 ms.

5. Conclusion

Design and analysis of the performance of series and parallel connection of hybrid raptor code and recursive systematic convolutional encoding process are carried out and obtained the simulation result appropriate for the 6G communication system. The proposed interleaved parallel connection of two error control methods delivers a lower Bit Error Rate and less Signal to Noise Ratio. Series and Parallel cascade form of connection prove that it improves the overall system performance, and the same will be implemented using diverse FPGA such as Vertex 4, Vertex 5 and Spartan 6. Finally, simulation results show that Vertex 4 required less power, area and delay than other FPGA devices. In the future, it may improve by adding an effective coding technique and implementing another FPGA device to analyse the 6G communication system's performance.

Conflicts of Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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