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Original Article

Multilevel Inverter Design with Reduced Switches & THD Using Fuzzy Logic Controller

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Abstract *- Multilevel inverter technology is now often used for residential and industrial medium voltage conversion. Because of nonlinear loads linked to the power supply, harmonics can seriously destroy equipment. Therefore, eliminating losses is essential to enhancing overall efficiency. An innovative 31-level, asymmetrical multilevel inverter topology in solar PV systems is presented in this paper. The proposed 31-level cascaded H-bridge asymmetrical multilevel inverter's significant benefits were fewer switches, reduced loss, less electromagnetic interference, and a reduced total harmonic distortion. The system was designed to feed solar energy into the power grid. The PV-isolated system demands a consistent DC voltage level from the photovoltaic cells, and the Fuzzy logic control technique is employed to achieve a stable output. A four-level flyback converter system integrated between the photovoltaic modules and the inverter greatly enhances the PV voltage over the DC link voltage. To develop driven pulse signals for the power electronics switches, the above topology needs to employ a multicarrier offset pulse width modulation technique. The bitwise voltage sources for the input DC voltages are 6Vdc1, 12Vdc2, 24Vdc3, and 48Vdc4. MATLAB/SIMULINK software is used to illustrate the performance of this multilevel inverter. A thorough examination of the suggested topology is beneficial due to its decreased accessory count, consistency, and value-effectiveness after a systematic comparison with the same and other levels in terms of switches, sources, and quantity of diodes & capacitors. The findings designed that this topology's THD is 3.06% and complies with IEEE harmonic criteria.*

Keywords *- Multilevel inverter, DC voltage, Fuzzy logic control, THD and Modulation technique.*

1. Introduction

Multilevel Inverter Topology has become popular in strong applications in recent years. The main idea is to use the most active semiconductor connectors to deviate the simple voltage during the power conversion. Multilevel inverters are widely employed for a wide range of purposes, especially alternative energy, FACTS devices, and solar systems. Most inverters are based on traditional Multilevel inverters such as NPC, T-type and (CHB). Cascaded inverters with multiple DC sources are another essential element of the topology among multilevel inverters. Both symmetrical and asymmetrical configurations of cascaded inverters are proposed. A recent study carried out a new converter topology and a unique modulation technique using hybrid architecture to improve efficiency, enhancement factor, and lower THD.

Introducing a new high-performance multilevel single-phase hybrid inverter. Because it offers single-phase conversion, small V and I, high gain & efficiency. Impedance-based enhancement converters are commonly used in solar applications. This structure has merits such as improved low power consumption, V gain characteristics, multi-layer o/p voltage, and high η [1]. The single-phase multilevel inverter architecture uses time-domain optimization techniques to reduce the THD of the o/p V and I at any RL load. It is used to calculate the switching angle of the inverter as an optimization constraint. [2]

Other approaches have also been suggested for isolated & networked apps. An original 1-ϕ Direct current - Alternating current multilevel modular converter (CTMLI) has been introduced with a compact amount of components at the o/p. In one phase, three full-bridge (FB) circuits are linked in equivalent to a DC to obtain a Nineteen o/p volt at the o/p devices; then three 1-ϕ combined modifiers are connected in sequence. Individually circuit is precise by a certain switching freq., and individual 1-ϕ modifier has a certain turns relation [3]. A five-level (5L) single-phase converter is used to demonstrate the switching strategy and multiple modes of operation. Since only three conductive switches generate each voltage level in each mode of operation, rigorous calculations are proposed to determine the lowest possible conduction and switching costs [4].

Furthermore, the nearest modulation approach is employed to boost overall efficiency by lowering the power converter's switching activity. The amount of switch elements and DC sources in the multilevel inverters for grid integration is kept to a minimum. The system's stability and sensitivity analysis is performed to evaluate the controller. This approach for distributed generation uses a multi-resonant proportional-resonant (PR) controller and a multi-resonant proportional-integral (PI) controller with multi-layer inverters to reduce the harmonic content of utility power and fixed disturbances. State error of grid-injected power [5]

A study was conducted in one step. Introducing reduced units makes it possible to create multilevel inverters for renewable applications. Multilevel symmetrical inverters use two DC sources. In the main circuit, the polarity of the output voltage circuit is controlled by a single-phase H-bridge converter. The supplementary network regulates the voltage on the dc Input bus by adjusting the number of input DC units before the main line. 2 PWM approaches have been investigated to control the output of multilevel inverters based on minimum power dissipation and minimized THD [6]. A recent study of a multilevel single-phase inverter is an interesting approach. Single-stage multilevel inverters are becoming popular in low-voltage and distributed power applications. The inverter has robust and controllable characteristics [7].

MLIs (multilevel inverters) have attracted much interest in the sector. This study proposes a method for finding optimised DC sources using the Particle swarm optimization to increase voltage quality and minimise thd. The PSO algorithm determines the optimal displacement angles [27]. This architecture is more effective and priced than standard multilevel inverters, with fewer DC sources, power supplies and component count factors and lower overall harmonic distortion. These multilevel inverters are used in FACTS and grid-connected renewable applications and are designed to be reliable under nonlinear loads. [9]

Multilevel inverters (MLIs) have recently gained notoriety for their excellent "voltage drop" & "total harmonic distortion (THD)" characteristics. MLI provides the convenient answer for the inclusion of alternative electricity, but circuit stability decreases as the number of power switches increases. Circuit implementations such as device count reduction (RD) with fault tolerance (FT) capabilities can improve reliability. The "Modified single-phase fault-tolerant MLI topology" shows the FT function's open-circuit fault (OCF) tolerance. Compared with other similar MLI topologies, the modified design has fewer diodes, switches, DC sources, capacitors, drivers, and overall block voltage (per drive) [10]. This study presents two innovative designs of 1-ϕ, multi-stage dual inverters for symmetrical and asymmetrical configurations. These designs may be utilised to drive and regulate electrical equipment and link renewable energy sources. This topology has the significant advantage of equalizing the capacitor voltage regardless of operating conditions, load characteristics or modulation index. In addition, the proposed topology can be scaled in a cascade to reduce complexity and significantly improve performance. A new topology was developed to show improved performance in relationships with the total number of switches & DC resources [11]. Inverters have low reliability due to the tall disappointing amount of semiconductor devices & capacitors and the high requirements in multilevel inverter topology architectures. Fewer devices, saving output power in the event of a burden, tolerating exposed and S/C breaker faults at any fault location, handling single switch faults and more & attaining normal voltage matching. Capacitors are a major challenge for remaining results for fault-tolerant network topology. The result is a fault-tolerant architecture based on standard inverters.[28]

Low-base switching frequencies are used in PE transformers for middle and high-voltage applications to reduce switching losses. The new technique is based on merging these two control systems, with certain levels of freedom used to remove specific harmonics and others used to minimize the residual THD content. In particular, this extended formulation of the problem is an example of minimum THD and H problems [13]. This paper proposes a novel design for a multi-layer inverter based on a redesigned capacitance design. The topology customs the charge/discharge characteristics of the cap. to increase the o/p voltage without using magnetic elements. Compared to similar conventional topologies, the planned ckt has fewer apparatuses, such as s/w, vol. sources, and capacitors. [14]

A number of inverters with higher voltage levels were presented in [29] to decrease the number of power switches. The output of these inverters' DC phases is transformed to the AC step by a full-bridge converter (FBC).

Based on the switch capacitor multi-layer inverter in [16], this provides a high boosting ratio inverter (SCMLI). A fuzzy logic simplified lowered detector is developed to accomplish MPPT control for the solar cell.

This article describes a 3-source fifteen-level architecture with 40 dc vol. sources and 12 switches, resulting in a total of 25 o/p stages. The researchers investigated different load circumstances and dynamic fluctuations in load and MI [17]. [18] developed a single-source-driven quad-raise multilevel inverter architecture (QB-MLI) with fewer resources than the previous switching capacitor topologies. With the associated control logic, this controller is used to manage the voltage levels of the two capacitors. They may be found in almost every medium or high motor-driven application, such as mine and construction sectors, drive systems, electricity production, and transmission, to name a few. [19]

The suggested various predictive control model (MPC) method for T-type 3-ϕ 3-level inverters has lower complexity and a constant switch freq. compared to steady-state, energetic reaction, and unbiased point vol. matching performance [20]. A number of inverters with higher voltage levels were presented in [21]. Traditional multilevel topologies such as the FC & NPC employ a single primary source, but the cascaded inverter design uses many isolated Power sources [22]. The cascaded multilevel inverter architecture was chosen due to its modular situation and suppleness in adding more modules. [30]

In symmetrically constructed CHBs, all DC-vol. ideals are like, however, in asymmetrically configured CHBs, DC-voltage source values are unequal to obtain essential developed vol. levels. CHB approaches are used for middle and developed vol. levels, while in other topologies, balancing and distribution vol. is difficult for advanced vol. levels [24]. This Pulse Modulated SCHM-bridge Multilevel Inverter reduces Entire Harmonic Distortion (THD). APF is used to correct harmonic current magnitude in the opposite direction. A pulse modulation approach is used in the planned SCHM system for component layout employing a linear quadratic regulator (LQR) [25]

2. Modified-Cascaded Inverter Topology

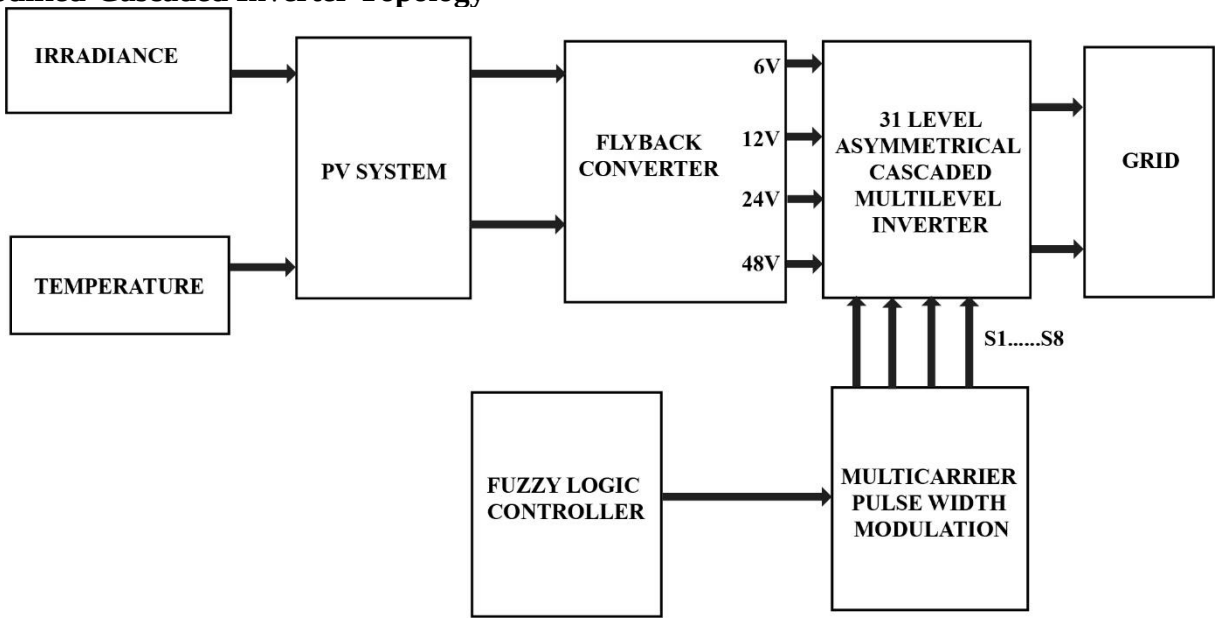

Fig. 1 Block Diagram of Proposed System.

The thirty-one-level inverters are supplemented by eight power switches and a DC vol. supply to provide the necessary output. The gate-triggering pulse for the 31-level MLI uses a multicarrier offset PWM scheme. The suggested structure generates more voltage levels from a few DC voltage sources and switches. The suggested topology entails a DC voltage source and eight unidirectional power switches. The power switches were represented by the symbols S1, H1, S2, H2, S3, H3, S4, and H4, and VDC was chosen to identify the DC voltage source. The flyback converter, which requires an input voltage of 15 volts, generates the DC voltage sources (Vdc1, Vdc2, Vdc3, and Vdc4) (Vdc). The pulses are produced successively and sent to the switches to obtain the required output voltage using the multicarrier offset modulation technique. The pulses are synthesized individually using the multicarrier offset modulation technique and fed to the switches. A few voltage output levels are generated irrespective of the switch-ON and switch-OFF states. The source vol. in this block diagram (Fig. 1) is fixed at Vdc1 = 6 V, Vdc2 = 12 V, Vdc3 = 24 V, and Vdc4 = 48 V. 100-ohm resistor and 175 mH uses, respectively, to get the extreme amplitude.

2.1. PV Module

Designing solar cells is a crucial step for comprehending a solar PV system. The proposed circuit consists of the photovoltaic cells, a four-level flyback converter, and a 31-level multilevel inverter is exposed in Fig. 2. A proposed ckt. with properties of (I-V) and (P-V); the consequence of solar irradiation and temperature are the basic categories that could be used to simulate solar PV. The intended solar PV has the behaviour of adjusting its output based on the circumstances.

2.1.1. Fill Factor of a Solar Module

The fill factor of a solar module is the ratio of its max power (Pm = VmxIm) to the product of its open ckt. Vol. and short ckt. Current.

$$Fill\ Factor = \frac{\text{Pm}}{\text{Voc}\times\text{Isc}}$$

The solar module is better when the Fill Factor (FF) is higher.

The relation of the maxi power under typical test conditions to the i/p power is known as the efficiency of a solar module. A solar module's i/p power is solar energy, which is equivalent to 1000 w/m2. Accordingly, the cell's nominal input power is thousand A W, where A represents the solar unit's visible part.

$$N = \frac{Pm}{1000A} \times 100\%$$

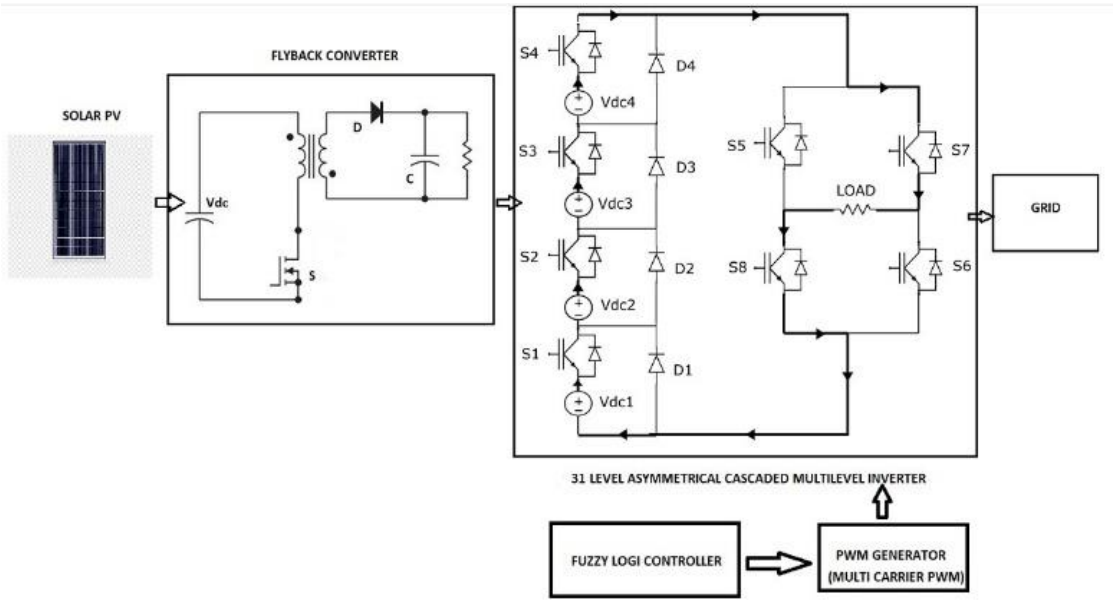

Fig. 2 Solar PV flyback converter for the proposed 21-Level MLI.

2.2. Flyback Converter

Fig. 3 depicts the flyback converter (FBC) with a R load. The FBC is the device that started it all, in which the inductor is divided in two to produce a transformer enabling electrical isolation between the i/p and o/p. In comparison to the fundamental transformer, it is modest in size. It can even be powered by low voltages like 5 volts or 12 volts. A 15V DC input and four AC outputs are needed in this arrangement. A high-frequency transformer that is a MOSFET switch is used to manage it. Since an IGBT can only function at a maximum frequency of 25 kHz and a flyback converter requires a minimum operating frequency of 100 kHz, we are unable to use an IGBT in this situation.

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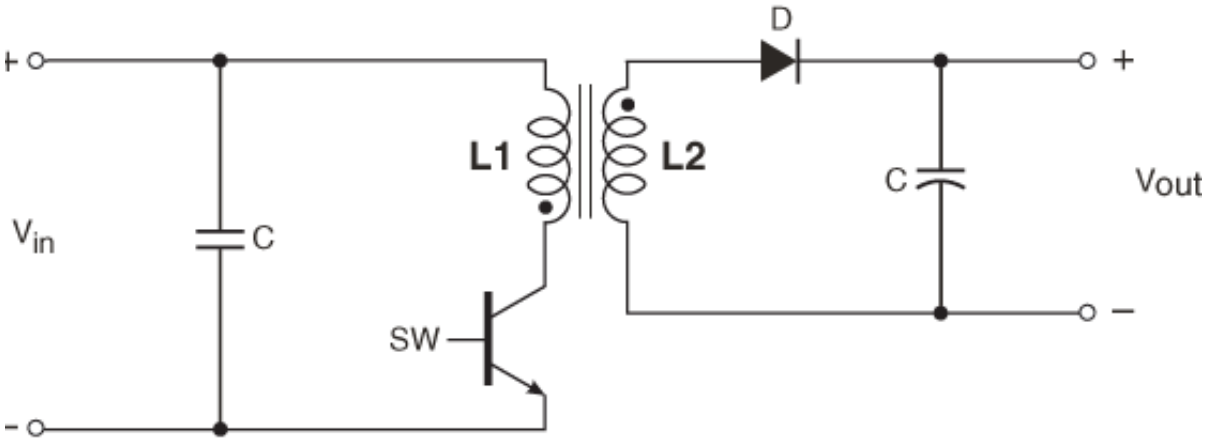


Fig. 3 Flyback converter

2.2.1. DC-DC Flyback Converter with Various DC Output Voltages

Flyback converters are used for high voltage power supplies for TVs and computer monitors and have an output power of 50–100W. It offers versatile performance with a small number of components. For example, you can add windings, diodes, and capacitors to increase the power. The voltage across the transistor is equivalent to the sum of the dc reference vol. Vg & the replicated load vol. V/n. The additional vol. is sometimes caused by sounds related to the leakage inductance of the transformer present. A trigger circuit may be required to reduce the magnitude of this clear vol. to a safe level within the transistor's maximum voltage. There are two methods commonly used when specifying a flyback converter when using the mean-shift approach. The initial path involves returning the stack to the critical side and then replacing the MOSFETs and diodes with PWM switches and linear analogs.

3. Multi-Carrier PWM Technique

Fig. 4 shows a schematic diagram of the asymmetric cascade inverter topology of the system. A structure that combines an H-bridge and a modular design. The H-bridge remains the same, but in a modular design, the DC source voltage and the number of switches must be changed accordingly to produce a multilevel output. The o/p voltage level in a modular design can be raised by raising the DC source and switch voltage. Analyzes performed on an asymmetric cascaded converter for level 31. In this configuration, the control signals for the inverter ckt. are made using a multicarrier PWM method. Multi-stage inverters can use this PWM technology to self-balance. A 31-level multilevel asymmetric cascade inverter is presented. In the proposed topology, there are many advantages to reducing schematic components. These advantages are part of these advantages to produce low tensions, low levels, and low tensions. The proposed technique in multilevel inverters is suitable for use in both industrial and renewable energy sources.

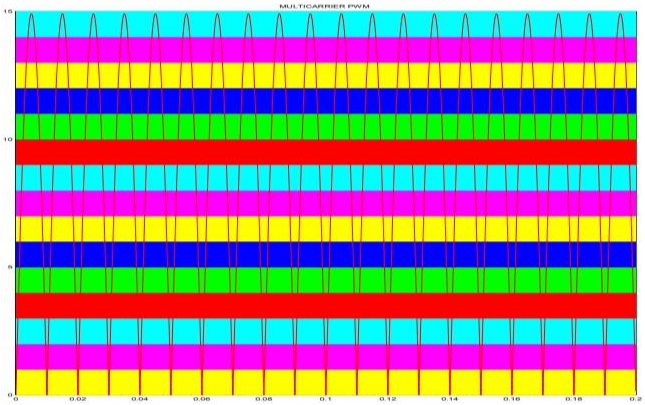


Fig. 4 Multicarrier PWM Modulation Technique

If the DC source voltages do not have the same amplitude, the inverter is called an asymmetrical cascade inverter. It is easy to raise the o/p vol. level by increasing the DC vol. levels and the amount of switches in the sectional project. The modified topology makes it possible to create multiple constant voltage sources and multiple voltage levels without adding switches. Use the following formula to determine the o/p vol. level for an unbalanced formation:

$$L = (2^{n+1} - 1)$$

3.1. Fuzzy Logic Controller Method for Multilevel Inverter

The Fuzzy Logic controller forms the description rules of the target management system to improve the system's functioning and control efficiently.

The process that shows a person's opinion is Fuzzy logic. The fuzzy logic controller is made up of three fundamental parts. Fuzzifier; Inference Engine; Defuzzifier.

3.1.1. Fuzzifier

To be employed with the fuzzy controller, every variable used to create the control signal must be specified using fuzzy rules notations and linguistic labels.

Positive Big (PB), Positive Medium (PM), Positive Small (PS), Zero (ZE), Negative Small (NS), Negative Medium (NM), and Negative Big are the seven fuzzy subsets that make up each discourse universe (NB). Here, the normalised values of e and ce are [-1,1], and the range of mn is [-1,1]. Any combination of error (e) and change in error (ce) results in a maximum of forty-nine rules being used.

$$Error(e) = Vref - Vin$$

$$Rate\ of\ error(ce) = error(n) - error(n-1)$$

Table 1. Table for Rule Base

RULES		**Rate of error(ce)**						
		PB	PM	PS	ZE	NZ	NM	NB
Error (e)	PB	ZE	NS	NM	NB	NB	NB	NB
	PM	PS	ZE	NS	NM	NB	NB	NB
	NS	PM	PS	ZE	NS	NM	NB	NB
	ZE	PB	PM	PS	ZE	NS	NM	NB
	PS	PB	PB	PM	PS	ZE	NS	NM
	PM	PB	PB	PB	PM	PS	ZE	NS
	PB	PB	PB	PB	PB	PM	PS	ZE

3.1.2. Defuzzifier

A fuzzy set representing the controller's output in linguistic notation must be transformed into crisp decision variables before it can be used in the control system. A defuzzifier is used for this purpose. There are several ways to digitize. The two most widely used techniques are I Mean of Maxima (MOM) and (ii) Center of Area (COA). The COA method is used for most monitoring applications. The method produces results sensitive to all applicable rules and calculates the control plane. The result often slips off the management's surface control of the reference voltage on any load using a rule-based fuzzy controller. The fault and the amount of variation of the fault are the inputs of the fuzzy controller. The entire Simulink environment is used to create controller and inverter system applications. The method generates results sensitive to any rules used and calculates the centre of the control surface. As an outcome, results often slip above the control surface. Monitor the reference voltage at any load condition using a rule-based fuzzy controller.

3.2. Modes of Operations

Four input source voltages from Fig. 1 are considered for the thirtyone-level: Vdc1, Vdc2, Vdc3, and Vdc4. Individual source's i/p vol. is Vdc1 = 6 V, Vdc2 = 12 V, Vdc3 = 24 V, and Vdc4 = 48 V. An asymmetrical inverter ensures long-term sustainability for both a (+ve) group and a (-ve) group. The (+ve) group transmits positive signal waves, whereas the -ve group generates negative signal waves. Fig. 8 (a-p) shows the modes of operation at all positive and negative levels, including zero levels. The operating modes are described in the switching pattern in Table 2.

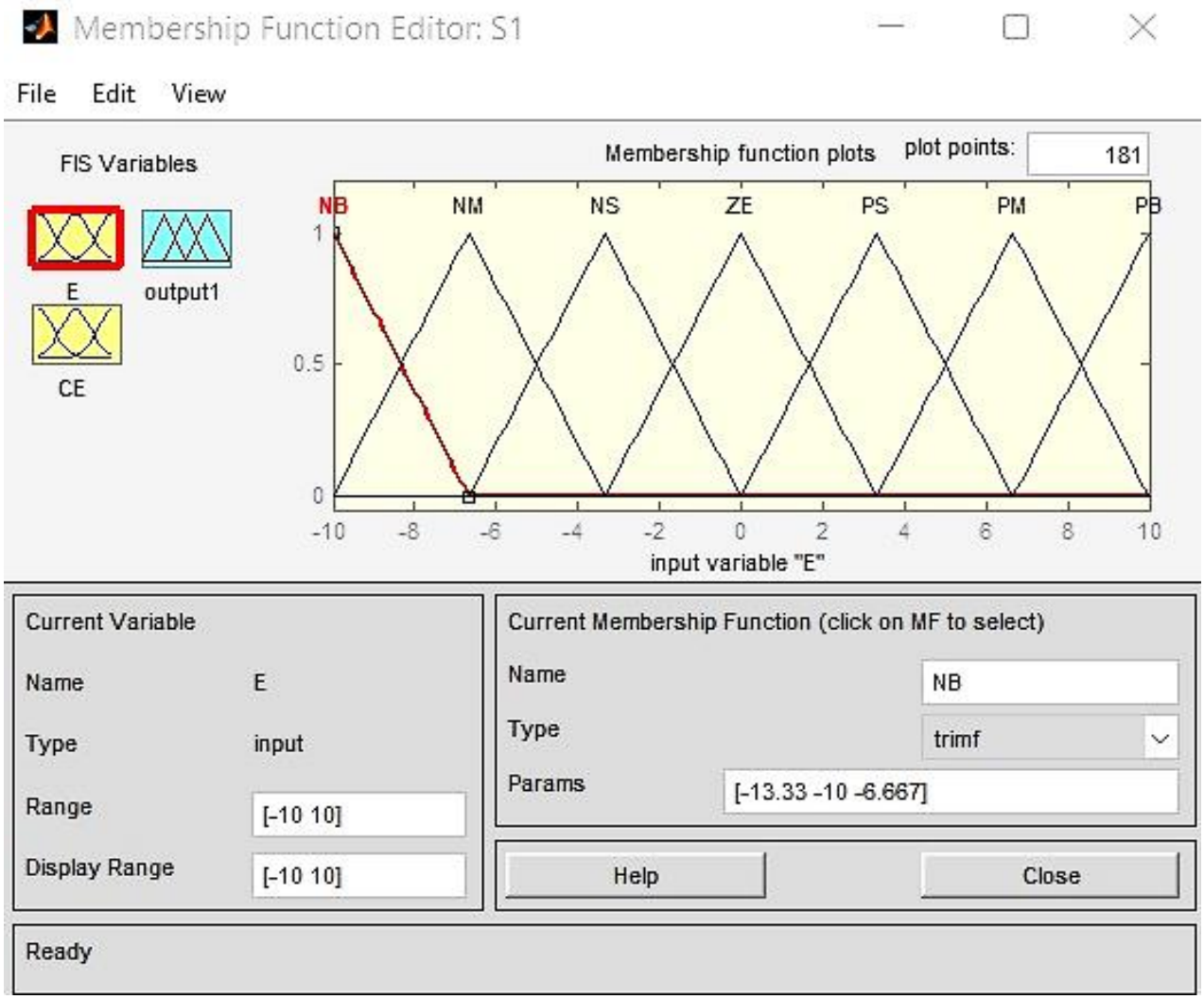


Fig. 5 Designed fuzzy controller membership function

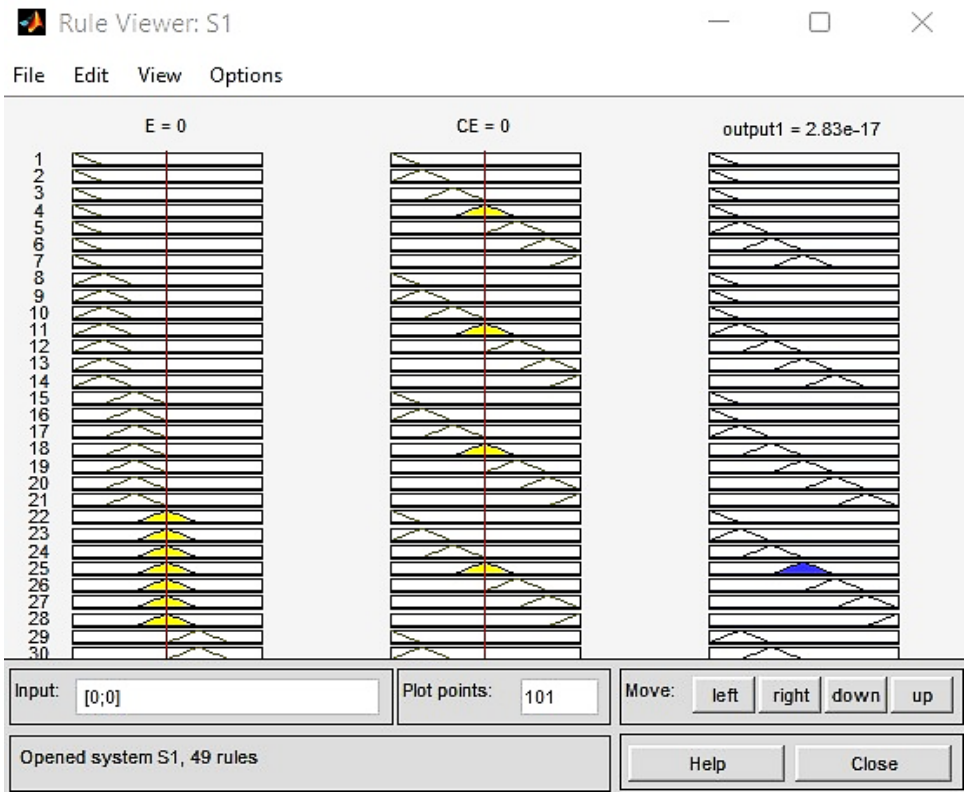


Fig. 6 Designed fuzzy controller rules

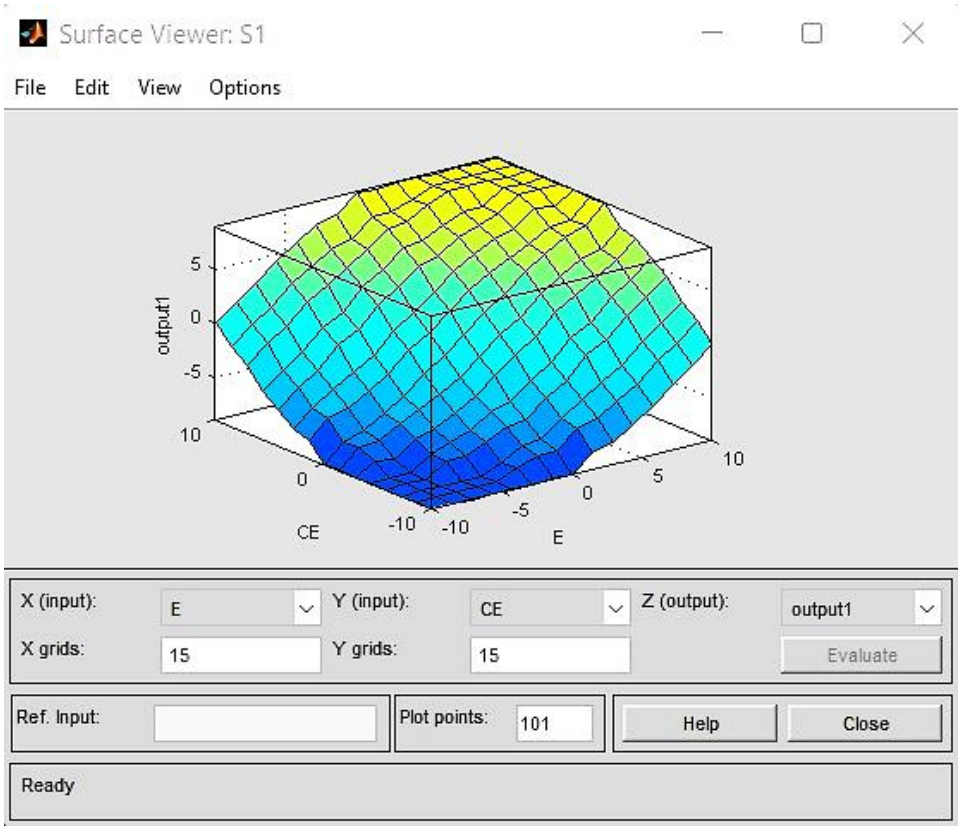
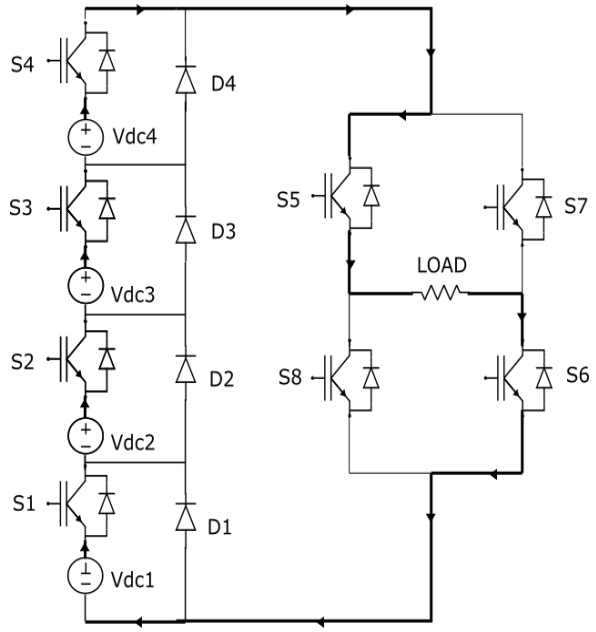


Fig. 7 The fuzzy layout's surface plot.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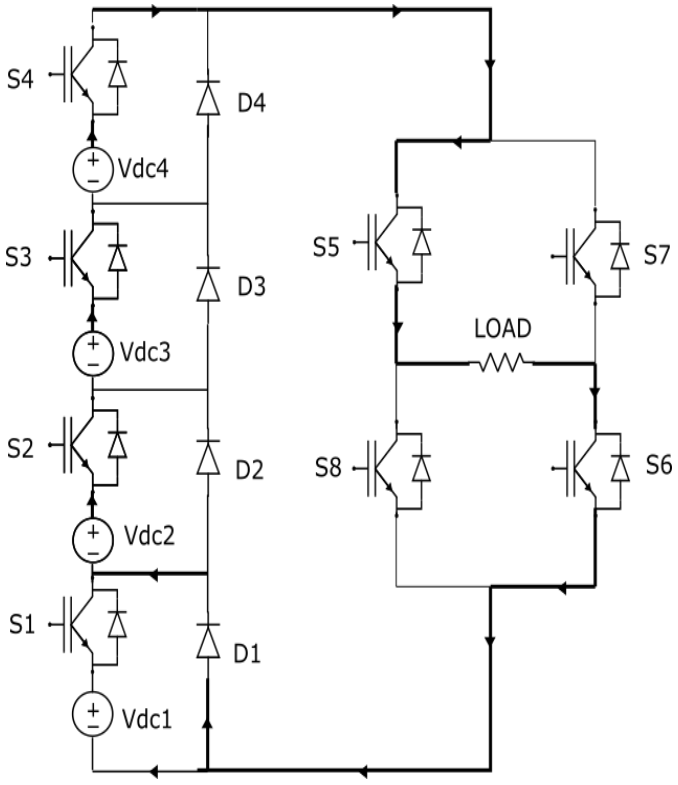
(a)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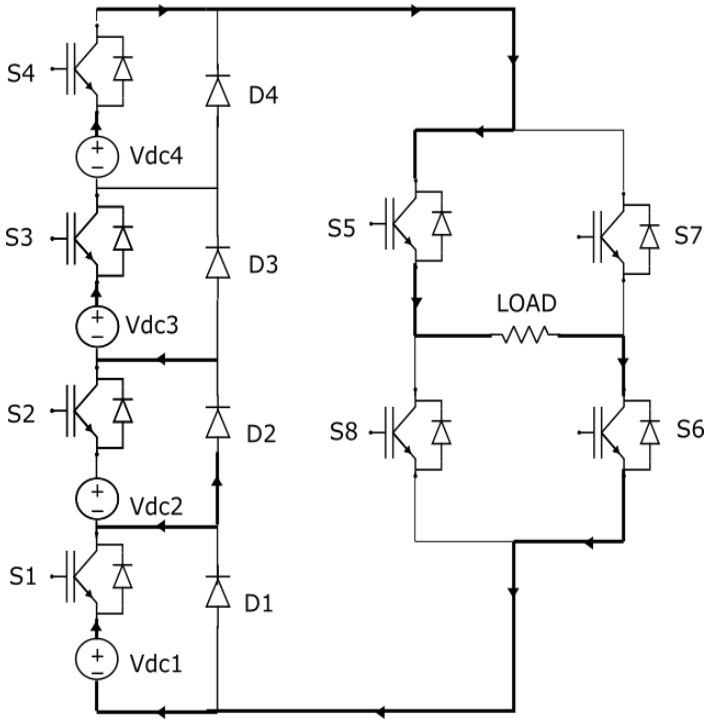
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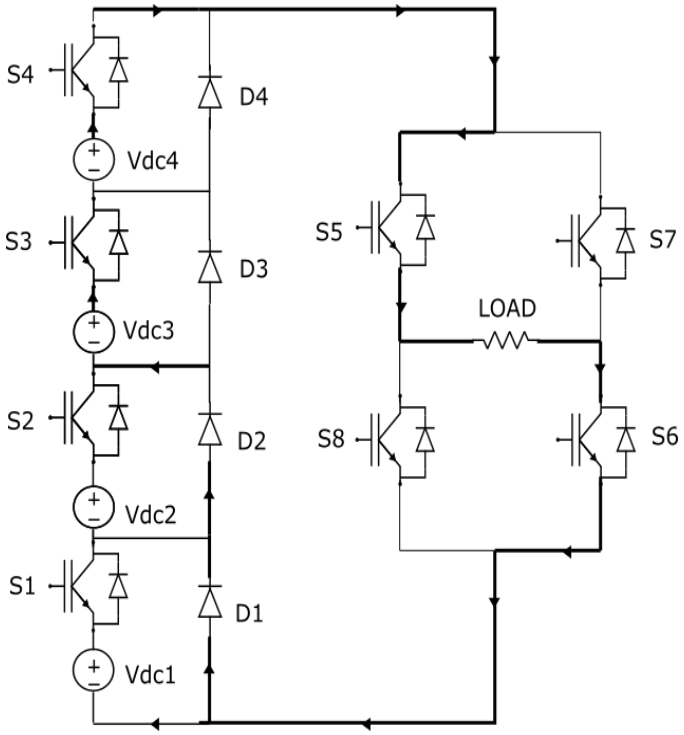
(c)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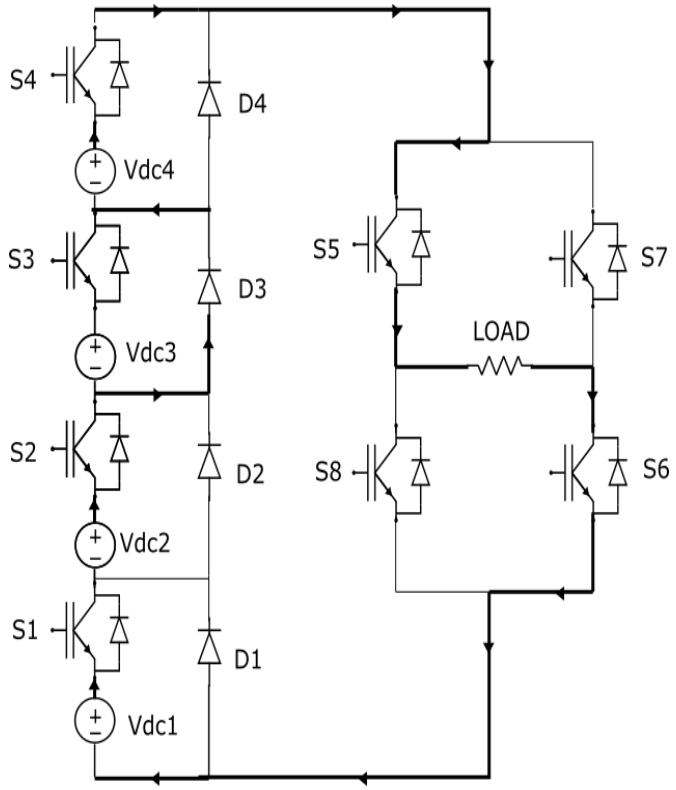
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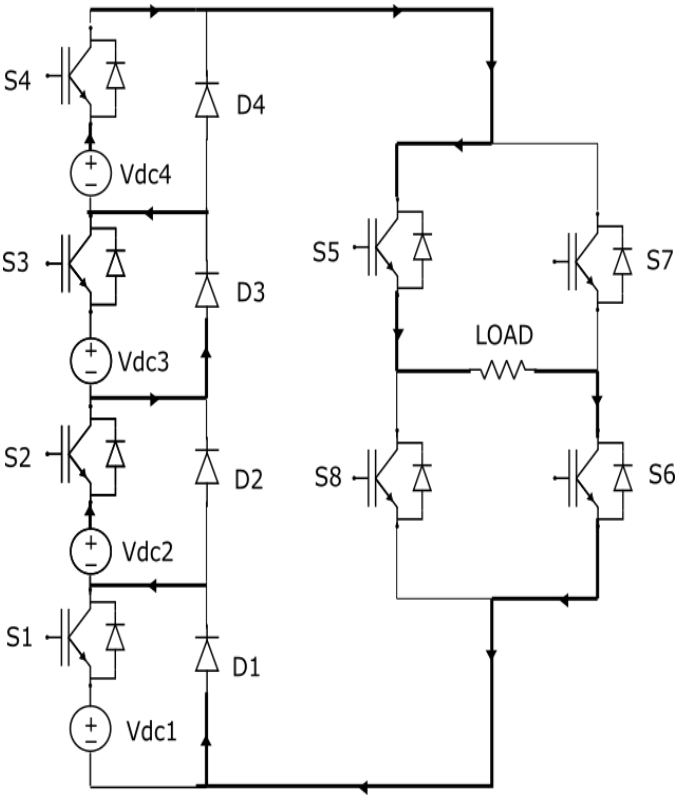
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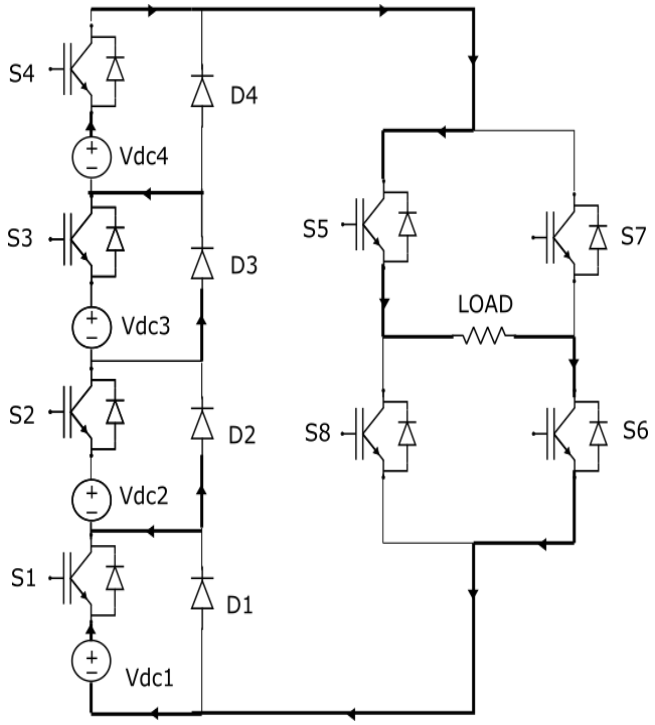
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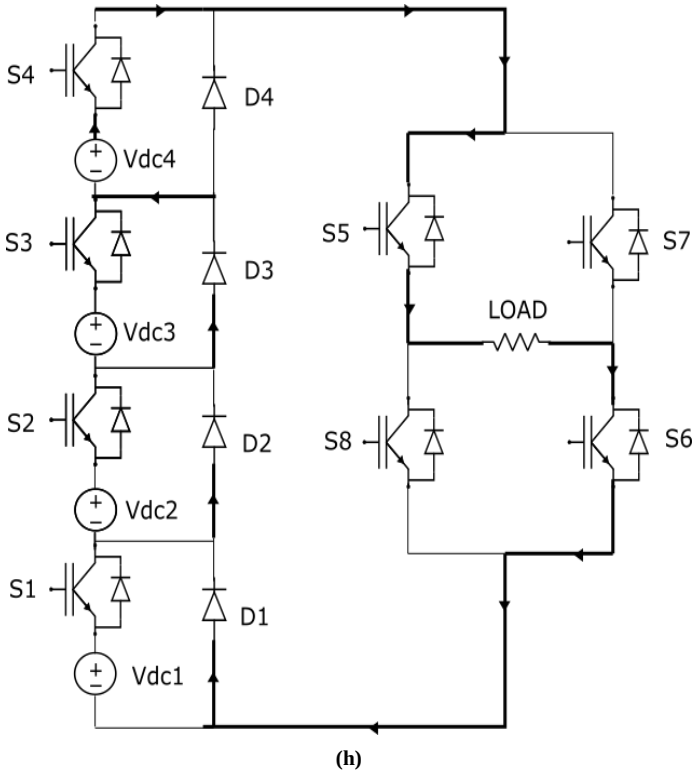
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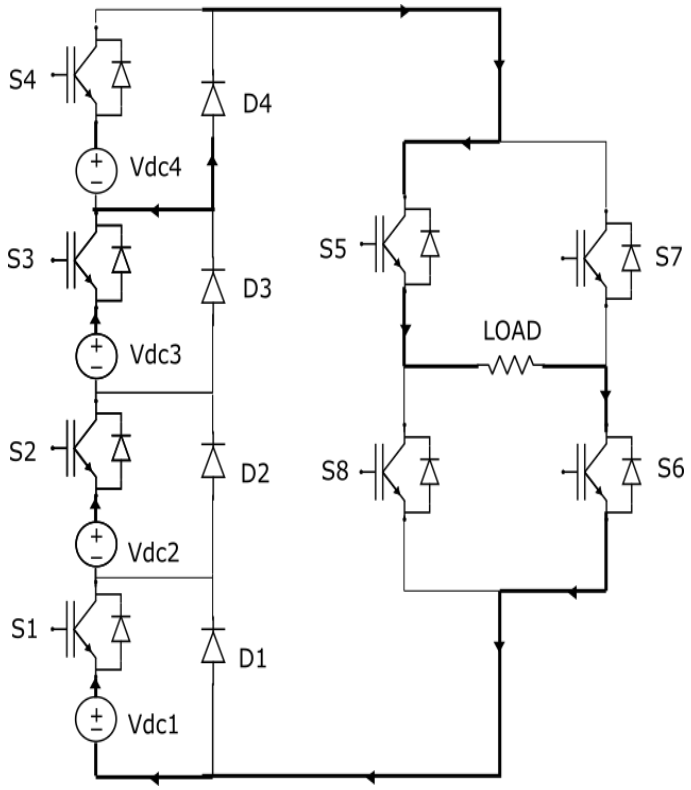
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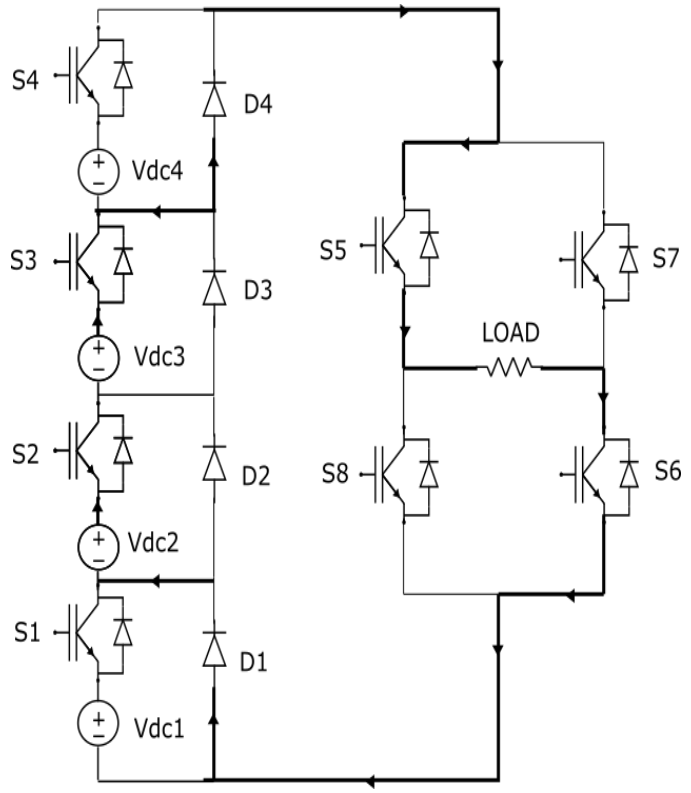
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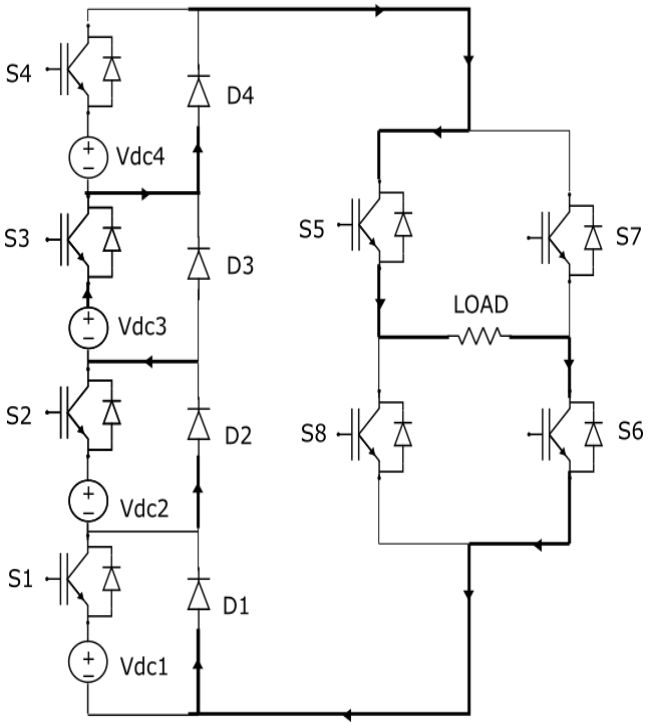
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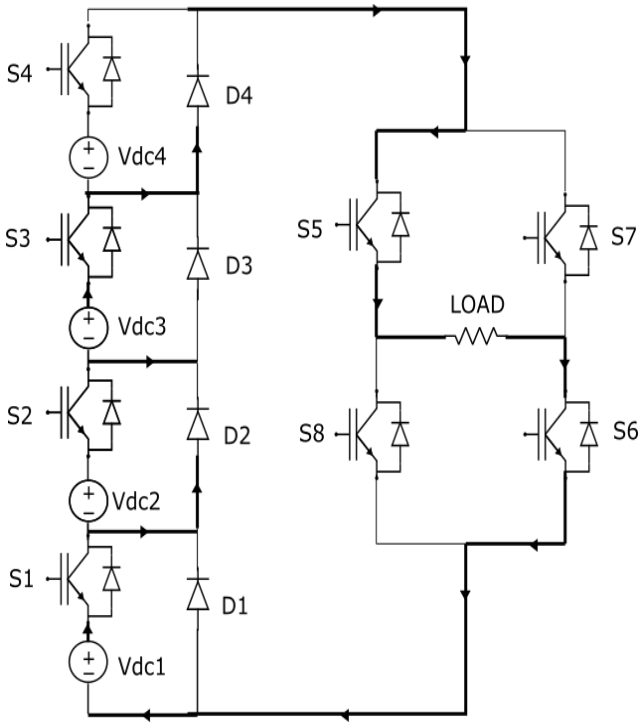
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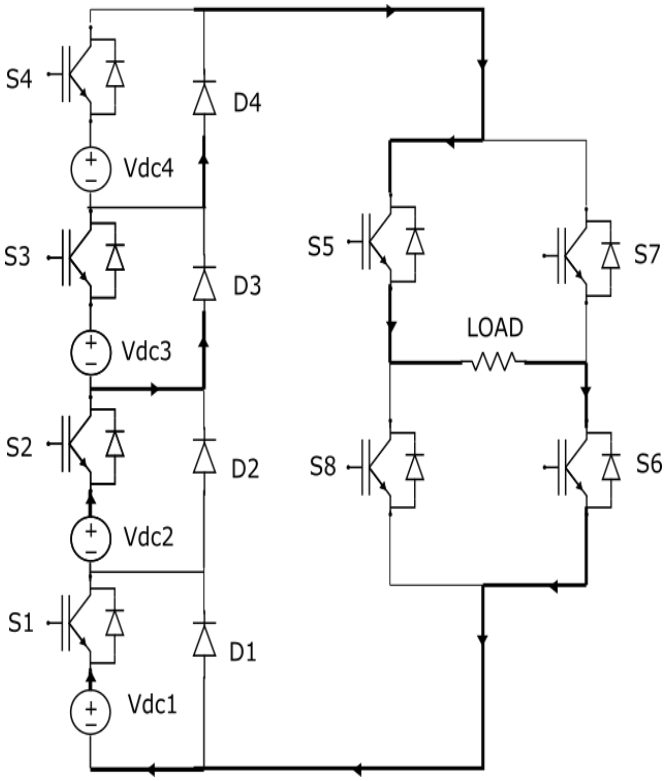
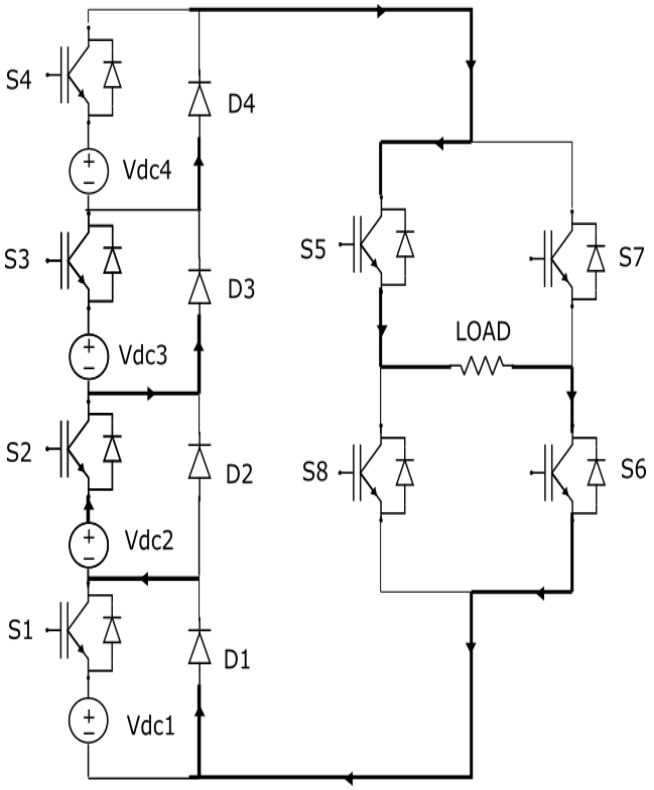
S6

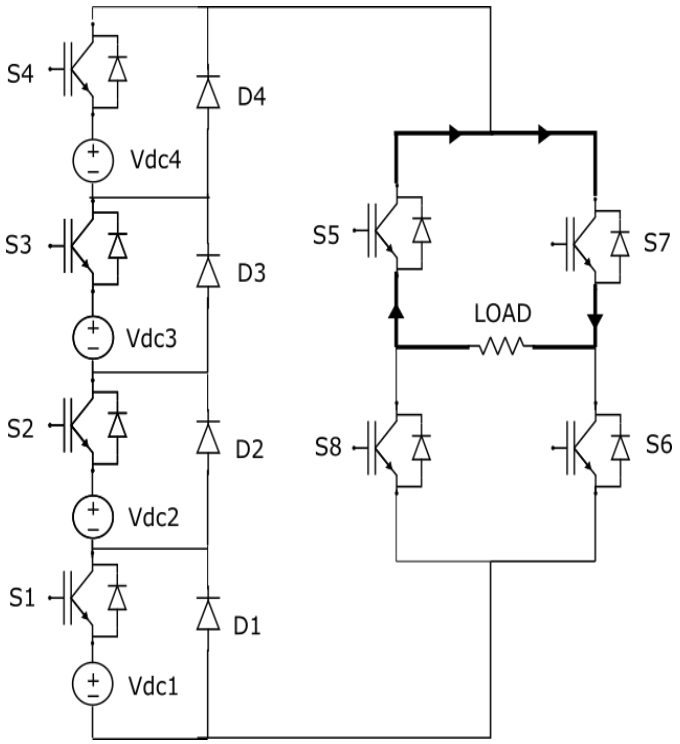
(l)


S4
D4
Vdc4
S3
D3
Vdc3
S2
D2
Vdc2
S1
D1
Vdc1
S5
S7
LOAD
S8
S6

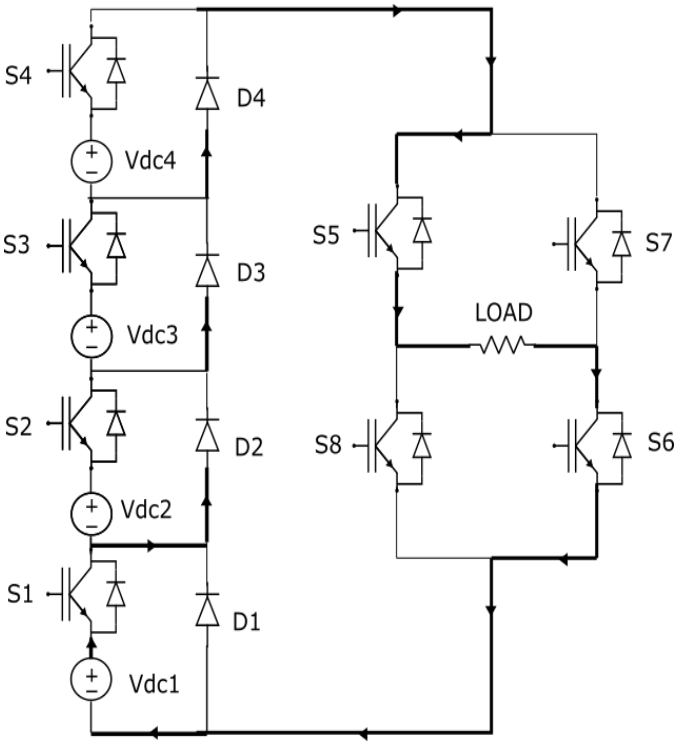
(m)


S4
D4
Vdc4
S3
D3
Vdc3
S2
D2
Vdc2
S1
D1
Vdc1
S5
S7
LOAD
S8
S6

(n)



(o)



(p)

Fig. 8 Designed 31-Level MLI's operational modes

Table. 2 Different Modes for 31-level cascaded inverter

MODES	Switches								Voltage Sources				Output Voltage (Vo)	
	S1	S2	S3	S4	H1	H2	H3	H4	Vdc1	Vdc1	Vdc1	Vdc1	Magnitude of Vo (Volts)	
1	1	1	1	1	1	1	0	0	1	1	1	1	+15 Vdc	+90v
2	1	1	1	0	1	1	0	0	1	1	1	0	+14 Vdc	+84v
3	1	1	0	1	1	1	0	0	1	1	0	1	+13 Vdc	+78v
4	1	1	0	0	1	1	0	0	1	1	0	0	+12 Vdc	+72v
5	1	0	1	1	1	1	0	0	1	0	1	1	+11 Vdc	+66v
6	1	0	1	0	1	1	0	0	1	0	1	0	+10 Vdc	+60v
7	1	0	0	1	1	1	0	0	1	0	0	1	+9 Vdc	+54v
8	1	0	0	0	1	1	0	0	1	0	0	0	+8 Vdc	+48v
9	0	1	1	1	1	1	0	0	0	1	1	1	+7 Vdc	+42v
10	0	1	1	0	1	1	0	0	0	1	1	0	+6 Vdc	+36v
11	0	1	0	1	1	1	0	0	0	1	0	1	+5 Vdc	+30v
12	0	1	0	0	1	1	0	0	0	1	0	0	+4 Vdc	+24v
13	0	0	1	1	1	1	0	0	0	0	1	1	+3 Vdc	+18v
14	0	0	1	0	1	1	0	0	0	0	1	0	+2 Vdc	+1v2
15	0	0	0	1	1	1	0	0	0	0	0	1	+1 Vdc	+6v
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17	0	0	0	1	0	0	1	1	0	0	0	1	-1 Vdc	-6v
18	0	0	1	0	0	0	1	1	0	0	1	0	-2 Vdc	-12v
19	0	0	1	1	0	0	1	1	0	0	1	1	-3 Vdc	-18v
20	0	1	0	0	0	0	1	1	0	1	0	0	-4 Vdc	-24v
21	0	1	0	1	0	0	1	1	0	1	0	1	-5 Vdc	-30v
22	0	1	1	0	0	0	1	1	0	1	1	0	-6 Vdc	-36v
23	0	1	1	1	0	0	1	1	0	1	1	1	-7 Vdc	-42v
24	1	0	0	0	0	0	1	1	1	0	0	0	-8 Vdc	-48v
25	1	0	0	1	0	0	1	1	1	0	0	1	-9 Vdc	-54v
26	1	0	1	0	0	0	1	1	1	0	1	0	-10 Vdc	-60v
27	1	0	1	1	0	0	1	1	1	0	1	1	-11 Vdc	-66v
28	1	1	0	0	0	0	1	1	1	1	0	0	-12 Vdc	-72v
29	1	1	0	1	0	0	1	1	1	1	0	1	-13 Vdc	-78v
30	1	1	1	0	0	0	1	1	1	1	1	0	-14 Vdc	-84v
31	1	1	1	1	0	0	1	1	1	1	1	1	-15 Vdc	-90v

3.3. Grid

A grid-connected system allows you to power your home or anywhere. Alternative energy sources like the sun and the wind are required. The extra energy produced is put back into the grid. Without renewable resources, electricity from the grid is used, eliminating the need for electricity storage costs such as batteries. The load consumes the MLI output, and the rest is sent to the network. An inductive filter is used because the power from the load cannot be passed directly to the grid.

4. Results and Discussion

An improved 31-level asymmetric cascaded converter was modelled using the Multi-carrier (MCPWM) method. Fuzzy logic is used for trace analysis. The 31-level skew corrected using Matlab/Simulink is a cascaded converter using the MCPWM method. The simulation specifications considered for this Resistive load are • I/p voltage (DC) = 90 volts (VDC1 = 6 volts, VDC2 = 12 volts, VDC3 = 24 volts, VDC4 = 48 volts). • FS = 2 kHz carrier switching frequency • Resistive-load = 100 The o/p vol. of the loading domain is 90 V (RMS voltage is 63.63 V). As shown, it specifies the o/p vol. of the load. The current through the load is 1.5 A. The graph shows the current flowing through the load. The figure shows a FFT study for a 31-stage asymmetric cascaded converter. The FFT THD value is 3.06%.

4.1. Simulation Circuit

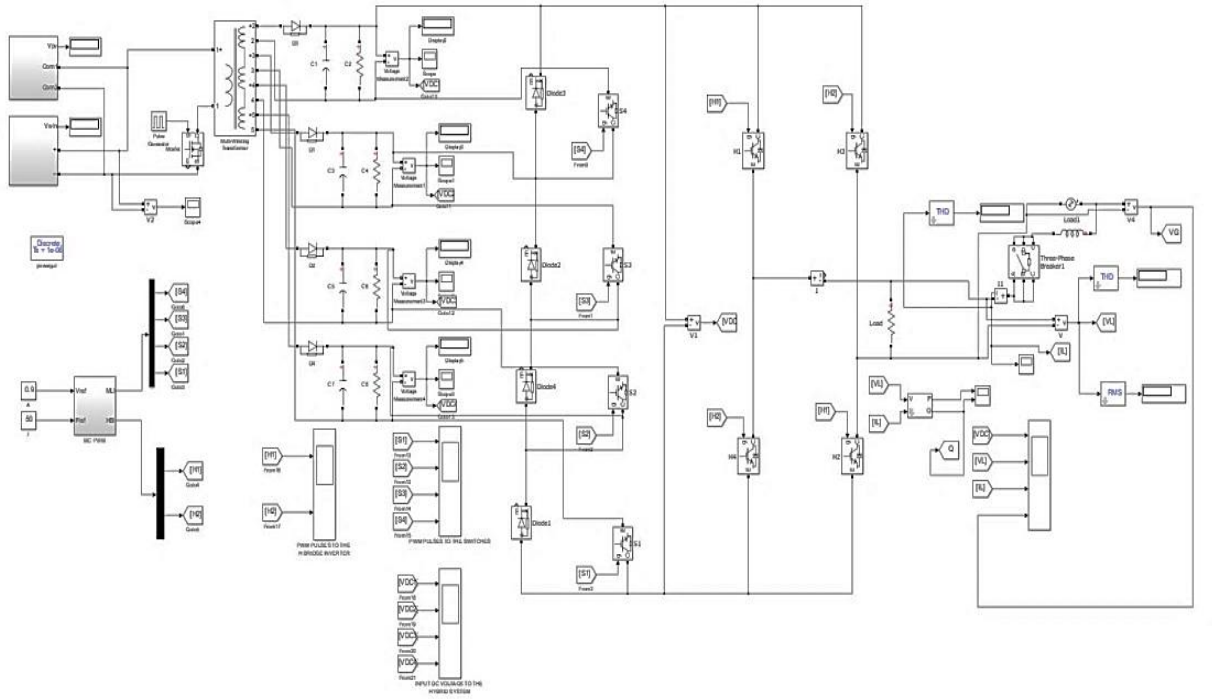


Fig. 9 Simulation Circuit of Proposed system

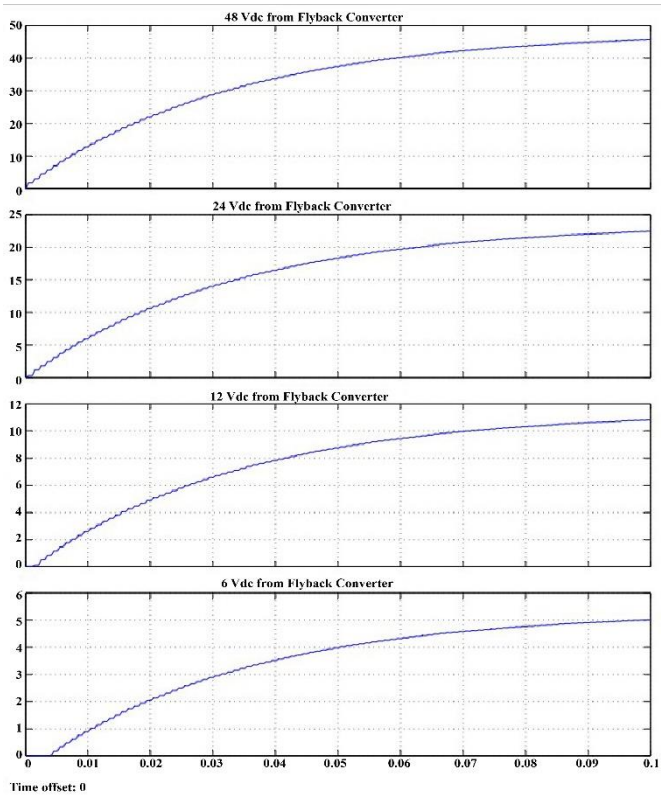


Fig. 10 Four Different Voltages from Flyback converter

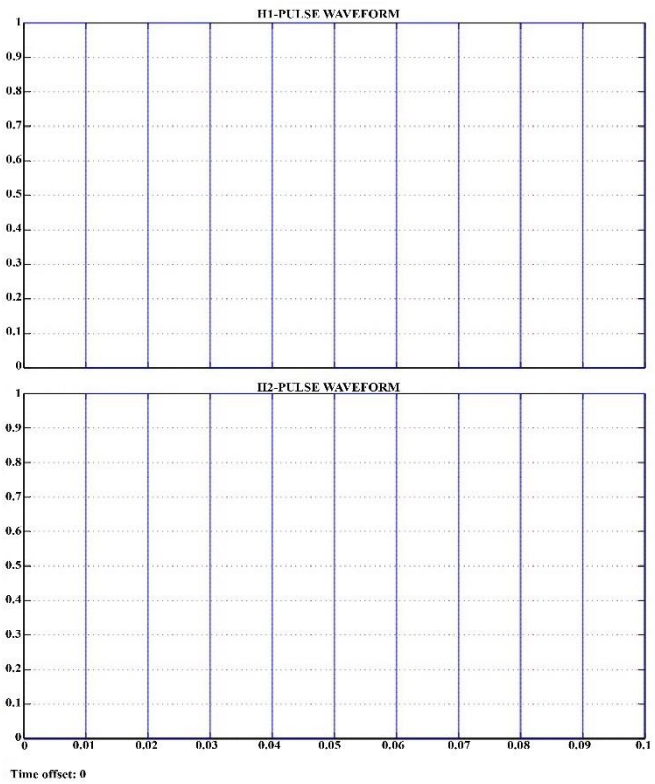


Fig. 11 PWM PULSES TO H1 AND H2

4.2. PWM Technique

A PWM uses a digital source to create analogue signals. It is essentially a square wave that is toggled between ON and OFF states. The multicarrier offset PWM technique is used in this project. Here, two control signals are compared, a carrier signal and a reference signal.

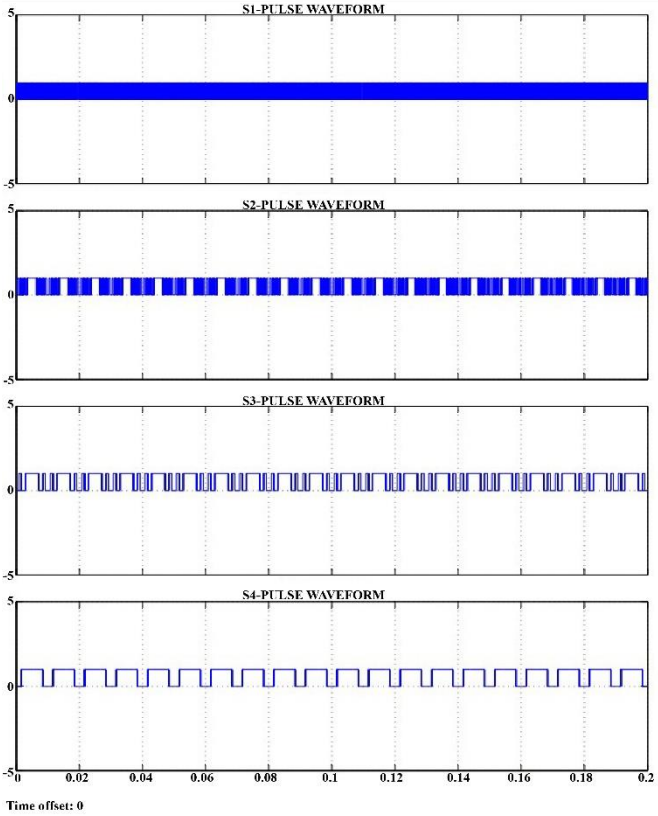


Fig. 12 PWM Pulses to S1 To S4

4.3. Simulation Output Voltage & Current

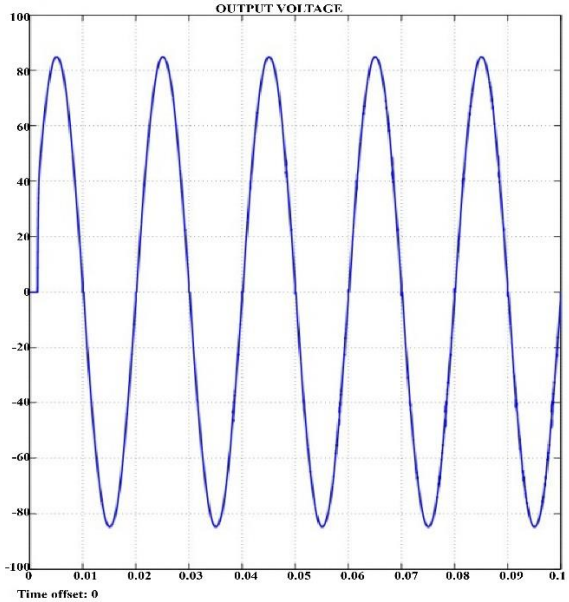


Fig. 13 Output Voltage

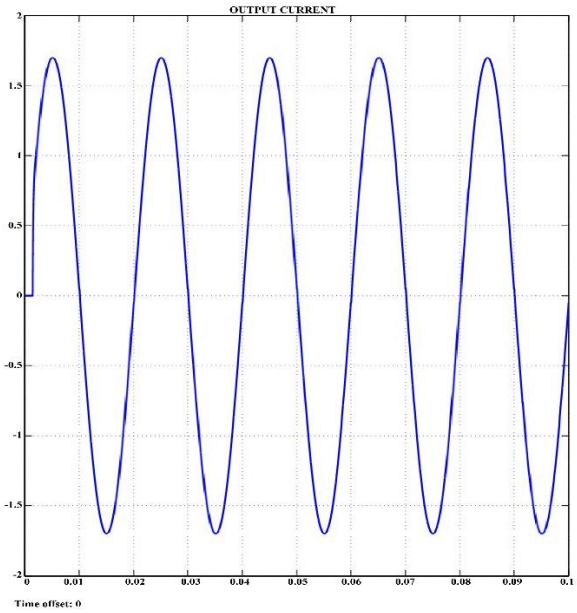


Fig. 14 Output Current

4.4. FFT Analysis

The FFT investigation of the thirtyone-level is obtainable in Fig .15 & 16. The value THD from FFT is 3.06% of output voltage and 3.17% of o/p c/t.

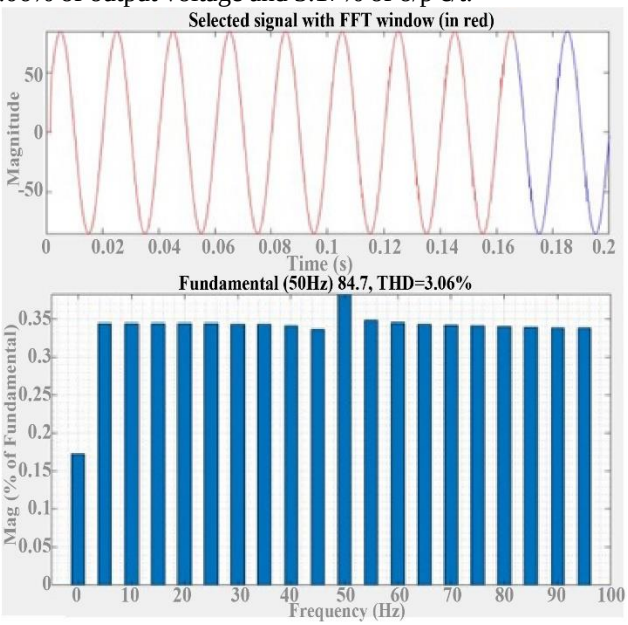


Fig. 15 Measurement of output voltage

The FLC monitors the input data & controls the converter to output the necessary current. The control technique was designed to determine the most precise MI for the multilevel inverter, which directly impacts o/p power. This closed-loop study enhances system solidity without compromising output quality. This controller keeps the o/p vol. constant depending on the ref. vol. in the regulator design, even when the i/p vol. to the inverter changes. The FLC can tolerate nonlinearity and operates with imprecise inputs.

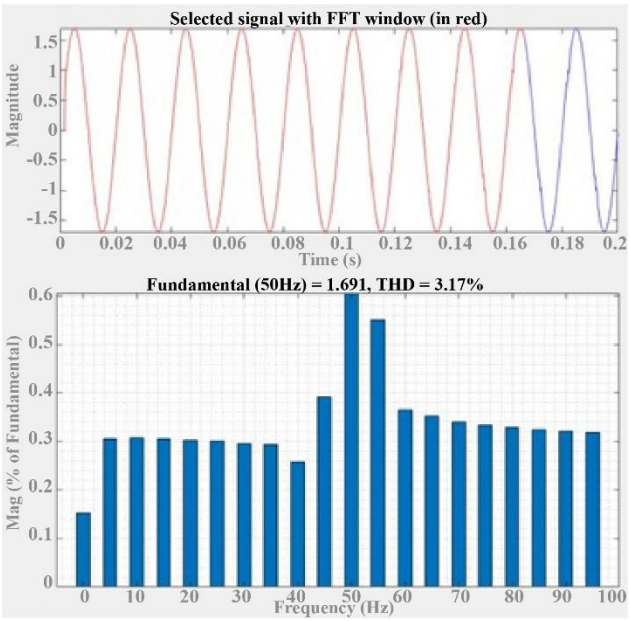


Fig. 16 Measurement of output current

4.5. Comparative Analysis of THD

Table 3. Comparative analysis of THD with some ref. papers

S. No	Reference papers	PWM technique	Controller	THD
1	Asymmetric multilevel inverter with the fuzzy controller using superimposed carrier PWM (2017)	Superimposed carrier PWM	Fuzzy logic controller	8.7%
2	31levelasymmetric cascaded MLI with DC-DC fly back conv. for PV systems (2020)	Low-frequency PWM	PIC controller	10.2%
3	THD minimization of the hybrid multilevel inverter using harmonic minimization technique (2018)	Harmonic minimization	High-speed multivariable digital controller (DS1104)	4.36%
4	Proposed paper	Multicarrier offset PWM	Fuzzy logic controller	3.06%

4.6. Comparison of Parameters with Conventional Topologies

Table 4. Comparison of parameters with different types of MLI.

ITEMS	DCMLI	FCMLI	CHBMLI	Ref paper	ProposedMLI
Number of Switches	60	60	60	10	8
Number of Sources	1	1	15	4	1
Output Voltage levels	31	31	31	31	21
Diodes	56	0	0	0	4
Capacitors	0	28	0	0	4
%THD	-	-	-	3.62	3.06

In Table 4, some parameters like the number of switches, no of sources, o/p vol. levels, semiconductor diode, capacitance, and % THD are compared among different types of MLI, such as those mentioned above in our proposed paper. From this table 4, we can see that the parameters of the proposed paper are efficient and with less Total Harmonic Distortion

5. Conclusion

A cascaded H-bridge asymmetrical multilevel inverter that generates any number of o/p vol. levels has been simulated. The key benefit of this design is the basic structure, which allows the multilevel inverter to be smaller and the driving circuit to be simpler. The simulation was done on the MATLAB/SIMULINK platform. A flyback converter's primary side has distinct output voltages of Vdc1=6V, Vdc2=12V, Vdc3=24V, and Vdc4=48V are generated respectively. Different voltage outputs are fed into Asymmetrical MLI, which produces a thirtyone-level o/p vol. level with only eight s/w. The o/p from the multilevel inverter is provided to the utility grid for further use. With the help of simulation, a THD value of 3.06% is obtained as the output voltage, and 3.17% is obtained as the output current. A comparative analysis of THD has been taken among some reference papers, confirming that the THD value in our proposed paper is less and within the IEEE standard (<5%). The results of the simulation are demonstrated in this paper.

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