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Original Article

ANFIS Control of PV Tied Grid System with Multi-Carrier PWM-Based Modular 5-Level Converter

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Abstract *- A grid-tied PV module with a Modular Multilevel Converter (MMC) is introduced in this work, which is highly preferred in various applications since it has high modularity and easy scalability. A PV output fluctuates, causing it to be unable to deliver stable DC voltage. So the multi-carrier PWM (MCPWM) method is employed to regulate an appropriate Modular 5 level converter (M5LC) that enhances the voltage. The ANFIS controller has been implemented to generate a reference signal and for the purpose of producing gating pulses for M5LC; this signal is compared to the carrier signals of MCPWM. A grid through three-phase VSI, which transforms DC voltage to AC voltage, functions as a converter's output voltage. A Reactive power compensation is made possible by employing the ANFIS regulator to manage the switches of the three-phase VSI. It results in reducing the total harmonic distortion (THD). The entire scheme is verified by MATLAB simulink.*

Keywords *- Modular 5 level Converter, PV module, Half Bridge Sub Module (HBSM), Grid synchronization and ANFIS controller.*

1. Introduction

The usage of PV-based power generation is actually high in recent days since it is environmentally friendly, static in structure and cost-effective. The issues in existing methods and technological advancements are the two major factors which have initiated the application of solar PV-based energy generation systems [1], [2]. The solar arrays are generally linked in series-parallel to satisfy the requirement of inverter voltage in PV systems [3]. In general, there are two types of PV systems, including standalone and grid-connected, among which the former consumes a huge amount of money since it includes a battery. In contrast, the latter is highly cost-effective, so it is recommended in various applications [4]. Due to climatic conditions and fluctuations, tracking maximum power from a PV panel is difficult. So many MPPT methods are employed to extricate maximum power from the PV module [5].

Different DC-DC converters are used to improvise an output voltage of a PV module. Initially, a boost converter is utilized to increase the fluctuating voltage of the PV panel. Still, it causes a sudden increase in input current and the occurrence of high power loss during switching [6], [7]. A buck-boost converter is employed to enhance voltage in the system, which operates in both the buck and boost modes [21]. Though it has a dual mode function, it fails to increase the voltage ratio in the broader range, which is overcome by the utilization of CUK and SEPIC converters. These converters have provided ripple-free current with improved system performance, but the obtained voltage of these converters is insufficient for PV power generation [9, 10].

Employing multilevel converters, including cascaded H Bridge (CHB) and diode clamped cascaded are emerged to avoid the specified issues of other existing converters, among which the diode clamped multilevel converter assists in removing the problems of partial shading and in reducing the distortions in voltage. In contrast, the CHB converter improves the PV battery system's Electro Magnetic Compatibility (EMC), and Cascaded Multilevel Converter achieves maximum power in unbalanced and partial shading conditions [11-13]. Despite having a lot of benefits, these converters are only useful in low- and medium-power operations. Hence modular multilevel converters are highly capable of working in high-power applications. Among various modular multilevel converters, modular multilevel matrix converters and Hexverter are generally used, which produce optimal output with high switching loss [22]. A modular 5-level converter is proposed to overcome this drawback in this work.

To control the converter, different modulation methods are utilized. According to the converter's switching frequency, the modulation techniques of grid-linked CHB converter are categorized as low-frequency and high-frequency modulation methods. Under the low-frequency modulation technique uses Selective harmonic

removal PWM (SHE-PWM), which regulates the harmonic spectrum of voltage and current. Under the high-frequency modulation method, phase shift PWM (PS-PWM) is utilized, which minimizes coupling inductance and increases efficiency [15-17]. The Space vector PWM is instigated to regulate an output voltage in a grid-tied PV system, in which an LC filter is used to limit the harmonics [23]. Due to its simplicity and easy instigation, The MMC is controlled using multi-carrier PWM methods in this study. The MMC comprises two different topologies, including a two-level submodule and a multilevel submodule, where HBSM and full bridge submodule (FBSM) are variants of multilevel submodules [19]. In this study, HBSM is utilized because the cost and power loss of MMC-based HBSM are lower than FBSM. To attain grid synchronization, the PI controller is utilized in prevailing systems, but it takes a long time to track the reference signal of voltage source inverters [VSI] [25]. Thus in this present study, ANFIS is employed to control the grid power in PV tied grid system since it owns fast learning capacity.

This study describes the ANFIS regulation of a PV-tied grid system using a modular 5-level PWM-based converter. The M5LC provides the constant DC voltage of the PV panel with the MCPWM technique. The ANFIS controller is implemented to control the grid power. A detailed explanation of the modeling of the PV panel, modeling of MMC, modeling of MCPWM technique, modeling of ANFIS controller, modeling of LC filter design and modeling of the synchronization of 3Φ VSI grid are given below.

2. Proposed Control Scheme

Normally, a PV module provides variable DC voltage, so it is necessary to improve a voltage as constant, for which a M5LC is employed since it has easy scalability and high power application. Figure 1 denotes the schematic representation of a grid-connected PV module with an M5LC control system.

A 3Φ M5LC with HBSM is employed in this PV system, and two SM are linked in series with a switching rate of $1KHz$ for each phase, which is then linked to a grid through a 3Φ VSI. A multi-carrier PWM method is employed to manage M5LC, maintaining DC voltage as constant and converting it to AC voltage at an output before supplying it via three-phase VSI to the grid. Synchronization of a grid occurs, and the THD has been decreased by using the ANFIS controller, which generates a reference signal analogized with a multi-carrier PWM carrier signal.

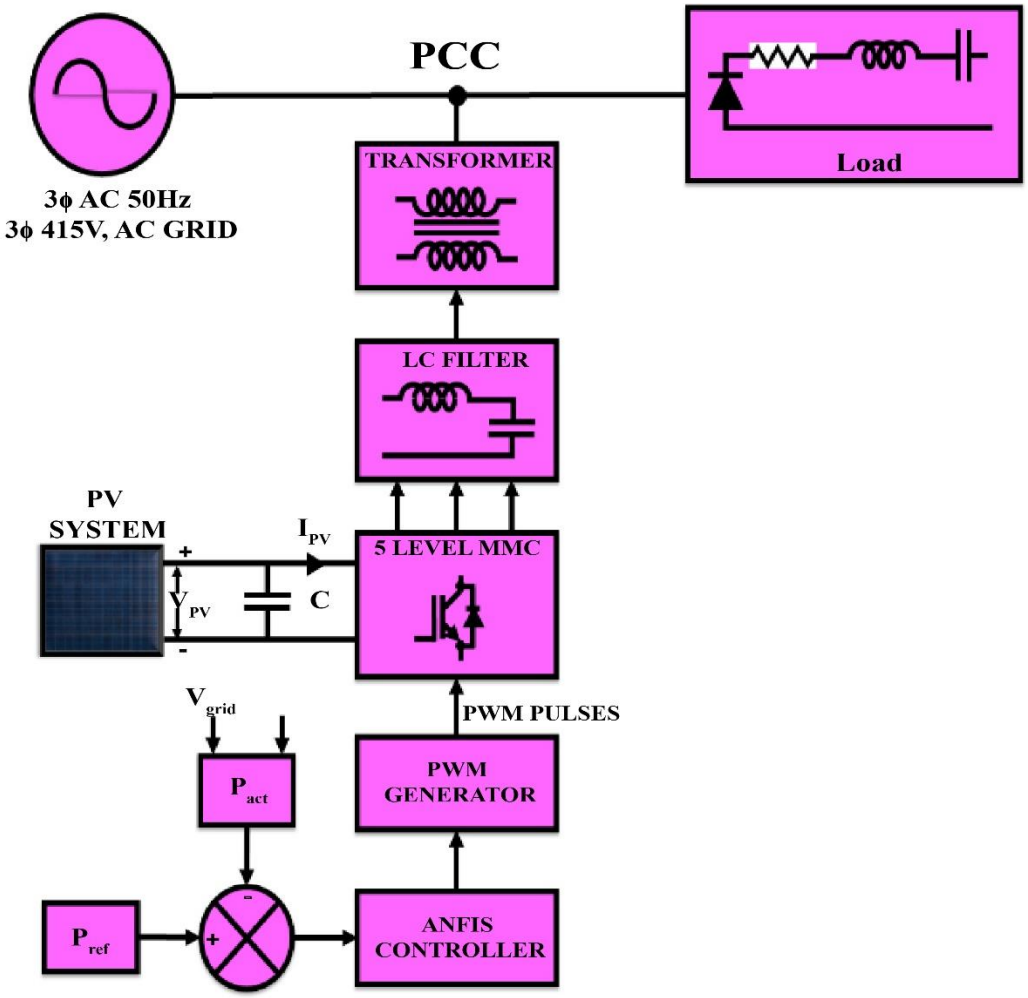


Fig. 1 Representation of control scheme

3. Modelling of Proposed System

3.1. PV Panel

Owing to the simplicity and precision, the single diode model with ohmic losses is commonly used to describe the electrical characteristics of the PV system. This system includes a current source, diode and series of parallel resistors, in which the current source is controlled by solar radiation. In Figure 2, a circuit model of this system has been illustrated.

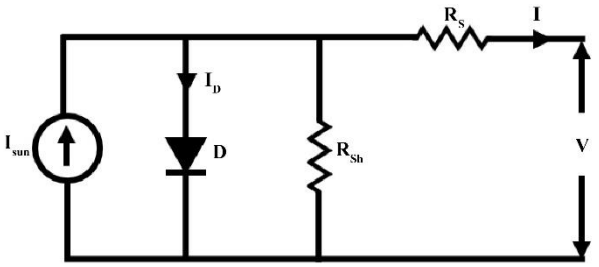


Fig. 2 An equivalent circuit of the Photovoltaic module

A terminal current in a cell is expressed as,

$$I = I_{sun} - I_o \left[exp\left(\frac{V+R_sI}{V_t\alpha}\right) + 1 \right] - \frac{V+IR_S}{R_{sh}} \quad (1)$$

The PV current produced by the sun is directly proportional to irradiance G, which is expressed as,

$$I_{sun} = \left(\frac{G}{G_{STC}}\right)\left(I_{sun-ref} + \Delta K_i T\right) \quad (2)$$

Where I_{sun} denotes the photocurrent of the PV cell, which is directly proportional to irradiance and temperature, I_o denotes the diodes inverse saturation current, V_t denotes the thermal voltage, which is expressed as $V_t = N_s KT/q$, R_s denotes the series resistance and R_{sh} denotes the shunt resistance.

3.2. Modular Multilevel Converter

A Modular Multilevel Converter (MMC) is certain for this study for its unique characteristics like high modularity and easy scalability. A MMC with $(2N + 1)$ voltage levels is generated by connecting a PV module with a capacitor and HBSM. Here, an MMC of five levels are utilized, and two SM are linked in each phase.

3.3. Operating Principle of the MMC

In a 3Φ MMC, each phase unit comprises two multivalves, and each multivalve contains N number of SM, which are linked in series, as illustrated in Figure 3. The HBSM contains two switches (T_1, T_2) and a capacitor C, which are associated in parallel, as illustrated in Figure 4. Under normal working mode, only one switch is turned ON, in which the direction of current flow is dependent on the charging or discharging of the capacitor. Depending on the current direction, neither the IGBT nor the freewheeling diode starts conducting when only one switch is turned ON. Three possible switching modes of MMC like $T_1\ ON$ or inserted mode, $T_2\ OFF$ or bypassed mode and blocked mode are performed as follows,

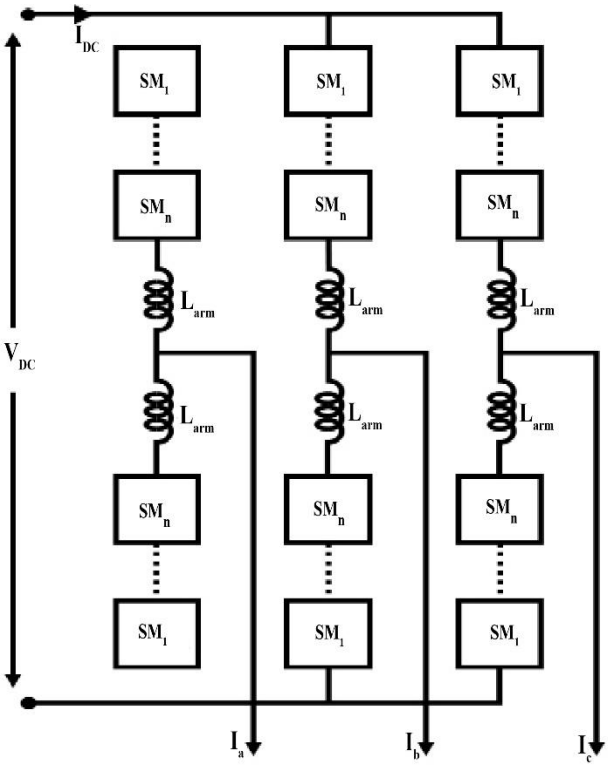


Fig. 3 Circuit layout of 3Φ MMC

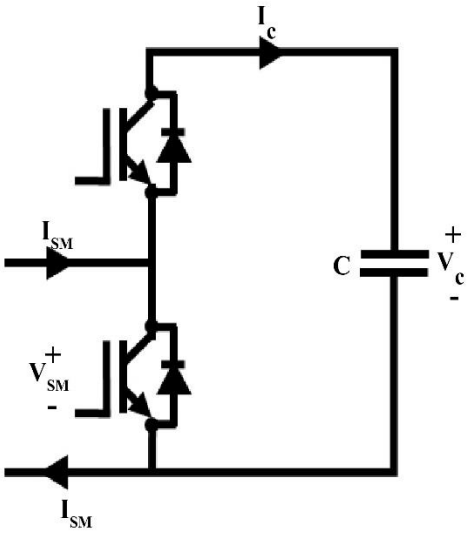


Fig. 4 Representation of submodule

- During the state of $T_1\ ON$, the switch T_2 is OFF. The output voltage of SM V_{SM} equalizes the capacitor voltage V_C and if the multivalve current is positive, it charges or discharges the capacitor.
- During the state of $T_2\ ON$, the switch T_1 is OFF. The output voltage of SM V_{SM} is equivalent to zero and capacitor voltage V_C is kept constant. Here the capacitor is neither charged nor discharged.
- During the blocked mode, the switches $T_1 and\ T_2$ are in OFF state, and so the freewheeling diode starts conducting. If the current is positive, the capacitor gets charged, but if it is ideal, the capacitor is not discharged.

3.4. Mathematical Modeling of the MMC

The converter with an infinite switching frequency and an infinite number of SM per multivalve is illustrated in Figure 5.

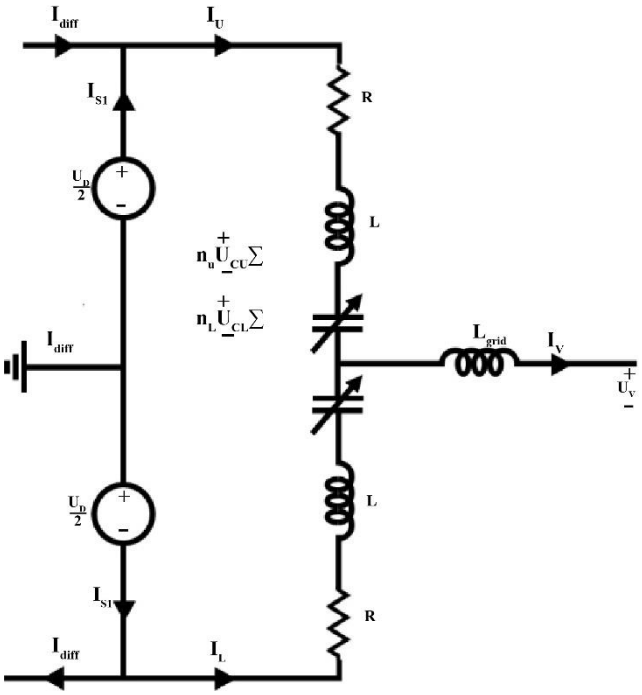


Fig. 5 Equivalent circuit of a phase leg

Apply KCL in the above circuit,

$$i_U + i_L = i_V \tag{3}$$

$$i_U = I_{s1} + i_{diff} \tag{4}$$

$$i_L = I_{s2} - i_{diff} \tag{5}$$

Where i_U denotes the current in the upper multivalve, i_L denotes the current in the lower multivalve, i_V denotes the output AC current, i_{diff} denotes the circulating current, i.e. $i_{diff} = \frac{i_U - i_L}{2}$.

Substitute equations (4) & (5) in (3)

$$i_V = I_{s1} + i_{diff} + I_{s2} - i_{diff} = I_{s1} + I_{s2} \tag{6}$$

The difference between the two multivalve currents is expressed as,

$$i_U - i_L = I_{s1} + i_{diff} - \left(I_{s2} - i_{diff}\right) = I_{s1} - I_{s2} + 2i_{diff} \tag{7}$$

If the converter contains N number of SM per multivalve, the bypassed N number of SM is defined as $n_m = 0$, the inserted N number of SM is defined as $n_m = 1$, and then the obtainable voltage in a multivalve m is expressed as,

$$U_{Cm} = n_m U_{C_m}^{\Sigma} \tag{8}$$

Where $U_{C_m}^{\Sigma}$ denotes the multivalve total capacitor voltage and $m = U, L$.

The sum of the two insertion indexes is equal to1, which is expressed as,

$$n_U + n_L = 1 \tag{9}$$

Where n_U denotes the upper multivalve insertion index on the range$[0, 1]$ and n_L denotes lower multivalve insertion index on the range$[0, 1]$.

Apply KVL in Figure 5,

$$\frac{U_D}{2} - n_U U_{C_U}^{\Sigma} - U_V - \left(Ri_{diff} + L\frac{di_{diff}}{dt}\right) - L_{grid}\frac{di_V}{dt} = RI_{s1} + L\frac{dI_{s1}}{dt} \tag{10}$$

$$-\frac{U_D}{2} + n_L U_{C_L}^{\Sigma} - U_V + Ri_{diff} + L\frac{di_{diff}}{dt} - L_{grid}\frac{di_V}{dt} = RI_{s2} + L\frac{dI_{s2}}{dt} \tag{11}$$

Assume,

$$I_{s1} = I_{s2} \tag{12}$$

Combine this assumption with $U_V = U_V$ in equations (11) & (12),

$$U_D - n_U U_{C_U}^{\Sigma} - n_L U_{C_L}^{\Sigma} = 2\left(Ri_{diff} + L\frac{di_{diff}}{dt}\right) \tag{13}$$

Where U_D denotes DC pole-to-pole voltage. The perfectly balanced case is denoted as $U_{C_U}^{\Sigma} = U_{C_L}^{\Sigma} = U_D$, which represents the circulation of current that is not perfectly balanced with the multivalve voltages. If the deviation from $U_D = 0$, the steady-state value of $i_{diff} = 0$.

Using equation (12) on equations (6) & (7), it is expressed as,

$$I_{s1} = I_{s2} = \frac{i_V}{2} \;\&\; i_{diff} = \frac{i_U - i_L}{2} \tag{14}$$

By using $\frac{U_D}{2} = \frac{U_D}{2}$ in equations (10) & (11), it is expressed as,

$$R(i_U + i_L) + L\frac{d(i_U + i_L)}{dt} + 2L_{grid}\frac{di_V}{dt} + 2U_V = n_L U_{C_L}^{\Sigma} - n_U U_{C_U}^{\Sigma} \tag{15}$$

The expression for

$$L' = \frac{L}{2} + L_{grid} \tag{16}$$

From Equation (3),

$$U_V = \frac{1}{2}\left(n_L U_{C_L}^{\Sigma} - n_U U_{C_U}^{\Sigma}\right) - \frac{R}{2}i_v - L'\frac{di_V}{dt} \tag{17}$$

The sum of capacitor voltages of the upper and lower multivalve is denoted by $U_{C_U}^{\Sigma}$ and $U_{C_L}^{\Sigma}$ respectively and U_V denotes output AC voltage.

From equation (17), it is noted that the U_V depends upon the output current i_V and the difference between two multivalves voltages is s $n_U U_{C_U}^{\Sigma}$ *and* $n_L U_{C_L}^{\Sigma}$. Here, the difference between $n_U U_{C_U}^{\Sigma}$ *and* $n_L U_{C_L}^{\Sigma}$ is regarded as inner alternating voltage, which is denoted as e_V.

$$e_V = \frac{1}{2}\left(n_L U_{C_L}^{\Sigma} - n_U U_{C_U}^{\Sigma}\right) \tag{18}$$

$$U_V = e_V - \frac{R}{2} i_v - L' \frac{di_V}{dt} \tag{19}$$

Equation (17) is rewritten in terms of the dq reference frame as well as the Laplace domain, which is expressed as,

$$v_d = e_{v_d} - \left(\frac{R}{2} + sL'\right) i_d - \omega L' i_d \tag{20}$$

$$v_q = e_{v_q} - \left(\frac{R}{2} + sL'\right) i_q - \omega L' i_q \tag{21}$$

Equations (20) & (21) are the output AC voltages in terms of the dq reference frame.

3.5. Modeling of Multicarrier PWM (MCPWM) Technique

To control M5LC, the MCPWM is used because of its easiness and simple instigation, and this control scheme minimizes the THD of output voltage. In M5LC, the MCPWM produces high-quality output waveform, and the carrier signals are generated based on level shifted and phase shifted with the carrier frequency of f_c. The carrier signals in the level shifted use triangular signals covering the range of the produced converter's output voltage, which has the same amplitude and frequency. A phase shift is implemented between carrier signals to enhance the converter's performance. The amplitude and time values are calculated using the following equations.

$$A_{k+1} = \sum_{k=1}^{(n-1)/2} A_k - \frac{4A_1}{n-1} \tag{22}$$

$$A_{k+1} = \sum_{k=(n+1)/2}^{n} A_k + \frac{4A_1}{n-1} \tag{23}$$

$$T_k = \frac{k-1}{(n-1)f} \tag{24}$$

Where k denotes any positive integer value.

3.6. Generation of Multicarrier Signals

By analogizing reference signals with carrier signals and gating pulses are produced. A modulating signal's peak-to-peak amplitude ratio A_{ref} to the peak to peak n number of the amplitude of carrier signals A_c is known as the amplitude modulation index m_a.

$$m_a = \frac{A_{ref}}{n\, A_c} \tag{25}$$

A ratio of required carrier signal frequency f_c to the frequency of modulating signal, f_m is known as the frequency modulation index m_f.

$$m_f = \frac{f_c}{f_m} \tag{26}$$

Control diagram for pulse generation has been illustrated in Figure 6. An analogization between the reference and carrier signals occurs at each period. Whenever a reference signal with positive carriers is greater than zero, the characters "1" or "0" are generated, whereas "-1" or "0" are obtained when it is higher than zero with negative transferors. The positive and negative sequence of pulses is expressed as,

$$P^{+} = \begin{cases} 1, & if\ M \geq C_r^{+} \\ 0, & if\ M < C_r^{+} \end{cases} \tag{27}$$

$$P^{-} = \begin{cases} -1, & if\ M \geq C_r^{-} \\ 0, & if\ M < C_r^{-} \end{cases} \tag{28}$$

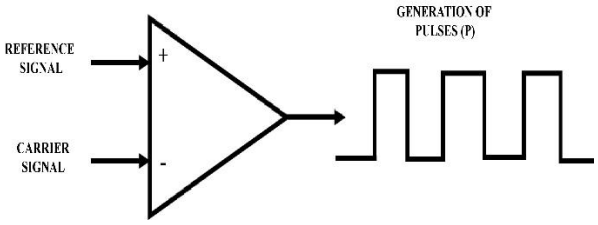


Fig. 6 Control diagram for pulse generation

The input of the comparator and the output signal is illustrated in Figure 7.

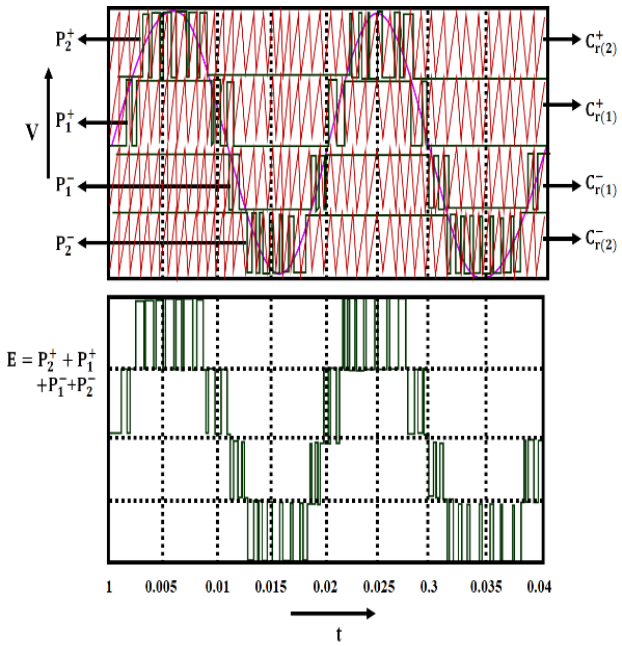


Fig. 7 The waveform of comparator input and output signals

The predicted output signal E is produced by adding the output signals of the comparator, and this E is utilized to operate the switch S. The logic switching modes of the switches are expressed as,

$$S = \begin{cases} 1 \; if \; E = k \\ 0 \; otherwise; where \; k = +(n-1)/2 \; to \; -(n-1)/2 \end{cases} \quad (29)$$

The M5LC switches are controlled by the pulses using a multi-carrier PWM approach, which reduces the THD of the converter's output voltage.

3.7. Modeling of ANFIS Controller

ANFIS, a combination of fuzzy and neural network approaches, produces a reference signal. An analogization of obtained signals with MCPWM carrier signals is performed to generate gating pulses of 3Φ VSI, which results in achieving the grid synchronization of the PV-tied grid system. The ANFIS has fast learning capacity and high accuracy in solving nonlinear or complex issues.

This method is a rule-based fuzzy logic, the rules created during the data-based training process. From the training samples of this process, the membership function variables of FIS in ANFIS are attained. Mamdani and Sugeno are the frequently used FISs, among which sugeno's output participation function is neither linear nor constant, whereas mamdani's output membership function is triangular, Gaussian, etc. Comparatively, the Sugeno-type FIS is more effective than the Mamdani-type FIS, so it is utilized in this study. The ANFIS Architecture is illustrated in Figure 8.

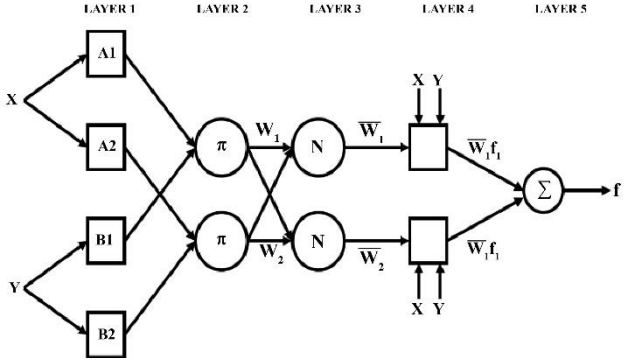


Fig. 8 ANFIS Architecture

Assume $x \; and \; y$ as two inputs to describe the architecture of ANFIS. The first-order fuzzy model of Sugeno has two fuzzy $if-then$ rules, which are stated as,

Rule1: If x is A_1 and y is B_1, then $f_1 = p_1 x + q_1 y + r_1$,

Rule2: If x is A_2 and y is B_2, then $f_2 = p_2 x + q_2 y + r_2$,

Where $A_i \; and \; B_i$ denotes the fuzzy sets, f_i denotes the output, $p_i, q_i and \; r_i$ denotes the variables of design, which are calculated during the process of training.

The ANFIS structure consists of five layers, which are described in the subsequent part, in which O_i^j denotes the output of the ith node and the jth layer.

***Layer* 1**: Each node denotes a node function, which is expressed as,

$$O_i^1 = \mu_{A_i}(x), \quad for \; i = 1,2 \quad (30)$$

Where x denotes the input to the ith node, A_i denotes the linguistic label, which is distinguished by the appropriate membership functions.

Layer* 2*: By means of multiplication, each node computes the firing strength of a rule, which is expressed as,

$$O_i^2 = w_i = \mu_{A_i}(x) * \mu_{B_i}(y), \quad i = 1,2 \quad (31)$$

***Layer* 3:** The previous layer's firing strengths are normalized to differentiate the firing strengths of each rule from whole firing strengths of whole regulations, which is expressed as,

$$O_i^3 = \overline{w_i} = \frac{w_i}{w_1 + w_2}, \quad i = 1,2 \quad (32)$$

Layer* 4*: A contribution of ith rule to the overall output is computed by node i, which is expressed as,

$$O_i^4 = \overline{w_i} * f_i = \overline{w_i}(p_i * x + q_i * y + r_i) \quad (33)$$

Layer* 5*: The overall output is computed by the single node as the whole contribution from each rule, which is expressed as,

$$O_i^5 = \sum_i \overline{w_i} * f_i = \frac{\sum_i w_i * f_i}{\sum_i w_i} \quad (34)$$

Thus, using ANFIS, grid power is controlled by the generation of 3Φ VSI gating sequence and reduces the THD.

3.8. Modeling of Three-phase Grid Synchronization

The output of 5-level MMC is attained as a constant DC voltage, which is converted into AC through a 3Φ VSI. A structure of a three-phase grid-connected VSI has been demonstrated in Figure 9.

ANFIS controller generates three-phase VSI gating pulses and controls grid power. Voltage, frequency and phase angle are the major factors in the process of attaining grid synchronization. In a 3Φ system, the phase-locked loop (PLL) is normally installed in a synchronously rotating reference frame (SRF) to simplify the structure of the loop filter. The use of SRF PLL prevents nonlinear loads from causing variations in the grid voltage. For an estimation of grid voltage, it yields phase angle and accurate frequency. Thus, it results in grid synchronization and a decrease in THD.

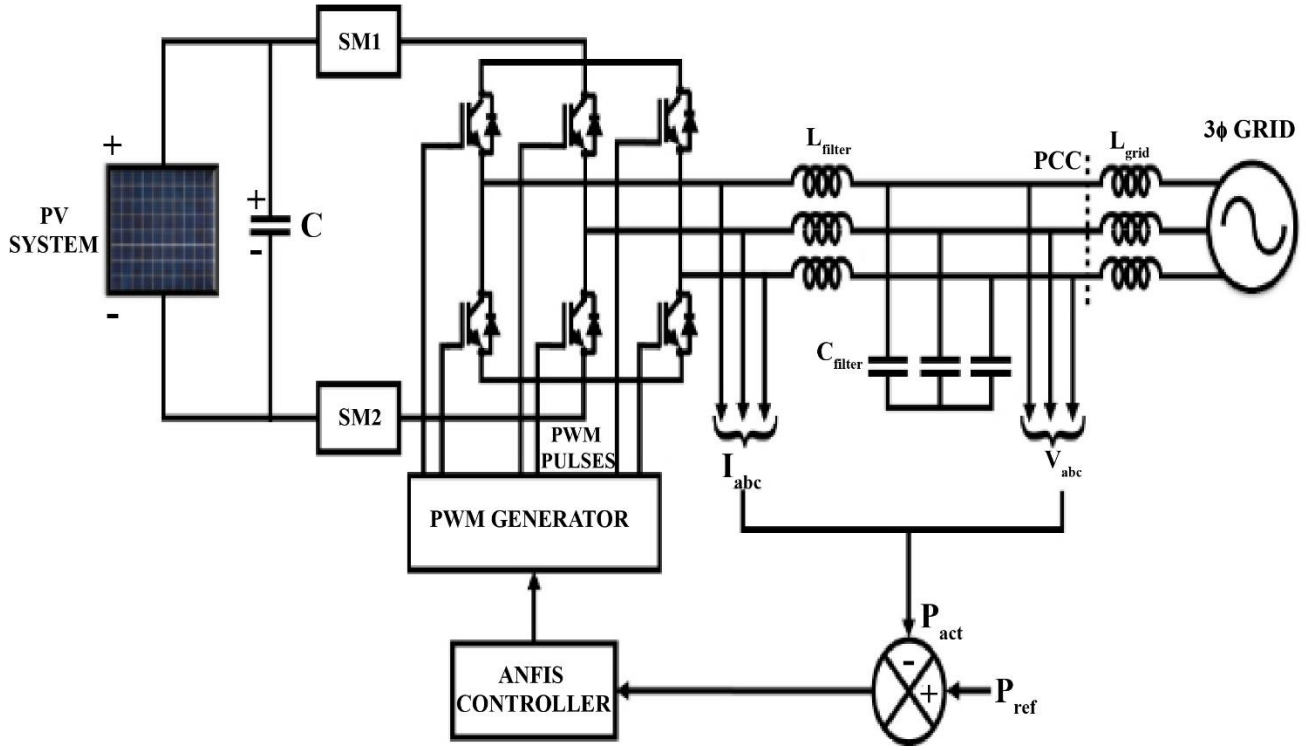


Fig. 9 3Φ grid connected VSI

3.9. Modeling of LC Filter Design

A 5% phase current at rated power AC current ripple and inductance on the inverting input are selected to build an LC filter. The voltage across an inductive filter is also 0 when the grid current is considered to be zero, which is expressed as,

$$V_L = V_{inv} - V_g \tag{35}$$

Where the voltage across the inductor is depicted as V_L, an output voltage of the inverter is represented as V_{inv} and V_g denotes the grid voltage.

A grid frequency f_N is lesser than switching frequency f_s and so the phase voltage depends on the switching frequency f_s. During switching time T_s, the normal value of inverter output voltage V_{av} is described as constant. With the utilization of the phase disposition PWM switching technique, peak to peak filter inductor current value (I_{pp}) has been expressed as,

$$\Delta I_{pp} = 2I_{rpm} = \frac{\frac{V_{dc}}{2} - V_{av}}{L_f} \cdot \frac{d_1}{f_s} \tag{36}$$

Where, the filter inductance is denoted as L_f and the duty cycle is denoted as d_1. During the interval $0 < \omega t < \pi$, it is expressed as,

$$V_{av}(\omega t) = d_1(\omega t)\frac{V_{dc}}{2} \tag{37}$$

$$d_1(\omega t) = m_a sin(\omega t) \tag{38}$$

Where the modulation index is denoted as m_a.

The maximum inductor current ripple I_{rpm} is expressed as

$$I_{rpm} = \frac{V_{dc}}{4L_f f_s}[1 - d_1(\omega t)]\, d_1(\omega t) = \frac{V_{dc}}{4L_f f_s}[1 - m_a sin(\omega t)] m_a sin(\omega t) \tag{39}$$

Assume $m_a = 1$, at $\pi/6$, $5\pi/6$, a maximum value of I_{rpm} is obtained as $1/4$.

$$L_f = \frac{V_{dc}}{16 f_s \Delta I_{ph(max)}} \tag{40}$$

Thus a value of the inverter side inductor is chosen based on the switching frequency.

To choose a filter's capacitance, a power factor fluctuation that may be observed by a grid must be set at 5%. An overall system impedance base (Z_B) is determined from a capacitance variation specified as,

$$Z_B = \frac{v_G^2}{P_{AV}/3} \tag{41}$$

$$C_B = \frac{1}{\omega_N Z_B} = \frac{1}{2\pi f_N Z_B} \tag{42}$$

Where line-to-line rms voltage has been denoted as v_G, active power as rated is indicated as P_{AV} and frequency of the grid is signified as ω_N.

4. Results and Discussions

In this present study, the reference signal is generated by the ANFIS controller, and M5LC has been employed to ameliorate the fluctuating output of PV. The carrier signals

of MCPWM, which are used to produce gating sequences for both the converter and inverter, are analogized with generated signal presently represented. With the utilization of the ANFIS controller, the M5LC is controlled, and the DC voltage is retained as constant. The three-phase VSI, which synchronizes a grid by converting DC to AC voltage, transmits the DC output of M5LC to the grid. MATLB software has been employed to simulate the suggested control method. In Table 1, the suggested system's specifications are described.

Table 1. Specifications of the proposed system

Components	Ratings/specifications
No. of panels	15
Sum of series cells	36
Area of the cell	125mm × 31.25mm
Range of temperature	-40 to 85° C
Maximum Voltage	1000 V
Operating Voltage	16.8 V
Operating Current	5.8 A
LC Filter	4.5mH/10μF
Frequency of Swithching	20KHz
Grid frequency	50Hx

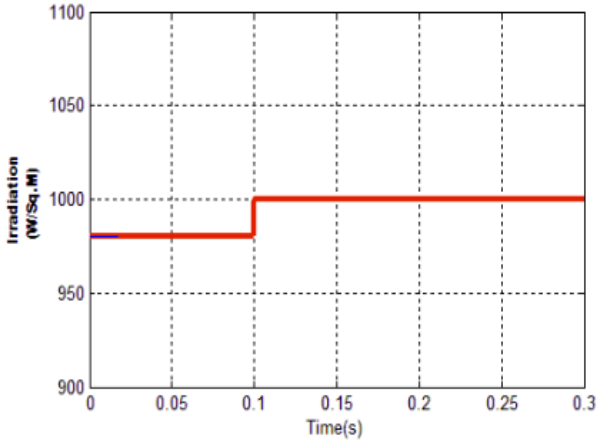
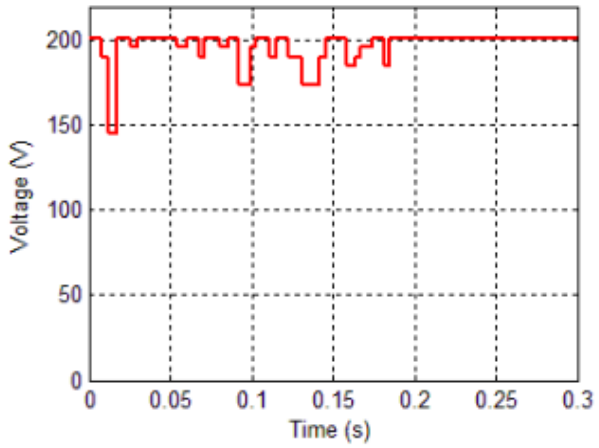
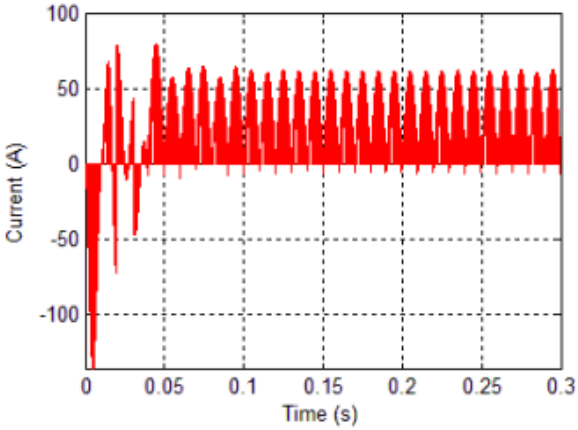


Fig. 10 Solar irradiation waveform



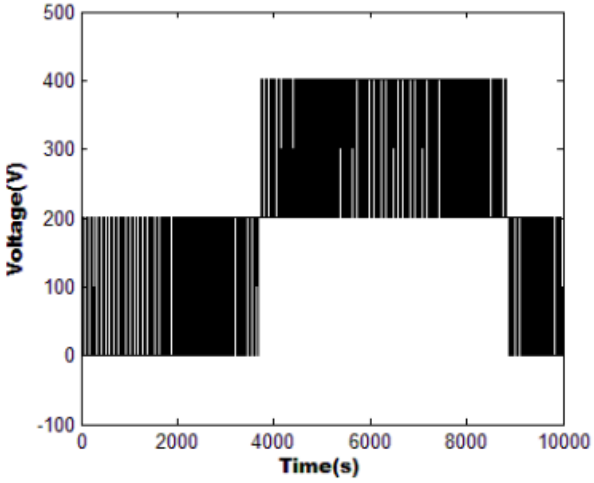
(a)



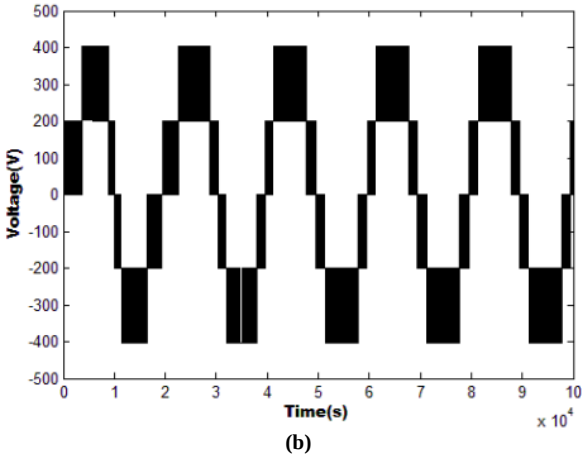
(b)

Fig. 11 Waveforms for (a) Photovoltaic panel voltage, (b) Current of Photovoltaic panel

A waveform of solar irradiation is depicted in Figure 10. Due to temperature fluctuations, initially, irradiation was set at $980\,W/m^2$ during a time period $0\ to\ 0.1\ s$ and after $0.1\ s$, irradiation reaches $1000\,W/m^2$.



(a)



(b)

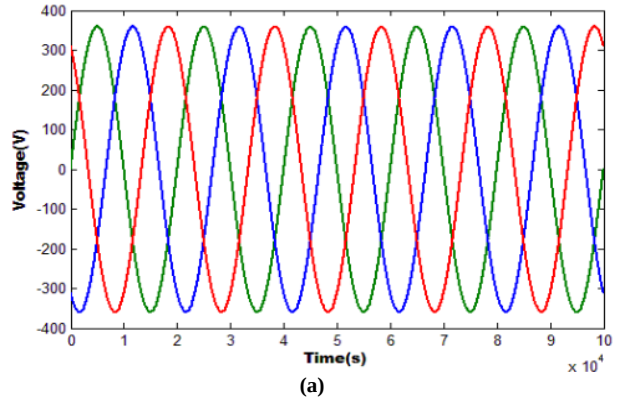
Fig. 12 (a) The voltage waveform of the MMC low-frequency converter (b) Voltage waveform of the MMC high-frequency converter

According to Figures 11, (a), and (b), voltage and current waveforms of a photovoltaic panel have been exhibited correspondingly. A waveform is a clear voltage

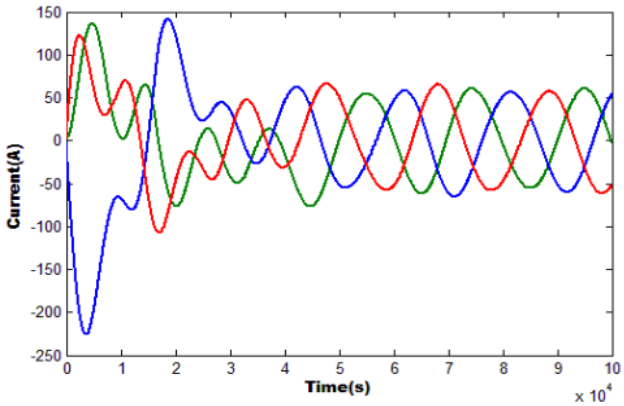
that is in a fluctuating state in the beginning, but after the time of $0.18s$, it remains constant at the voltage of $200V$.

The Voltage waveforms of low and high-frequency MMC converters are presented in Figure 12 (a) & (b). The voltage achieved for the MMC LF converter ranges from $0\ to\ 400V$. For the MMC HF converter, the voltage has been obtained between $0\ to + 400V\ \ and\ \ 0\ to - 400V$. It consists of five levels, among which 2 levels are positive, 2 levels are negative side, and 1 level is zero.

Considering Figure 13 (a) and (b), voltage and current in an inverter have been depicted, respectively. After 4 seconds, harmonics are eliminated with the support of M5LC, as shown in the current waveform, after the harmonics had initially appeared.

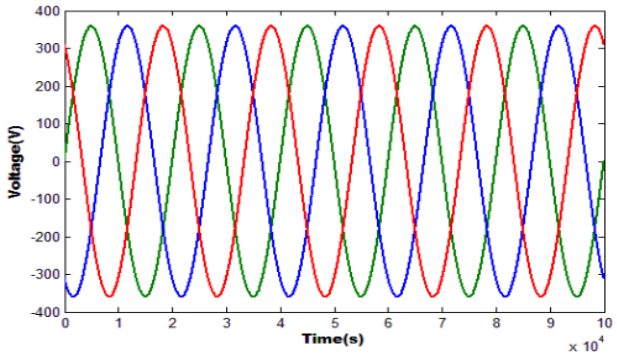


(a)

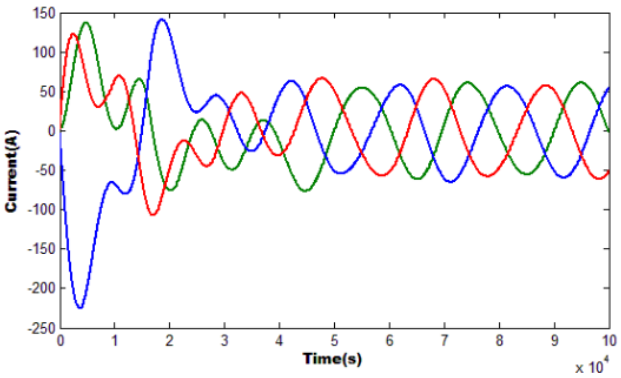


(b)

Fig. 13 (a) Inverter voltage waveform (b) Current waveform of the inverter



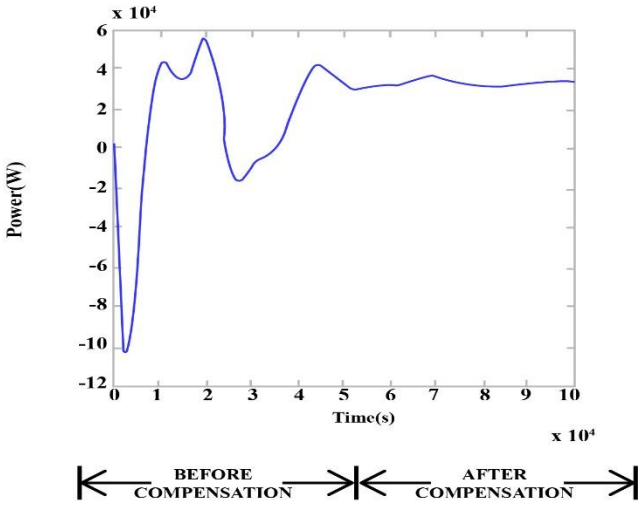
(a)



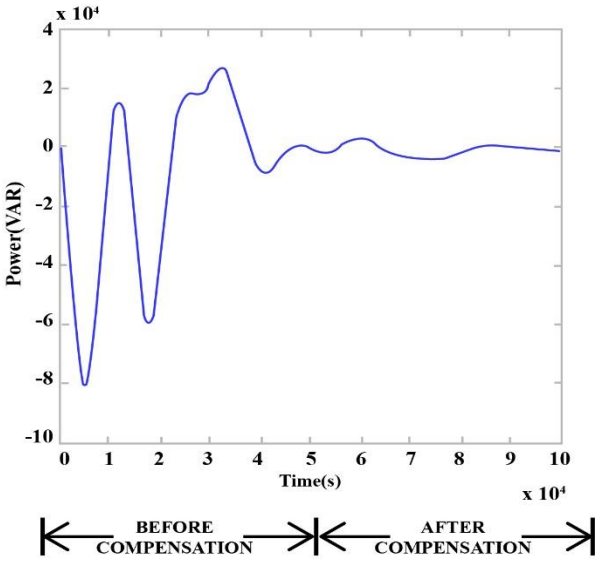
(b)

Fig. 14 (a) Grid voltage b) current waveform

Considering Figure 14 (a) and (b), grid voltage and current have been shown. A waveform included harmonics at an early stage, but after 4 s, the harmonics were removed using the M5LC technique and transformed to sinusoidal.



(a)



(b)

Fig. 15 (a) Real and (b) Reactive power waveform

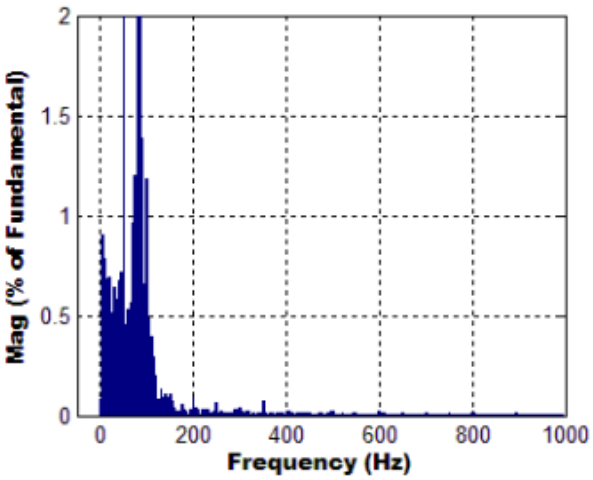


Fig. 16 Grid current THD using ANFIS controller

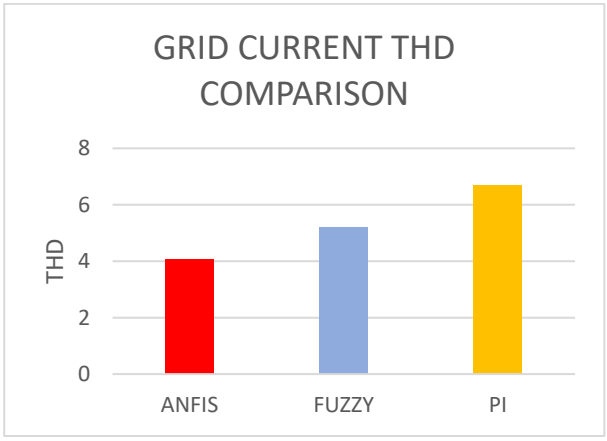


Fig. 17 THD comparisons for grid current

In Figure 15 (a) & (b) a, real and reactive power waveforms have been demonstrated. Both waveforms initially exhibit a fluctuation, which is eliminated by using the M5LC-based ANFIS controller. As shown in the graph, the compensation occurs after the time of 5 *s*.

ANFIS controller has been employed to depict a grid current THD. Considering Figure 16, the grid current THD for the ANFIS controller is 4.07%.

In Figure 17, grid current THD is illustrated for comparison. As shown in the comparison, an ANFIS performs better than Fuzzy and PI controllers with a low THD for grid current of 4.07%.

5. Conclusion

This paper explains an M5LC-based grid-integrated PV system with enhanced PV module voltage. The proposed converter is controlled by the MCPWM technique, which retains the DC voltage as constant. ANFIS controller generates a reference signal compared to an MCPWM carrier signal. DC output of the converter is converted into AC voltage with the assistance of 3Φ VSI and then given to the grid, through which the grid synchronization and reactive power compensation are achieved. ANFIS performs better when the grid current THD is less than 4.07%. The proposed control scheme is validated through MATLAB software.

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