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Original Article

Temperature Effects in a Power RF LDMOS Device Performance Due to Hot Carrier

Mohamed Ali Belaid [1,2]

[1] *Umm Al-Qura University, College of Engineering Al-Leith, Makkah, Electronics and Communication Engineering Department, P.O. Box 715, 24382 Makkah, Saudi Arabia*
[2] *Université de Sousse, Ecole Nationale d'Ingénieurs de Sousse, LATIS- Laboratory of Advanced Technology and Intelligent Systems 4023, Sousse, Tunisie*

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Abstract *- Thermal constraints special in high-temperature levels, is the most observed degradation mechanisms in power RF electronic devices. To evaluate the degradation level, the main indicator may be the measurement of on-state resistance (R_{DS-on}), which is systematically associated with the evolution of the internal device structure. This evaluation of thermal constraint's effects on I-V characteristics of power RF N-LDMOS devices, especially of R_{DS-on} resistance, is the main constraint of LDMOS devices in high-temperature operations that can partially or change the performances of physical and electrical devices. R_{DS-on} is highly dependent on temperature. The parameters relevant to the temperature evaluation characterization of the device are reported and proven by the basic physical behavior. The experimental results analysis is presented and used to explain the physical preview of temperature impacts on power RF LDMOS performance. The physical parameters like current lines, concentration, and mobility are considered, following temperature dependence. Finally, initial impacts analysis is discussed.*

Keywords *- Reliability, R_{DS-on} resistance, Power RF LDMOS, Temperature effects, Hot carrier.*

I. INTRODUCTION

Metal Oxide Field Effect Transistors (MOSFETs) are the most widely used active devices in the high power RF field. The cost of MOSFETs represents a clear advantage over III-V technologies for application rates up to around 4 GHz. The semiconductor behavior is delicate to temperature evaluation, especially the power RF devices [1-2-3]. Thermal effects are still the principal cause of degradation in most cases. The temperature affects important variations in electrical behavior and has a huge effect on reliability, conducting partial degradation or total. It limits the lifetime and plays an important role in many degradation processes of semiconductors.

Coming from the widely tested and mastered silicon industry, it is an adaptation of basic MOSFET developed for radio frequency power applications. In addition to its low manufacturing cost, the LDMOS transistor has all the electrical and thermal characteristics required for complex modulations because of its frequency, thermal stability, and good linearity. The exceptional linearity of the LDMOS transistor places it as the best candidate to meet the stringent requirements of the mobile phone standards. This technology significantly reduces power consumption and thermal problems in base stations, thus increasing power density by 50%, efficiency by 6-8%, and power gain by 2 dB compared to other technologies [4]. When a current is passed through the drain in a MOS transistor, the power is absorbed in the channel region and heating in the channel sector. The current increase is due to high dependence and irregular temperature inside the transistor [5-6]. Important studies are made to increase the breakdown voltage and decrease the ON resistance, with proof and physical explanation [7-8], making it a suitable candidate for high-voltage and power integrated circuit (IC) applications. In on state (linear region), the MOSFET can be considered a resistor, and the R_{DS-on} is the resistance between drain and source when this one is in on state. This resistance is one of the important characteristics of power RF MOSFETs. The main challenge in development is to reduce this resistance to limit the self-heating and the voltage drop in the on state [1-3-6].

This study is presented in the following way: the experimental characterization of power N-LDMOSFET is detailed in part 2. The results discussion is represented in part 3. The conclusion and prospects are cited in part 4.

II. EXPERIMENTAL CHARACTERIZATION OF POWER N-LDMOSFET

The characterization should be as possible and hold climatic constraints to account (humidity, temperature, etc.). The IC-CAP (Integrated Circuit-Characterization and Analysis Program) software interface is used for the measuring instruments to guarantee this characterization method. This part describes the main static characteristics I-V of the Power RF LDMOS. This measurement type aims to evaluate the device quality and study their behavior in the various operating modes (linearity, saturation). However, obtaining a certain number of inherent parameters (channel current, threshold voltage, transconductance, on-state resistance, etc.) will be among the main criteria for failure analysis. This section performs all measurements on transistors of power RF technology N-channel. The experimental bench includes an Agilent E5270 DC analyzer (maximum output power: 20 Watts), driven by IC-CAP software and a Peltier effect module regulated in temperature (0 °C to 200 °C) controlled by a BILT chassis, all linked by GPIB bus to a control PC (see Fig.1). The device under characterization was placed on a thermal module by a contact fixing screw with an interstitial fluid (conductive silicone grease) to maintain a constant temperature. The command unit pipe DC supply temperature regulation and voltage.

The most important electrical parameter in the Ohmic region is a zone where the drain-source current I genuine growing depending on drain-source voltage V_{ds}. The $R_{DS\text{-}on}$ resistance of a power MOS transistor is defined as the total resistance between the source and drain when the transistor is operating in a linear (see Fig.2-a), low-drain-source voltage regime when this same voltage tends to zero. The ratio calculates the value:

$$R_{DS-on} = (V_{ds}/I_{ds})_{Vds \to 0} \qquad (1)$$

The $R_{DS\text{-}on}$ resistance value depends on the channel opening; it is generally measured for gate voltages. The channel is fully open, so one is at the saturated value. Fig.2-b shown $R_{DS\text{-}on}$ decreases vs. gate voltage increases. The resistance is very high for V_{gs} values below the V_th, which avoids passing a current below the threshold; the transistor is completely blocked.

III. RESULTS ANALYSIS AND DISCUSSION

The degradations created by temperature are not the only causes of defects during the device operation. On the other hand, thermal phenomena are still the principal cause of failures in most cases. The study targets the $R_{DS\text{-}on}$ evaluation of power RF MOSFET devices with temperature effects and physic impact. The $R_{DS\text{-}on}$ is the total resistance that appears between drain and source when the transistor is linear operation (low source-drain voltage). It is mainly the sum of two components: the drift zone resistance R_{Drift} and the inversion channel resistance R_{ch} (see Fig.3).

$$R_{DS-on} = R_{ch} + R_{Drift} \qquad (2)$$

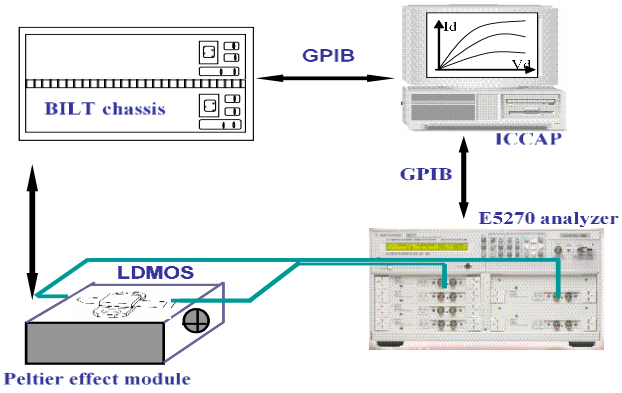
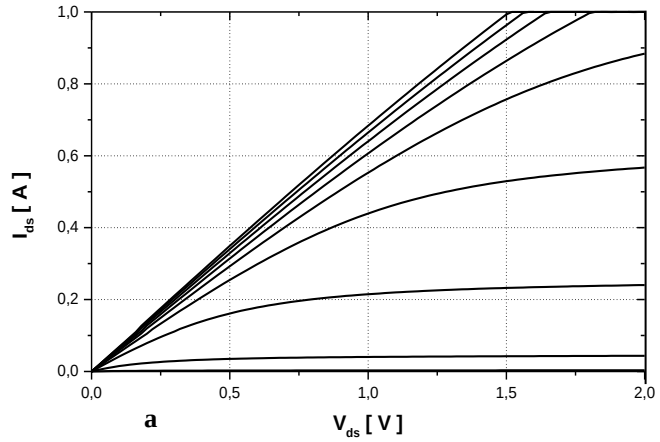


Fig. 1 Bench of the measurement of the I-V parameters



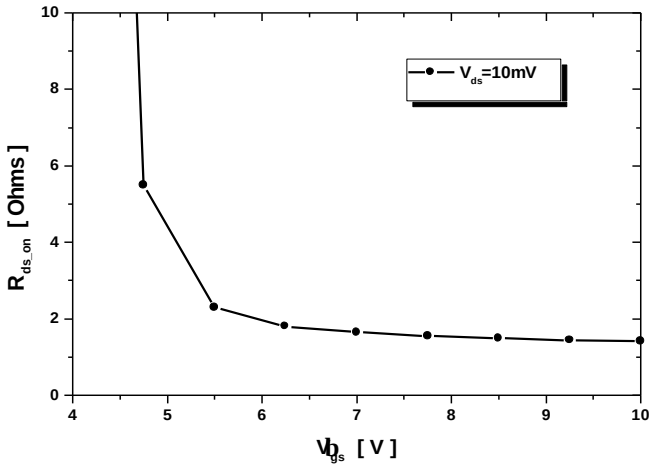


Fig. 2 The experimental $R_{DS\text{-}on}$ resistance: (a) Slope from the I_{ds} vs. V_{ds} in Ohmic part, V_{gs} [3;10V], step=1V, (b) Experimental variations vs. V_{gs} voltage

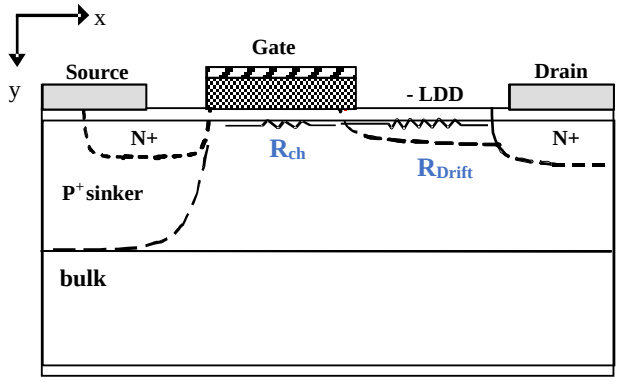


Fig. 3 Cross-section view of RF LDMOSFET with various components of $R_{DS\text{-}on}$ resistance

The inversion channel resistance (R_{ch}) depends on the geometrical data, the temperature, and the source gate bias, which is adjusted by the following relation [9]:

$$R_{ch} = \frac{L}{W\mu_{EFF}(T)C_{OX}(V_{gs}-V_{th}(T))} \quad (3)$$

The R_{Drift} is the resistance of the N-type weakly doped zone. It is a function of the drain polarization: when the drain voltage increases, the channel resistance depends mainly on the gate voltage, while the R_{Drift} resistance depends on the drain voltage. This dependence results in a limitation of the carrier's speed in the drift zone due to the strong electric field and the zone's short length. When the field is higher, the carrier mobility is lower, which decreases the area resistive behavior, and therefore, the resistance weight becomes significant compared to other resistive components. The model developed for this voltage-controlled resistor is calculated by writing the current unidimensional equation in the drift zone [9]:

$$I_{ds} = q.\mu.n.S.\frac{dV}{dy} \quad (4)$$

Where q is the elementary electron charge, μ is the electrons mobility in the drift zone, S is the zone considered section, n is the electrons density, V is the potential, and dy is an elementary portion in the longitudinal structure direction. By integrating the current expression over the length of the drift zone and the potential difference at its terminals, to deduce the expression following the drift resistance [9]:

$$R_{Drift} = R_{d0} + K(V_{ds} - V_1) \quad (5)$$

Where V_{ds}-V_1 is the potential difference across the drift zone and K is a constant. The term R_{d0} mainly depends on the drift zone length, doping, and resistance, a linear function of the source-drain voltage. The linear current is the Ohmic regime of output characteristic I_{ds} vs. V_{ds}, as shown in Fig.2-a. This region is described by the relation below; when a drain bias is applied in such a way that $V_{ds} < V_{ds\text{-}sat}$, then:

$$I_{ds} \approx \frac{W}{L}\mu_{EFF}C_{OX}[(V_{gs}-V_{th})V_{ds} - \frac{V_{ds}^2}{2}] \quad (6)$$

With μ_{EFF}, the carrier's mobility of the conduction channel [9]:

$$\mu_{EFF} = \frac{\mu_0}{\left[1+\frac{|E_X|}{E_C}\right]\left[1+\frac{|E_Y|}{E_0}\right]} \quad (7)$$

In these expressions, W and L are the width and length of the conduction channel. C_{OX} is the gate oxide capacity, μ_0 is the low-field electron mobility, E_X and E_Y represent the transverse and longitudinal components of the electric field, E_C is the transverse critical field, and E_0 is the longitudinal critical field value beyond which the electron velocity saturation is observed. The equation (7) can also be written as [10]: which highlights the temperature dependence of the conduction channel mobility:

$$\mu_{EFF}(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m} \quad (8)$$

For the LDMOS device, m = 2.5, which leads to a temperature dependence of electron mobility in the conduction channel of the $T^{-2.5}$ form. The LDMOS experiences a greater reduction in carrier mobility at a higher temperature than CMOS. In comparison, CMOS mobility follows a $T^{-1.5}$ type law [9]. Fig.4 shows that the I_{ds} at low current levels vary linearly with temperature. This is due to the reduction of the threshold voltage.

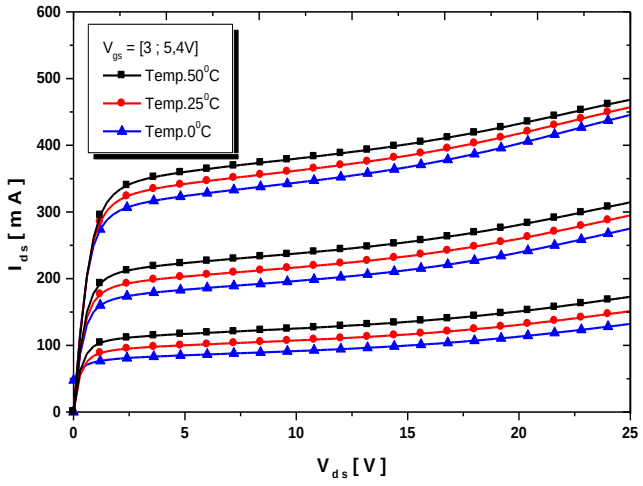


Fig. 4 Variation of channel current with different temperatures

The threshold voltage V_{th} corresponds to the source gate voltage value, from which the transistor begins to conduct (formation of the inversion channel allowing the current flow between drain and source). In other words, the zone where

the acceptor impurity concentration is the highest imposes the threshold voltage, which corresponds to the maximum doping value N_{max}. In the LDMOS case, the highest concentration is in the conduction channel. This one is given by [9]:

$$V_{th}(T) = \emptyset_{ms} + 2\emptyset_f + \frac{\sqrt{2\varepsilon q N_{max}(x)(2\emptyset_f)}}{C_{ox}} - \frac{Q_{ox}}{Q_{ox}} \quad (9)$$

The temperature dependence of (9) comes principally from the Fermi potential that is written as

$$\emptyset_f = \frac{KT}{q}\ln\left(\frac{N(x)}{n_i(T)}\right) \quad (10)$$

The V_{th} is an electrical parameter depending on the temperature. In these relations, ϕ_f is the Fermi potential, ϕ_{ms} is the difference of output work between the metal and the semiconductor, ε is the silicon dielectric constant, kT/q is the thermodynamic unit, and n_i is the intrinsic concentration. The temperature dependence of the n_i (intrinsic concentration) is written by [9-11]:

$$n_i(T) = 3.87x10^{16}T^{3/2}e^{-E_g/2kT} \quad (11)$$

The energy gap variation with the temperature is low and does not consider the error introduced with E_g, which is independent of temperature [10]. The evolution of the DMOS threshold voltage vs. temperature is met by grouping (9)-(11) and differentiating, which gives:

$$\frac{dV_{th}}{dT} = \left[\frac{\emptyset_f}{T} - \frac{K}{q}\left(\frac{E_g}{2KT} + \frac{3}{2}\right)\right]\left(2 + \frac{\sqrt{2\varepsilon q N_{max} 2\emptyset_f}}{2\emptyset_f C_{ox}}\right) \quad (12)$$

The V_{th} as a function of physical and technological parameters of MOS shows that it decreases with temperature (Fig.5). This variation is linear vs. the temperature and can be shown below by [9]:

$$V_{th}(T) = V_{T0} + (V_{tT}T_j) \quad (13)$$

T_0 is the ambient temperature, V_{T0} is the threshold voltage at T_0, V_{tT} is the equation coefficient, and T_j is the junction temperature. Fig.6 plots the measured threshold voltage of a typical n-channel LDMOS device over 20-150 °C. The V_{th} evolution is linear: but decreases when the temperature increases (see Fig.6).

The $R_{DS\text{-}on}$ is defined by the linear drain current (Eq.1) and is inversely proportional, so the resistance in the on state decreases as the gate voltage increases, shown in Fig.7-a, which plots the measured on-state resistance of the LDMOS structure in Fig.3. At large V_g corresponding to strong inversion, the mobility effects dominate, and (Eq.2) - (Eq.3) predict an increase in on-state resistance with temperature (see Fig.7-b). The parameter $R_{DS\text{-}on}$ depends on distribution and heat dissipation, which represents the flow of heat inside the transistor [5-12]. The numerical simulations were performed in a power LD-MOSFET structure to analyze the thermal behavior and effects. With physical simulation and the drifts analysis of the electrical quantity's evolutions, in terms of the applied temperature, the relationship between the electrical parameters shifts and the main physical mechanism is clarified.

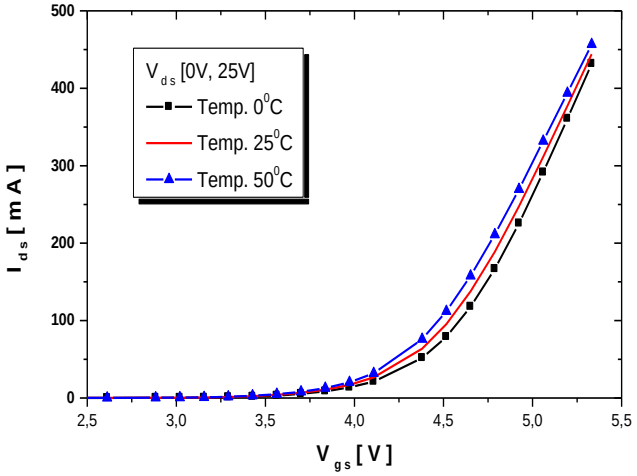


Fig. 5 Temperature influence on the threshold voltage V_{th}

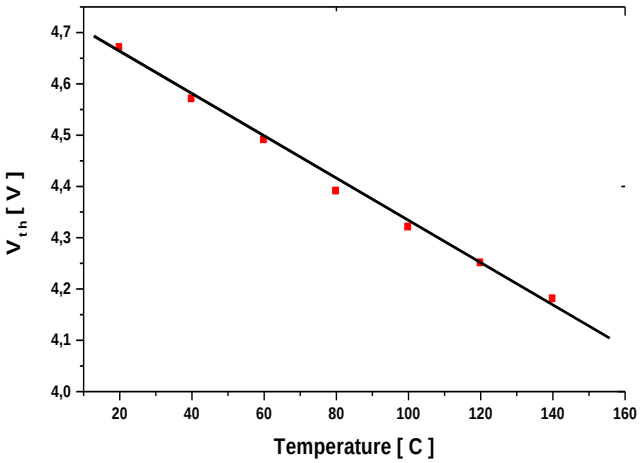


Fig. 6 Variation of n-channel LDMOS threshold voltage with temperature

Enough high electric field in the space was charging region causes electron pairs holes by shocks between the carriers and the crystal lattice [12]. This leads to a doubling of the carrier number, and thus a strong current is generated. Indeed, for operation in extreme values of voltages and currents, a thermo-electric feedback mechanism can tighten the current at localized hot spots [12-13]. This phenomenon changes the performance or destroys the device. Although this phenomenon is well known for MOSFETs, its consideration for LDMOS has become essential due to the use of the latter in RF power applications. Knowing the

temperature distribution inside the structure in the drift area is necessary to identify local "hot spots ."The dissipation power in the drift area was located in a manner non-uniform distribution [5-11]. Because the breakdown voltage effect can lead to thermal runaway [2-3-9] if the rise of channel temperature is superior enough. The temperature rise due to self-heating takes inside the power LDMOS active zone, degrading the electrical device behaviors and finally modifying the performance to a considerable extent [13]. The I-V parameters shift due to the modification of physical properties addition, particularly affecting the $R_{DS\text{-}on}$.

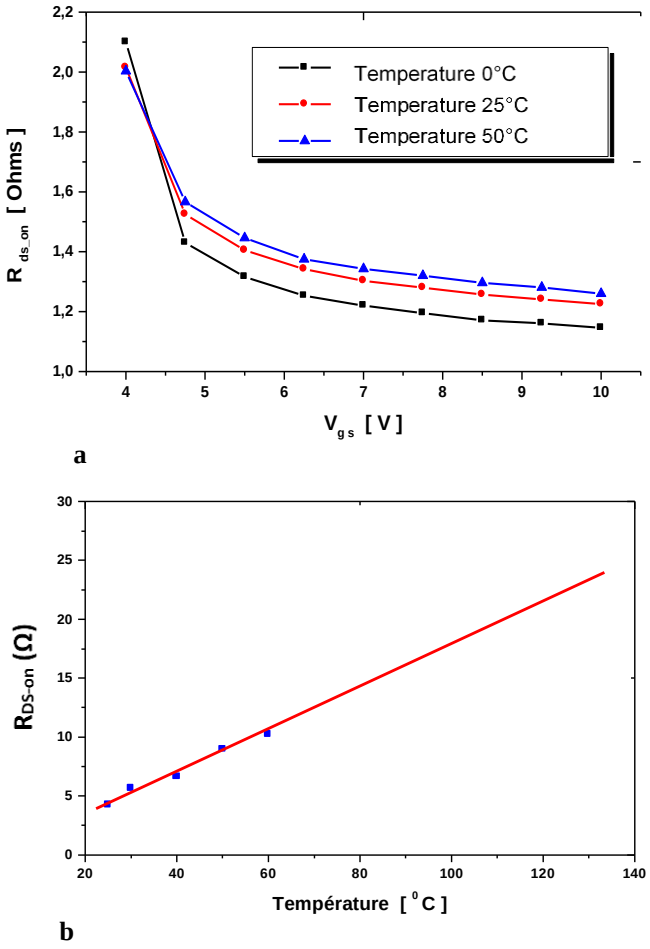


Fig. 7 Variations of $R_{DS\text{-}on}$ resistance of a power RF N-LDMOS: (a) vs. V_{gs} voltage at different temperatures, (b) according to temperature

The temperature rise increases the drain current due to the reduced threshold voltage in the low current area. It is reduced due to the effective mobility deterioration in the high current area [2]. The parameters evolve to the level electric field, which increases the carrier injection ingrown silicon dioxide layer (SiO_2) and in interface state Si/SiO_2 [13-14-15]. The current flow lines are located most of the percentage along and below the $Si\text{-}SiO_2$ interface. It is noticed that the concentration is very high at the gate level, at the right side of the drain, when providing a way for a major increase of the surface current density at the gate edge [14-15].

The presence of an intense electric field under gate oxide by a peak in area LDD [1-3-5] and a high electrons concentration at the SiO_2/LDD interface [3-5] contributed to the appearance of hot carriers generated by impact ionization [5-9]. For these test conditions (polarization, temperature, etc.) provided, all advantages are consistent with the degradation caused by the hot carriers. As the congestion of current lines is greater at low temperature at the SiO_2 / LDD interface, many electrons accelerate to high velocities through this high electric field peak [5-11]. The origin of the observed shift is related to a very high electric field that increases carrier injection into the grown silicon dioxide layer (SiO_2) and into the interface state Si/SiO_2 [1-5-10]. The impact ionization degradation effects are closely related to current density. With the largest number of free electrons in the silicon oxide area, most electrons are quintessence deep inside the drift region [5-10-16]. Then results in accumulating a negative charge at the $Si\text{-}SiO_2$ interface [3-10-17].

Therefore, this high electric field peak [1-5-16]. So, they become energized and must be accelerated away from their normal flow. The analysis of relevant electrical parameters (I_{ds}, V_{th}, G_m, $R_{DS\text{-}on}$) strongly correlated to a structural zone, allowing us to locate the degradation area and distinguish the prevailing degradation mechanism, which happens to be at interface SiO_2/N-LDD. The latter is the failure phenomenon by the hot carrier's

IV. CONCLUSION

An Analysis of temperature dependence on the $R_{DS\text{-}on}$ of power RF LDMOS transistors has been presented. The results highlighted that $R_{DS\text{-}on}$ is sensitive to temperature and rises with it, and the foundation of these shifts is related to the physical behavior degradation. The threshold voltage decreased monotonically with temperature, while I_{ds} current and $R_{DS\text{-}on}$ resistance have increased with temperature. These results show consistency with experimental and physical results and reflect that temperature effects are the main reason for failure in most cases. The LDMOS electron concentration distribution and mobility exhibit a temperature dependence that is intense in the channel current (drain side).

To improve these performances, it is possible to compromise between the high current gain, the high transition frequency, and the low pass resistance. Studying the Drift zone construction from doping is necessary to absorb the intense electric field in the current channel. However, as with any device used in power RF applications, these transistors have operating limitations related to the thermal problems, which vary enormously to the device's electrical characteristics. Its consideration in the design has become indispensable for the power RF MOS devices, especially to reduce the on-state resistance as low as possible.

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