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Original Article

Evaluating the Statistical Stability of POSIT Arithmetic and IEEE 754 Float to Accelerate Data for Detection of Breast Cancer

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Abstract *- In recent years, the researcher has focused on the hardware implementation of Floating Point Units (FPUs), which have a huge area and energy footprint. Due to their greater accuracy, speed, and simpler hardware design, Posit Arithmetic Units (PAUs) are proposed to replace IEEE 754-2008 compliant FPUs. It is important to improve existing floating-point IP cores for field-programmable gate array (FPGA) based applications. In comparison with other floating-point formats, posits number representation offers greater dynamic range and numerical accuracy. Various researchers attempted to implement a support vector machine (SVM) using hardware implemented on FPGA platforms to achieve high performance at lower power consumption and cost. As a result, the algorithm is unsuitable for embedded real-time applications. Therefore, SVM linear classifier is implemented on hardware, decreasing the latency and executing the task in real-time. This paper proposes an SVM linear classifier with pipeline architecture for fast processing in Verilog HDL using a single-precision IEEE standard 754 number format with 32-bit representation. The POSIT algorithm design is done with 24-bit representation using a software approach to determine the accuracy of prediction for the detection of Breast Cancer. The accuracy rate is computed both using software and hardware for performance evaluation. The pipelined SVM architecture is designed using Verilog HDL and synthesized using the Vivado simulation tool. The design is configured to the Xilinx KC705 Kintex-7 evaluation board for implementation.*

Keywords *- Breast Cancer, FPGA, IEEE 754 format, SVM, Vivado tool, Verilog HDL.*

1. Introduction

Breast cancer seriously risks women's lives and health [1]. The illness is treatable in the early stages, but it is not recognized until later, which is the primary reason for the death of so many women worldwide. Breast cancer detection at an early stage is critical for successful treatment and lowering the mortality rate. In the United States, 12.15 percent of women [2] will develop this cancer during their lifetime. For the last two decades, machine-learning researchers have been improving classifier effectiveness. As a result, machine-learning research has resulted in a new generation of cutting-edge supervised machine learning [29] classification algorithms, such as SVMs.

SVMs are considered a very good supervised learning algorithm that offers cutting-edge accuracy at the cost of high computational complications [4]. On the other hand, the standard versions of the SVM algorithm are very time-consuming and computationally intensive, presenting a challenge to investigate other hardware architectures than the CPU. It motivates the SVM to be realized on hardware platforms to attain high-performance computation at low-power consumption and cost.

Posit has various benefits over floating point numbers, including greater accuracy, a wide dynamic range, the capacity to provide results that are bitwise equal across platforms, simpler hardware, and the capacity to manage exceptions more effectively [5]. Compared to IEEE float floating point units, posit processing units require less circuitry. It is more efficient to employ low-precision posits than inexact computing methods that attempt to compensate for decreased quality of answers [6]. A wide range of applications is accelerated and performed with a substantial performance by FPGAs, proving that they are superior to other comparable platforms, such as graphics processing units (GPUs) and general-purpose processors [25]. As a result, FPGAs have become increasingly popular for realizing and accelerating SVM on hardware for low-power embedded system applications.

Section 2 describes the literature review related to the identification of Breast cancer, SVM, IEEE 754 float, POSIT arithmetic, and FPGAs, which are necessary for understanding the suggested method for the identification of cervical cancer. Section 3 discusses the system architecture implementation with floating point multipliers and adder trees in more detail. Section 4 presents the proposed design simulation, synthesis, and implementation

in more detail. Finally, a brief conclusion and future implementation are presented in section 5.

2. Related Work

In real-time scenarios, Deep Neural Networks (DNNs) are increasingly constrained by real-time constraints, so information representation must be re-evaluated. Encoding information in a way that can be processed rapidly and represented in a hardware-friendly way is a very challenging endeavor. In recent studies, posit formats have been shown to satisfy real-time constraints better than IEEE 754 standards for floating point representations of real numbers. According to Cococcioni et al. [8], Posit-based DNNs can be activated in the same way as 32-bit floats with 16-bit down to 10 bits. Despite their lower performance, 8-bit Posits could be a good substitute for 32-bit floats due to their high speed and low storage properties.

According to Van Dam et al. [9], there are approximately 160 MPOPS for multiplication, 250 MPOPS for addition, and 180 MPOPS for accumulations. As a result, intermediate results can be rounded off without affecting decimal accuracy. For the same number of bits, posit arithmetic gives higher decimal accuracy than the IEEE floating point format. Selvathi et al. [10] proposed integrating a computerized diagnostic system for breast cancer identification onto FPGA using Artificial Neural Network (ANN). The features of the WBCD are used to train and test the Multilayer Perceptron Neural Network (MLPNN). Baez et al. [11] proposed using Xilinx SDSoCTM to optimize the HLS methodology (Software-Defined SoC (System on chip)). The multiclass SVM classifier algorithm is designed using C programming and implemented on ZC7020 (ZedBoard) and ZC7045 (ZC706) devices.

Mohammadi et al. [12] proposed hardware implementation of SVM with parallel processing using Stochastic Gradient Descent for implementation onto FPGA. Fiolhais et al. [26] proposed a fused dot product processor with exact operand arithmetic that can output an incomplete result per cycle. The processor employs a long interval accumulator with full fixed-point precision to achieve full accuracy. Bassoli et al. [14] investigated FPGA implementations of IEEE 754 floating-point adder and multiplier for fast data processing using a conventional approach and customizations to save the chip area. The binary parallel multiplier and adder, which is a digit-serial multiplier, were proposed by Louca et al. [15]. One of the most significant limitations of existing embedded FPGAs is their major hardware development effort and time-to-market.

Table 1. Summary of different methods for breast cancer detection with limitations for the WBCD dataset

Author	Method	Application	Hardware	Acc. Rate	Area, Timing, and Power	Limitations
T Chandrasekaran et al., 2021 [16]	ANN based machine learning classifier	Breast Cancer Detection	Hardware-Software Co-design (CMOS-IC)	ANN=96.9%	-------	The limited dataset has been used for training. The ANN requires a huge volume of data for proper training.
Selvathi, D et al. 2018 [17]	ANN implementation using FPGA	Breast Cancer Classification	FPGA Virtex 5 board using XILINX ISE tool	90.83%	-------	limitation is optimization is not done, and no on-board Implementation
Batista et al. 2020 [18]	Pseudo-logarithmic number representation	Data classification	FPGA	-------	--------	Accuracy rate not computed Timing optimization not done Expensive multipliers with simpler adders
González-Díaz_Conti et al. 2022 [19]	ANN	Breast Cancer Detection	Xilinx Vivado 2016.1 FPGA Device: Zynq-7 ZC702	-------	LUTs:2267 Power:1.752 W Timing: ------	Accuracy rate not computed Timing optimization is not done

Numerous researchers [20]–[23] have contributed their work to implement the SVM machine learning algorithm, which is becoming increasingly popular in research due to the promising opportunities it provides in this field. Kim et al. [28] presented an IEEE 754 single precision multiplication method to cut down on the number of logic blocks. The suggested work estimates only one of the operands and iteratively compensates for the calculation error to attain limited errors in respective applications.

Most authors proposed CAD system development for the detection of Breast cancer, and very few papers report FPGA implementation for the detection of various types of cancer. As per the literature review, no paper is found on implementing an efficient SVM classification system for the identification of Breast cancer onto FPGA. Most existing implementations other than Breast cancers are not realized on modern FPGAs board, as evident from the literature review.

3. Proposed Architecture for Faster Data Classification

3.1. System Architecture

The SVM linear classifier's proposed FPGA design is shown in Figure 3. The architecture's adder tree constructs the classification function f(X) with the bias 'b' and polynomials such as patient data and weight value. Once testing data is passed into the FPGA board, the trained model uses it to perform a classifying procedure. The results are compared using the decision function to obtain either benign or malignant.

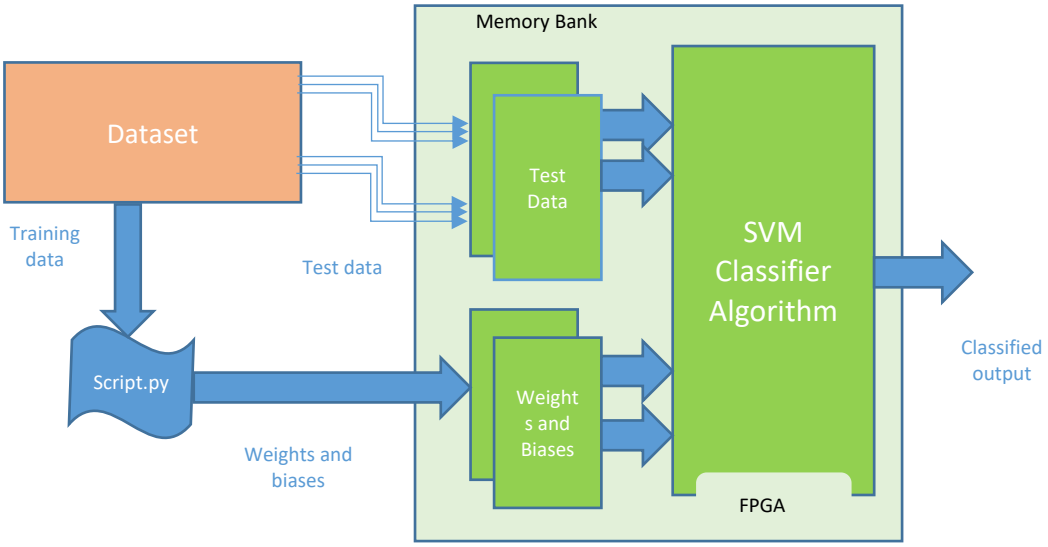

Fig. 1 System Architecture for Classification

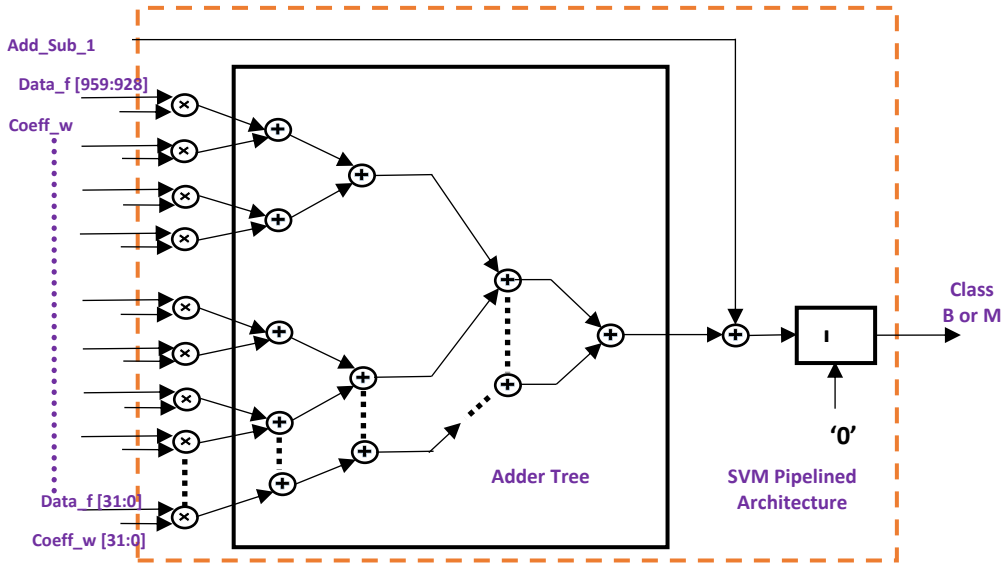

Fig. 2 SVM Linear Classifier Architecture

3.2. Design of BRAM Controller

The block RAM controller's design is essential to load breast cancer patient data and computed weight values using python script corresponding to each feature in Wisconsin Breast Cancer Dataset. The loaded data can be used further as input by designing a linear SVM classifier to create a training model to classify two data classes.

3.3. Computing for Linear SVM Classifier

32-bit handles the system's computations signed floating-point multipliers and adders with a single sign bit, a 23-bit mantissa, and an 8-bit exponent. The floating-point math packages are based on the VHDL 1164 numeric_std package and use the package's signed and unsigned arithmetic. Because the numeric_std package is well supported by simulation and synthesis tools, they are extremely efficient.

4. Experimental Results and Discussions

This study seeks to determine the most useful features in identifying malignant or normal cancer. The main objective is to discover whether breast cancer belongs to malignant or benign. Here, the standard WBCD dataset is analyzed for 569 patients with 30 best features to categorize between two data classes for the detection of Breast Cancer.

4.1. Simulation Output Waveform Analysis of Top Module of SVM Linear Classifier

The pipelined SVM architecture is designed using Verilog HDL, then synthesized by Vivado (ver. 2017.4) simulation tool. The design is implemented through translating, mapping, placing and routing, and generating a bit stream. Ultimately, it is configured to the Xilinx KC705 Kintex-7 evaluation board. Below are the simulation results for the single precision IEEE standard 754-based SVM linear classifier algorithm.

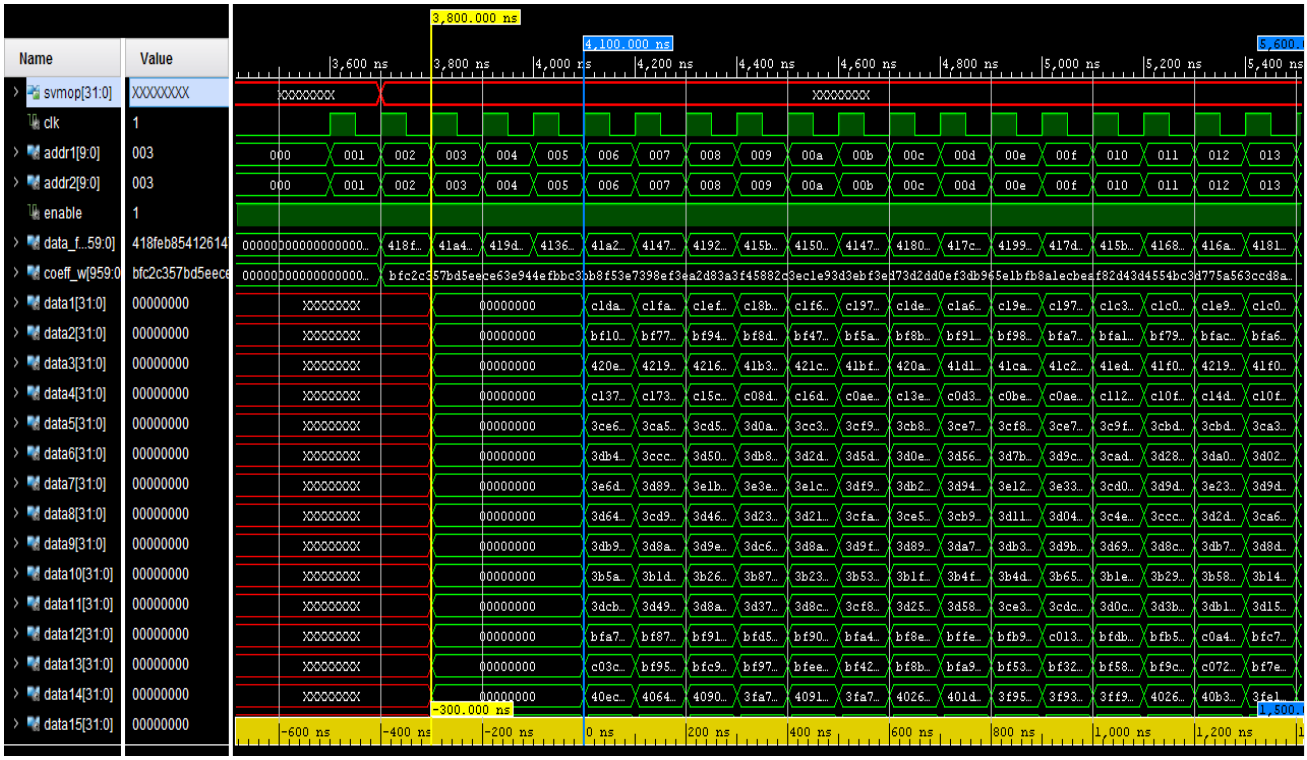

Fig. 3 The Output Waveform for Top Module of SVM Classifier: Depicts Data Loaded into BRAM at 3700 ns

The Simulation result of the SVM linear classifier depicts data loaded into BRAM for training to the positive edge of the clock, as shown in Figure 3. There are 30 features in the WBCD dataset, and each feature is represented with a 32-bit floating point number. So total bandwidth required to accommodate each patient's data is 960 bits wide. The simulation window shown in Figure 4 depicts pipelined adder tree operation with different stages of operation.

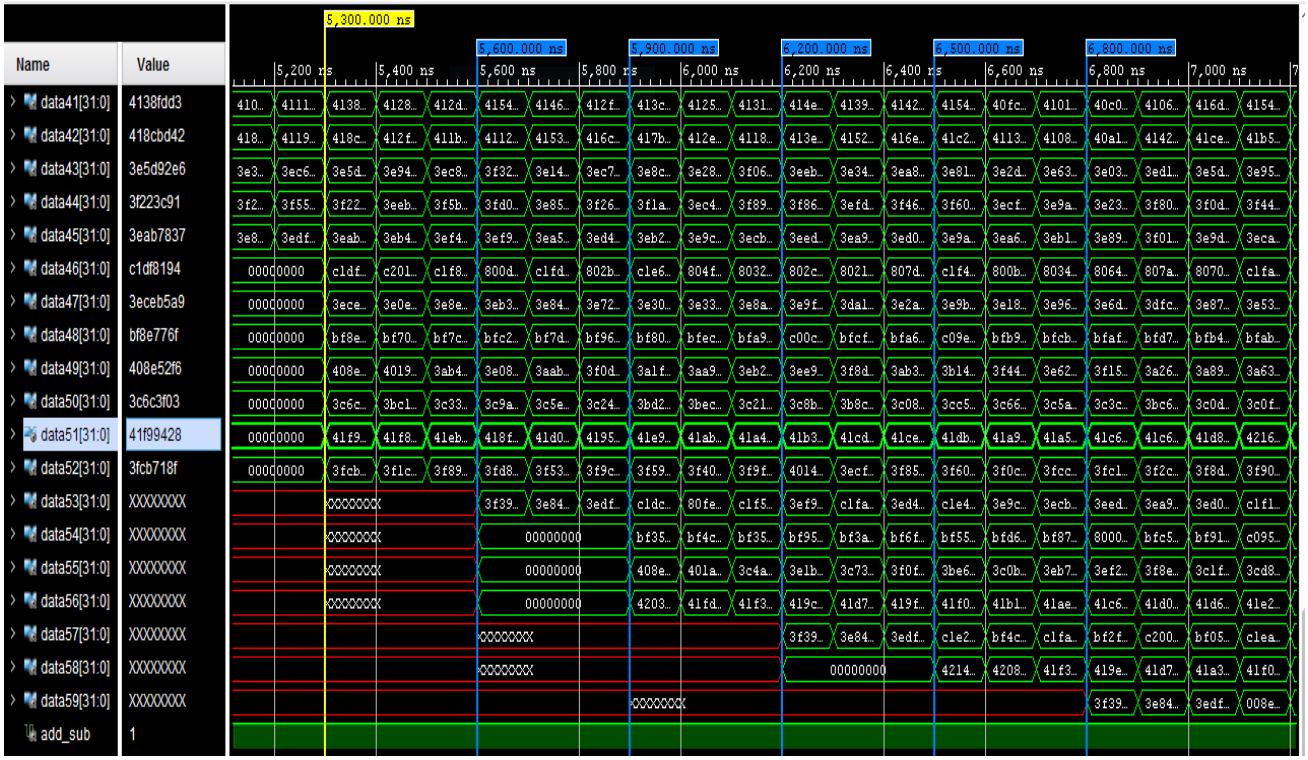

Fig. 4 Simulation Waveform of Adder Tree Pipelined Operation in SVM Linear Classifier at Different Stages

4.2. Logic Synthesis of top module SVM classifier system

After synthesis and implementation, it becomes very easy to check and analyse the different metrics such as area, power, and timing. The implementation result is more accurate in evaluating the performance analysis of the system. The schematic view of the top module SVM classifier after synthesis is shown in Fig. 5.

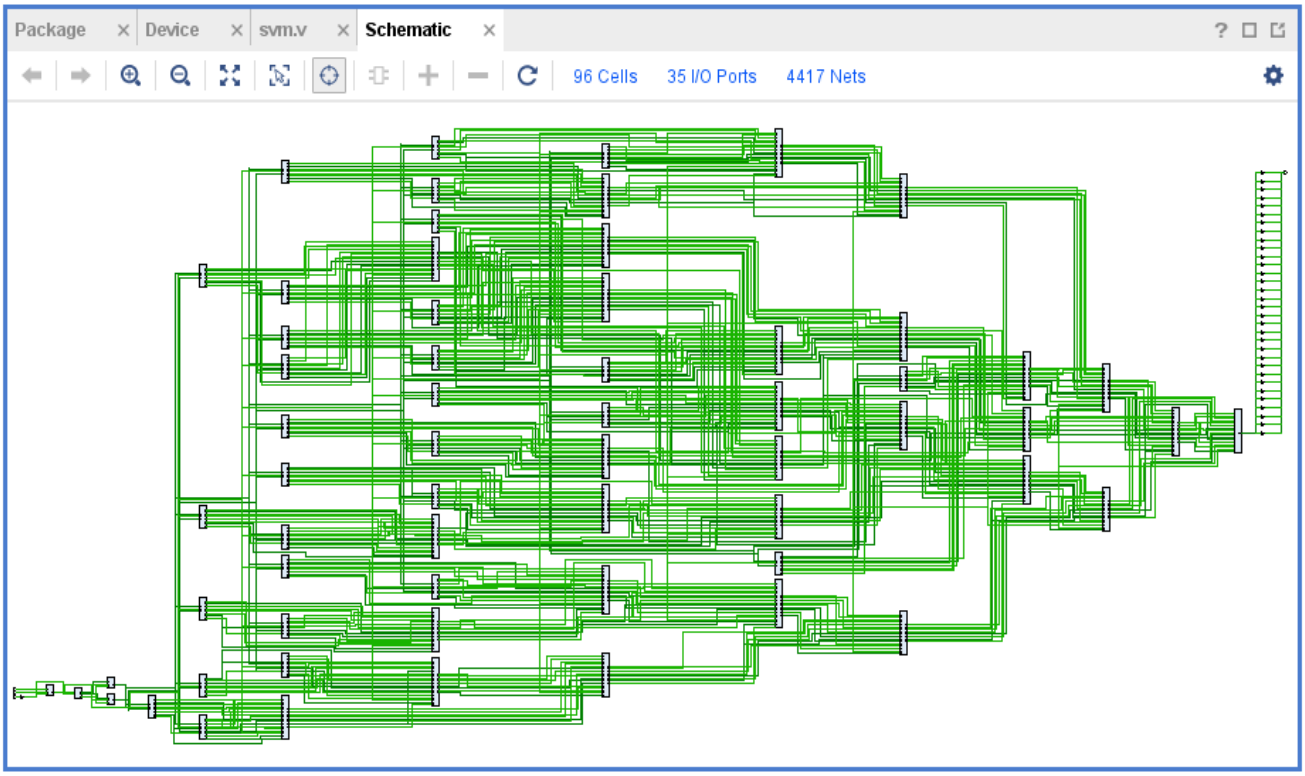

Fig. 5 Schematic View of Top Module SVM Classifier after Synthesis

4.3. Analysis of SVM output

The obtained hexadecimal number needs to be converted into a real number for comparison to find out the classified output, whether it belongs to 'Benign' or 'Malignant.' If the SVM output is positive or equal to '0', then the decision is taken w.r.t 'Malignant.' Similarly, if the SVM output is negative or less than '0', then a decision is taken w.r.t 'Benign.' It results in more inaccuracy than only positive, negative, and '0' for classification. To overcome this problem, a confusion matrix needs to be incorporated to increase the percentage accuracy by considering true positive or negative and false positive or negative. The accurate classification rate of the proposed system is 91%. The classification accuracy can further be increased by using an exact dot product accumulator with additional hardware cost.

There is a slight improvement in accuracy percentage obtained using Posit 24-bit format to IEEE 754 floating point algorithm implementation for detecting breast cancer using the WBCD dataset. The accuracy of precision for detection of breast cancer is obtained after running software code in Java for 24-bit posit format. The accuracy obtained is about 0.9122 using the Posit 24-bit format for IEEE 754 single precision 32-bit representation. The obtained result indicates that using the Posit 24-bit format, it is possible to obtain a better accuracy of IEEE 754 single precision 32-bit representation.

Table 2. Summary of POSIT arithmetic and IEEE 754 float

Format	Representation	Accuracy
IEEE 754 float	32 bits	91%
POSIT arithmetic	24 bits	91.22%

The summary of performance evaluation of POSIT arithmetic and IEEE 754 float is presented in table 2.

5. Conclusion

The proposed parallel implementation of the SVM algorithm for detecting breast cancer using the Vivado simulation tool as a training system is presented. The major objective of this solution is to reach a high data processing rate to satisfy the needs of computationally demanding applications. As a result, all possible multiplications and additions were parallelized. Finally, based on interpretations using the synthesis results, it can be concluded that implementing this technique in hardware would result in significant performance enhancements over the existing methods. The simulation and synthesis results exhibit that the SVM linear classification system is more effective in fast data classification. According to experimental results with a maximum frequency of 100 MHz in linear classification, the classification accuracy of about 91% in linear one has been achieved. The accuracy obtained is about 0.9122 using the Posit 24-bit format with respect to IEEE 754 single precision 32-bit representation. The obtained result indicates that using the Posit 24-bit format, it is possible to obtain a better accuracy of IEEE 754 single precision 32-bit representation.

The FPGA implementation of the SVM linear classifier with an exact dot product accumulator improves the percentage of accuracy related to state-of-the-art. It provides more flexibility to alter the structure in the future.

Conflicts of Interest

"Laxmisagar H.S and Hanumantharaju M.C declare that there is no conflict of interest regarding the publication of this paper."

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