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Original Article

Failure Identification of Power Converter Circuit using LabVIEW myRIO

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Abstract *- Failure diagnosis in power converter circuits is challenging due to its non-linear device characteristics. The power switches and electrolytic capacitors are the two main components that cause power converter failure. Predictive strategies are needed to be developed upon detecting these failures at the earliest, preventing catastrophic damages from spreading throughout the circuit. Predictive strategies include failure detection and failure identification. This paper discusses the technique involved in power switches and electrolytic capacitor failure analysis in power converter circuits. Two state variables are considered, firstly, the inductor current for Open Circuit (OS) and Short Circuit (SC) failure in power transistors, and secondly, the Equivalent Series Resistance (ESR) value for electrolytic capacitor failure. The proposed technique is implemented in a boost converter circuit for evaluation. The inductor current is monitored using a micro current precision current transformer, providing the appropriate footprint to predict failure due to open Circuits and short circuits in the power switches at its earliest. It is diagnosed using the myRIO FPGA target device. The ESR value that varies concerning the degradation of the electrolytic capacitor is measured online using precise measurement equipment.*

Keywords *- Fault diagnosis, Power switch, Inductor current, Electrolytic capacitor, Equivalent Series Resistance (ESR), myRIO FPGA Target.*

1. Introduction

Power converter plays a vital role in various applications as a fuel to power the circuitry. Any failure of such converters results in the breakdown of the entire system. Failure diagnosis of these converters is one of the main focuses of power electronics research. The key components that cause 90% of such breakdowns are the converter circuits' power switches and electrolytic capacitors [1]. Power switch failures are due to Open Circuit Failure (OC) and Short Circuit Failure (SC) [2],[3],[4]. Voltage (V) and current (I) characteristics across the circuit components are considered common State variables in diagnosing transistor failure. Observing the current slope of the inductance is a common method used in diagnosing OC and SC failure [4],[5]. Failure diagnosis Using Field Programmable Gate Array (FPGA) is one of the fastest approaches to identifying failure at its earliest [6]. This paper explains in detail an effective, fast and low-cost fault diagnosis of a circuit failure in DC to DC converter using state variables such as the inductor current and ESR value to determine the power Switch and electrolytic capacitor.

2. Review of Literature

This section discusses the existing techniques carried out in power converter failure detection. In [7], a technique of fault detection and fault tolerance of power switches in a DC-DC converter using an inductor current derivative is discussed. In [8] discusses the switch open circuit failure identification in the Voltage Source inverter using an electromagnetic field across the induction motor during the failure. In [9] discusses, OC failure identification of power switch in Permanent Magnet Synchronous Motor control using two fault identifiers such as the mean value of the stator current and the direction of the inductor current. [10] discusses power switch OC fault detection in an H-Bridge Inverter with the combination of load current and switching pulse. In [11], the paper discusses Push-Pull Converters' power switch OC and SC failure based on I & V characteristics in the time domain using Hardware In Loop method (HIL). In [12], the OC switch fault in the power inverter is diagnosed through the current phase comparison method using a DSP processor at a sampling frequency of 5 KHz. In [13], the DC-DC converter OC failure on one or more switches is diagnosed by sensing the inductor current using a DSP board. In [14] proposes the power switch fault diagnosis strategy in DC to DC converter, in which the change in the direction of the induction current is used as a signature for OC detection. In [15], fault detection of OC of power switches in the converter is implemented using capacitor current.

The capacitor current, phase current, and voltage combination show the fault condition. In [16], the fault analysis of OC & SC in a power switch in DC to DC converter is diagnosed by monitoring the current across the capacitor for the switching cycle and inductor voltage. Electrolytic capacitors have added advantages due to their large capacitance value, higher voltage range in a compact size and nearly low cost, making them an inevitable component in power converters. Faults in electrolytic capacitors may be due to constructional and parametric failure [16]. Constructional failure causes due to high electrical stress. Parametric failure causes due to the degradation of physical parameters such as electrolyte evaporation, thereby changing the Equivalent Serial Resistance (ESR) [16]. Due to parametric failure, the capacitance value decreases the ESR value increases. Hence by monitoring the ESR value, the degradation of the Electrolytic capacitor can be determined. It is a general principle that if higher the ESR value is and lower the capacitance is higher, the capacitor will be replaced [17]. The ESR value can be calculated using two approaches, namely: (i). Offline approach (measuring the ESR after the capacitor is removed from the circuit); (ii). Online approach (measuring the ESR value while in the circuit)[18]. The online approach is preferred due to its advantage of measuring the ESR value without dismantling the capacitor from the application circuit [19]. In [19], the fault diagnosis examines the relativity between the input current slope and the output voltage at the conduction time. It also discussed the relativity between the Temperature and the ESR value. In [20] proposes a simple method to calculate the ESR value in an online mode based on the variation in the output voltage. The inductor's output ripple voltage and current slope are the key signature element in ESR measurement. In [21], online fault monitoring of aluminium electrolytic capacitors is proposed using magnetic field-based sensing. The proposed approach considers the voltage drop on the capacitor as the key parameter to measure the ESR value, indicating the capacitor lifetime. In [22] discusses the overview of different lifetime monitoring approaches for capacitors, predicting ESR value using capacitor voltage and calculating the ESR Value and capacitance using the current and voltage ripple. In [23], the ESR calculation of electrolytic capacitor in buck converter is proposed using current and voltage characteristics. It proposes two methodologies considering the inductor current slope and the output ripple voltage as key characteristics in estimating the ESR value using linear algebraic transform function and orthogonality.

The proposed method monitors the inductor current slope sign to determine the OC and SC failure in the power switch and the ESR value across the Electrolytic capacitor to determine its lifetime. This paper focuses on FPGA-based implementation of the failure detection of the power switch and electrolytic capacitor in a boost converter circuit. The state variables are sampled at a higher sampling rate of 40MHz, 25ns per sample. The proposed approach has the diagnosis of the power switch within half the switching cycle.

3. Proposed Methodology

3.1. Switch Failure in Boost Converter

The proposed fault detection technique in the power switch is explained in detail in this section. The technique is implemented, the output is verified using the boost converter circuit, and the same can be implemented in other converter circuits. Fig.1.(a) illustrates the conventional circuit diagram of a boost converter in which the input voltage is scaled up at the output. The power switch (Q), inductor (L), and output capacitor (C) act as major components to scale up the output voltage. The scale-up factor is determined depending on the inductor parameters. The power switch is triggered using Pulse Width Modulation (PWM) at a few KHz. Boost converters operate in two modes, namely the Continuous Current Mode (CCM) and Discontinuous Current Mode (DCM).

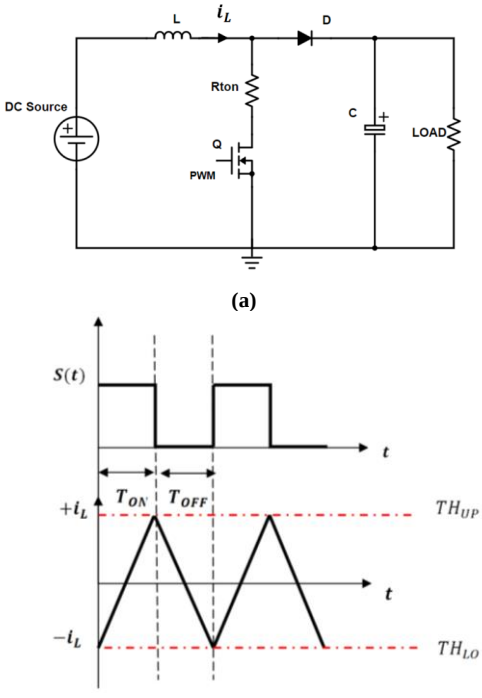


Fig. 1 (a) Conventional boost converter circuit. (b) Boost converter inductor current slope

Power switch failure can be categorized as OC and SC failure; State variables such as inductor current can provide a significant signature of such OC and SC failure in power converter circuits [4-7]. Considering the operation of a conventional boost converter in CCM mode, assume that the power switch is in an ideal state and provided with desired PWM pulse s(t). During the conduction time, the inductor L

starts charging, increasing the inductor current i_L. Similarly, during the non-conduction time, the energy stored in the inductor charges the output capacitor C, thereby decreasing the inductor current slope. Fig.1.(b) illustrates the inductor current slope during normal operation. The OC and SC failure can be identified by monitoring changes in inductor current magnitude than the threshold level. SC failure in the power switch results in a sudden elevation in the inductor current than the higher threshold level TH_{UP}, in a positive direction.

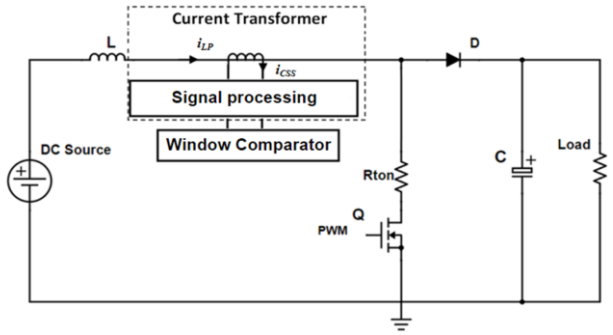


Fig. 2 Inductor current measurement circuit.

OC failure in the power switch impacts the inductor current, resulting in a more rapid descending of current than the lower threshold level THLO in a negative direction. Hence this paper focuses on sampling the inductor current and monitoring the slope direction of the inductor current; the OC and SC of the power switch can be identified. Fig.2 illustrates the inductor current measurement in the boost converter circuit using a current Transformer (CT). ZMCT103C is a micro-accurate current transformer with a turn ratio of 1:1000. It is a donut-shaped module whose output is a few mA currents. i_{LP} is the current in the primary winding, and current i_{CSS} is the current in the secondary of the current transformer. The corresponding voltage is measured across the secondary winding burden (with signal processing circuit). The OC and SC failure in the power switch can be identified using the change in inductor current exceeding the thresholds, which can be monitored using the window comparator.

Whenever the input of the comparator crosses the upper and lower threshold values, the output of the comparator goes high. Fig.3(a) shows the basic circuit diagram of the window comparator. It employs a dual comparator to compare the input signal whether it is within two threshold limits, one is the upper threshold limit (V_U), and another is the lower threshold limit (V_L). The output voltage from CT is given as the input (V_{in}) to the window comparator. The input V_{in} is connected to the upper converter's positive end and the lower comparator's negative end. The upper threshold voltage (V_U) is connected to the negative terminal of the upper-end comparator, and the lower threshold voltage (V_L) is connected to the positive terminal of the lower-end comparator. The comparators' output is connected to a NAND gate latch circuit. The reset input is used to reset the latch. The working principle of the window comparator can be explained using three states,

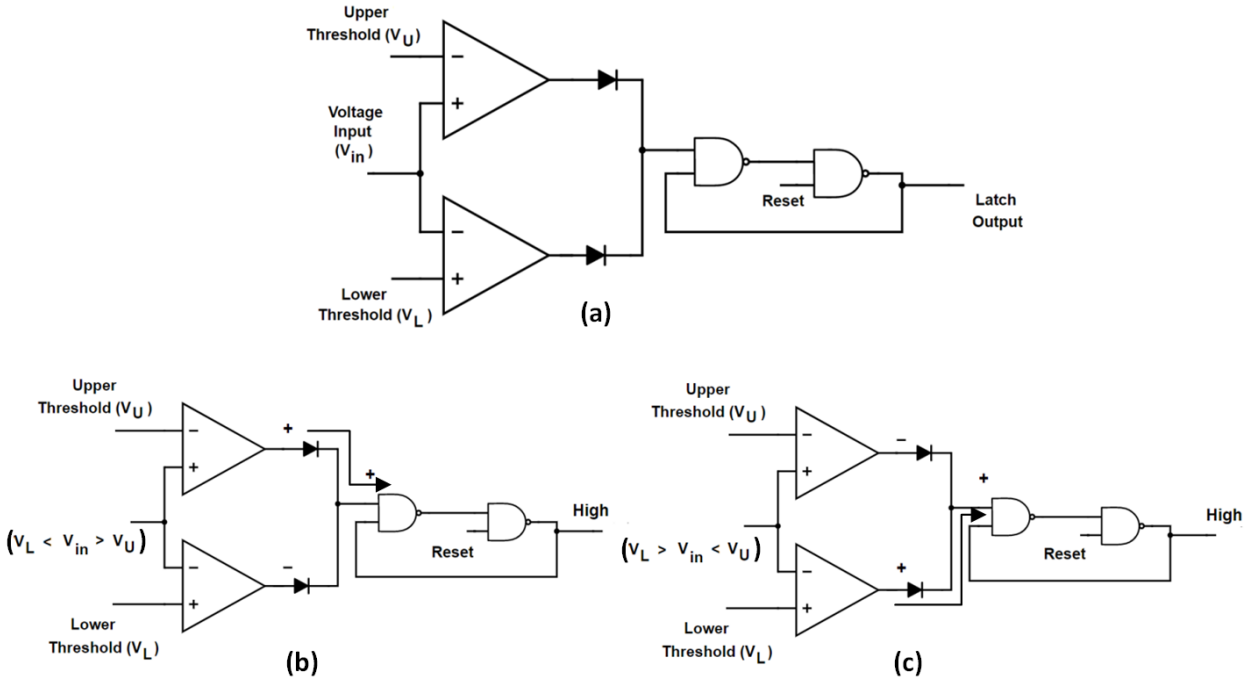


Fig. 3 (a) Window comparator. (b) Comparator State2 condition. (c) Comparator State3 condition.

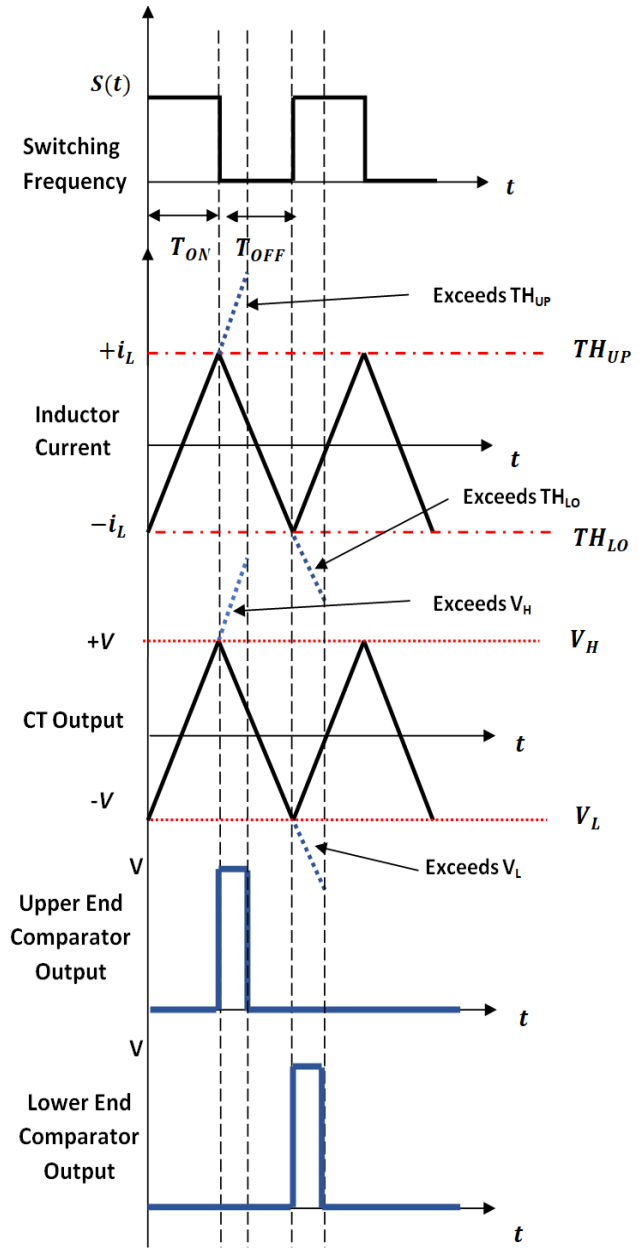


Fig. 4 Window comparator output waveforms

State 1: Consider if $V_L < V_{in} < V_U$; since V_{in} is less compared to the V_U and greater than V_L, the upper-end comparator output goes low, and the lower-end comparator output goes low. Hence the diodes connected at the output of both the comparators turn off and latch the output to a low level.

State 2: Fig.3(b) illustrates the comparator circuit working at state1. Consider If $V_L < V_{in} > V_U$; since V_{in} is greater than V_U, the upper-end comparator output goes high, and the lower-end comparator output goes low. Hence the diode connected to the output of the upper-end comparator turns on and latches the output to a high level.

State 3: Fig.3(c) illustrates the comparator circuit working at state 2. Consider if $V_L > V_{in} < V_U$, V_{in} is less than V_L, the upper-end comparator output goes low, and the lower-end comparator output goes high. Hence the diode connected to the output of the lower-end comparator turns on and latches the output to a high level.

Fig.4 illustrates the State2 and State3 waveforms. The proposed method is tested by injecting failure across the power switch. Considering the DC to DC boost converter in CCM, The OC and SC failure are injected, and a response is observed. Fig. 5(a) shows the boost converter circuit with 2 switches S1 and S2. S1 is connected in series with the power switch to injecting the OC fault, and S2 is connected across the power switch to inject the SC fault. By manipulating switches S_1 and S_2, the direction of the inductor current is changed. During a fault, free condition switch S_1 is in close (ON) condition and switch S_2 is in open (OFF) condition. Fig.5(b) illustrates the inductor current in fault-free conditions. Considering SC failure, Fig.5(c) illustrates the inductor current during SC failure, and $S_2(t)$ is the switching action of switch S_2. Initially, consider Switch S_1 in a close condition and S_2 in an open condition which is a normal condition. When Switch S_2 is closed, since S_2 is connected parallel to the source and drain of the power switch Q (MOSFET), forming a least resistance path when compared to the source and drain of the power switch, there will be a sudden rise in the inductor current.

Considering OC failure, Fig.5(d) shows the inductor current slope during OC failure, and $S_1(t)$ is the switching action of switch S_1. Initially, consider Switch S_1 is in a close (ON) condition and S_2 are open (OFF) condition, which is a normal condition. When S_1 is open, the circuit becomes an open circuit, and the circuit impedance is equal to ∞. The power switch is open, and the energy stored in the inductance discharges through the diode and the output circuit, reducing the inductor current rapidly, as indicated in Fig.5(d).

Fig.6(a) illustrates the fault diagnostic setup. The inductor current is captured using a current transformer, and the corresponding voltage is 250mV peak to peak. Two switches, S1 and S2, are connected in series and parallel with the power MOSFET P80NF55. S1 is used for open circuit failure injection, and S2 is used for short circuit failure injection. The inductor current is measured using the CT ZMCT103C connected in series with the inductor L with a burden resistance of 1kΩ. The voltage is sampled using an FPGA target device (myRIO 1900 Hardware) at a sampling time of 25ns per sample.

Fig.6(b) illustrates the inductor current sampled output in fault-free conditions. The power MOSFET is switched at a clock frequency of 20 KHz with a 50% duty cycle. The

boost converter is provided with a DC input of 10V using an external DC source, and the output is boosted up to 18.8V DC. Fig.6(c) and (d) illustrate the fault injection response of the inductor current during SC and OC conditions, respectively. Fig.6(e) and (f) illustrate the upper and lower threshold levels. The output voltage from the CT is amplified using Op-amp to 4V peak to peak and shown. Fig. 6(g) shows the SC fault injection (at point P) and the detection of fault using a window comparator (at point Q). Fig. 6(h) shows the OC fault injection (at point R) and the detection of fault using a window comparator (at point S). The changes in the inductor current crossing the thresholds are monitored using LabVIEW and FPGA target devices. The diagnosis unit is controlled using LabVIEW. The reviewed power switch failure detection techniques discussed at the beginning of this paper are compared with the proposed technique, with parameters such as state variables, detection time and detection control in table 1. The comparison chart states that the proposed method is implemented in aDC–DC boost converter. The inductor current slope is considered the state variable, and the failure can be detected at one-fourth of a switching cycle of the MOSFET.

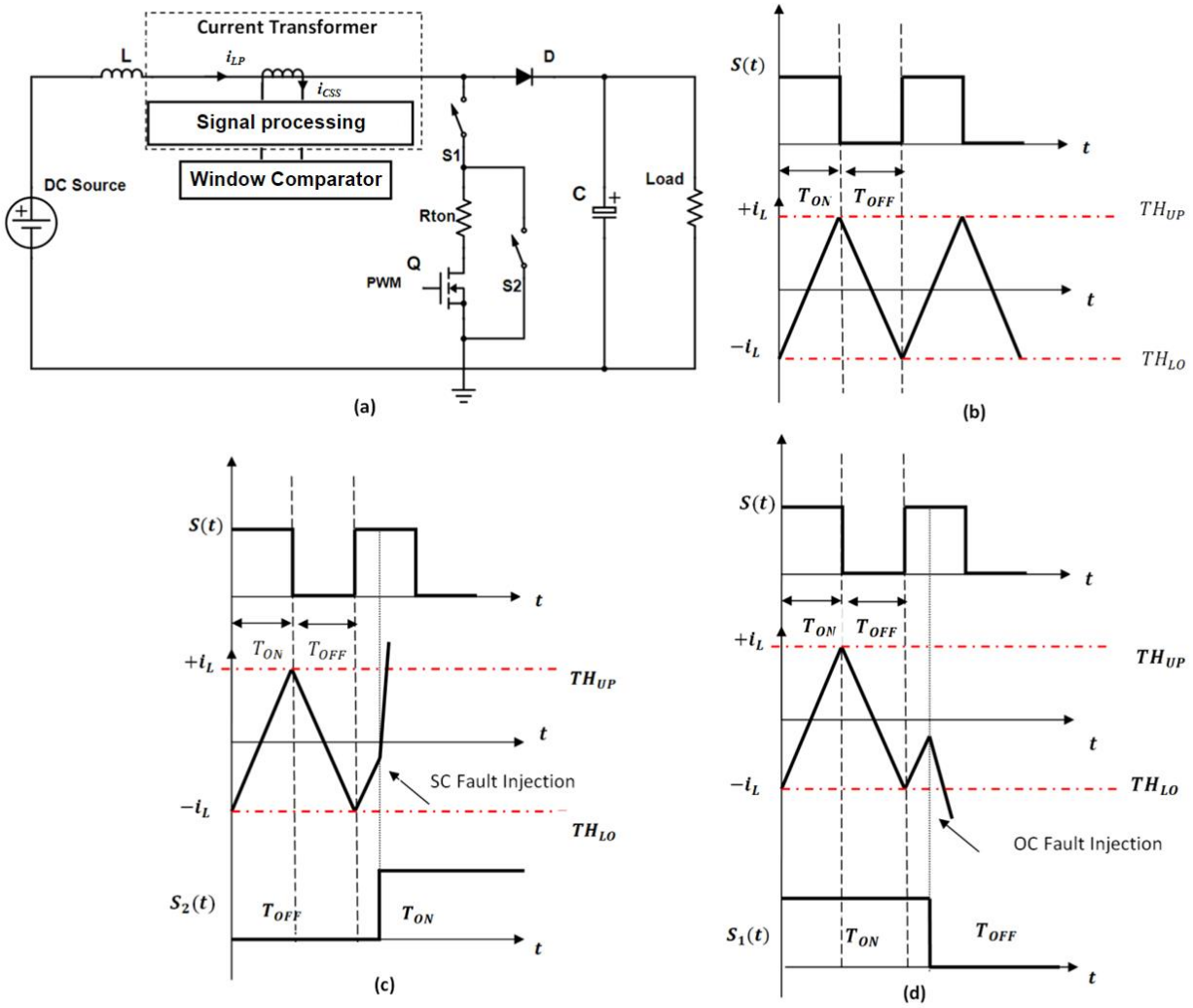


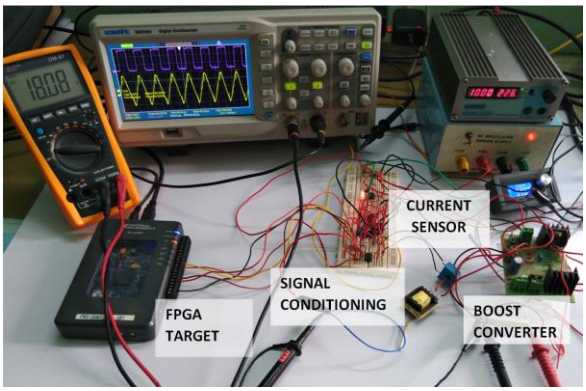
Fig. 5 (a) Failure injection circuit. (b) Failure-Free inductor current. (c) Inductor current during SC failure. (d) Inductor current during OC failure.

The components list of the boost converter circuit under test is illustrated in table 2.

3.2. Electrolytic Capacitor Failure in Boost Converter

This section discusses the proposed failure analysis technique to identify the electrolytic capacitor's degradation. The failure in the electrolytic capacitor can cause due to structural failure, resulting in a dead component and parametric failure due to the degradation of the electrolytic capacitor over time. Dissipation of electrolytes is one of the main causes of degradation, thereby increasing ESR value and resulting in High rippled output Voltage [26-29]. The voltage stress, ageing, temperature, and operation frequency are the factors that affect ESR, and any rise in ESR results in

a rise in peak-to-peak output voltage ripple [28]. High voltage Stress is applied across the capacitor in reverse polarity using an external DC source to evaluate the degradation factor of the electrolytic capacitor. The voltage stress, in turn, varies the ESR of the capacitor. The ESR is measured using LabVIEW and the LCR meter MCH 8817A for further evaluation. The LCR meter is connected to the PC via RS232 communication. Using LabVIEW, the ESR values are logged at different frequency ranges for faulty and fault-free electrolytic capacitors for monitoring the degradation factor. The whole diagnostic process is automated using the LabVIEW tool, and failure is predicted. Fig. 7(a) illustrates the experimental setup of the CUT for ESR measurement. The LCR meter is probed across the output filter capacitor of the boost converter circuit, and the ESR value is measured online. To validate the proposed approach, different values of capacitors are considered, i.e. 100µF and 47µF. Fig. 7(b) chart illustrates the ESR values of good and faulty capacitors 100µF and 47µF operated at different frequencies, 1 kHz to 100 kHz. It is observed that the ESR value of the faulty capacitor is very high compared to that of the good capacitor. Fig.7(c) and (d) illustrate that the ESR value of a 100µf electrolytic capacitor is 0.5 Ohms, whereas the ESR value of the faulty capacitor due to degradation is 3 Ohms. It is also observed that the capacitor value decreases in the faulty capacitor.



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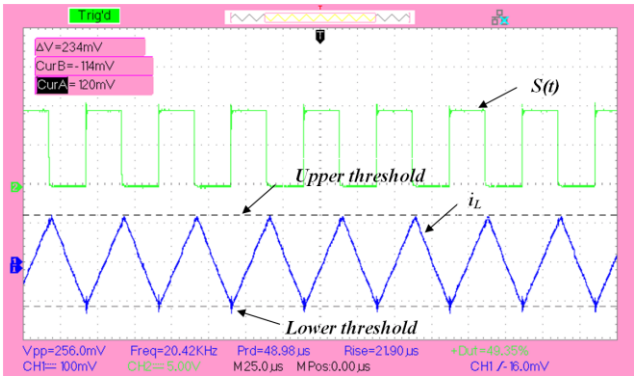

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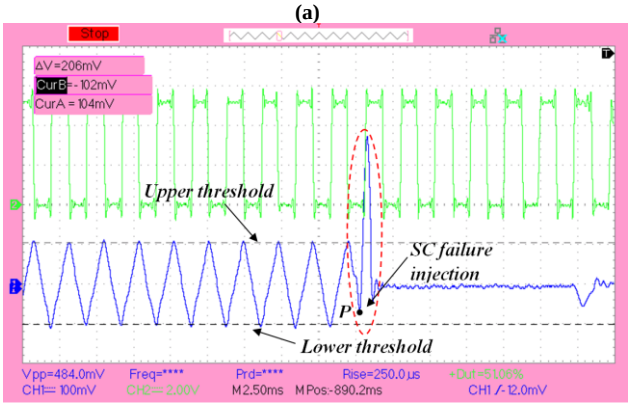

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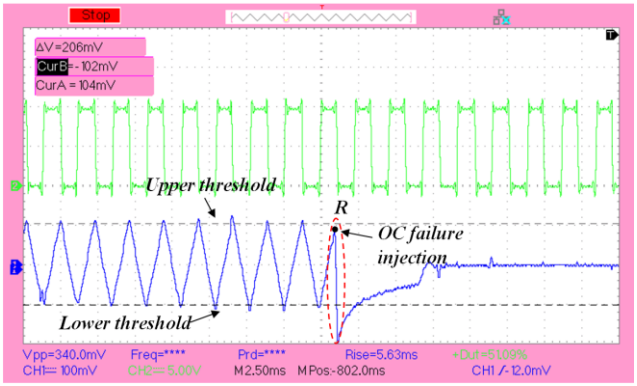

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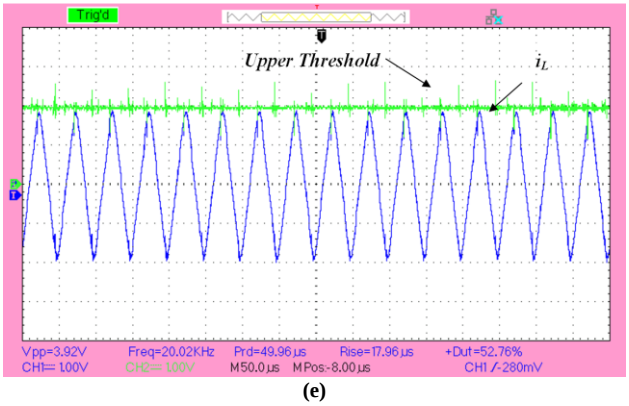

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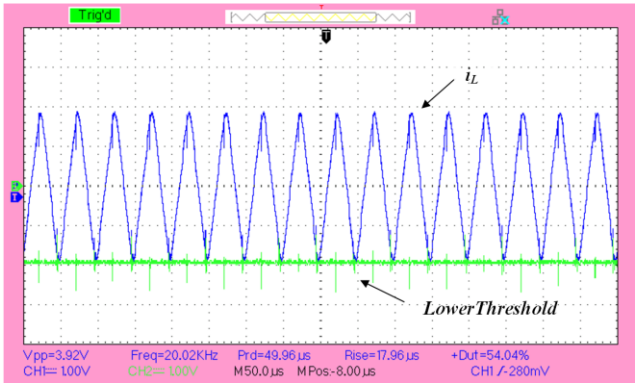

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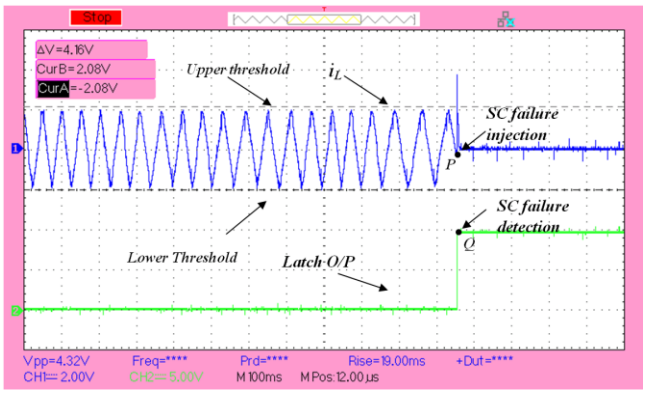

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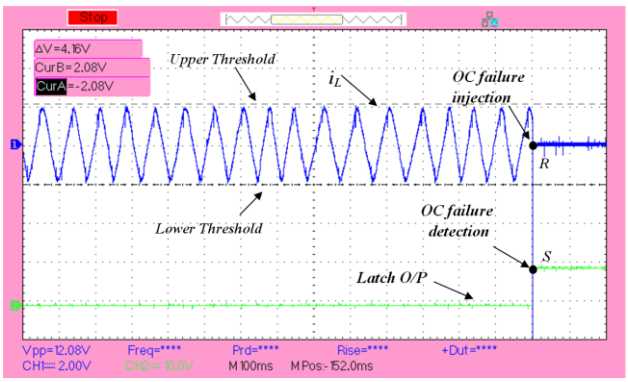


(h)

Fig. 6 (a) Experimental setup. (b) Failure-free inductor current slope i_L. (c) Inductor current slope during SC injection. (d) Inductor current slope during OC injection. (e) Upper Threshold Level. (f) Lower Threshold level. (g) SC failure detection. (h) OC failure detection.

Table 1. Power circuit Switch failure diagnosis techniques comparison chart.

Reference	Application	State variable	Detection time	Detection Control	Type of Failure	Cost
[1]	DC-DC converter	Capacitor Current	$T_d < 1/2t_s$	Gate logic	OS and SC	LOW
[2]	SRM Driver	Current error	1ms	Simulation Matlab	OS and SC	LOW
[3]	Multilevel converter	Capacitor voltage	$T_d = t_s$	Simulation Matlab	OS and SC	LOW
[4]	Push-pull converter	Inductor current and voltage	1-2 t_s	FPGA	OS and SC	LOW
[5]	Dc to DC converter	Inductor current	$T_d = t_s$	DSP	OS and SC	HIGH
[6]	DC to DC converter	Inductor current	$T_d < t_s$	DSP/FPGA	OS and SC	Mid
[7]	DC to DC converter	Inductor current	$T_d = t_s$	DSP	OS and SC	HIGH
[8]	PWM Inverter	Electromagnetic Field	$T_d < t_s$	Simulation	OS	HIGH
[9]	Inverter	Output current	$T_d < t_s$	dSPACE	OS	HIGH
[10]	H-bridge Inverter	Load current and voltage	$T_d = t_s$	dSPACE	OS	HIGH
[11]	Push-Pull Converter	Switch voltage and current	$T_d < 2t_s$	HIL (FPGA)	OS and SC	LOW
[12]	Power Inverter	Output current	8.33ms	DSP	OC	LOW
[13]	DC to DC converter	Inductor current	$T_d < t_s$	DSP	OC	LOW
[14]	DC to DC converter	Inductor voltage and current	$T_d < t_s$	DSP	OC	LOW
[15]	NNPP Converter	Capacitor Current	NA	DSP/FPGA	OC	HIGH
[16]	DC to DC converter	Inductor voltage	$T_d > 1/2\ t_s$	Gate logic	OC and SC	LOW
Proposed Method	**DC to DC converter**	**Inductor current**	**$T_d < 1/4t_s$ 25ns**	**FPGA**	**OC and SC**	**LOW**

T_d: failure detection duration.
t_s: Switching time.

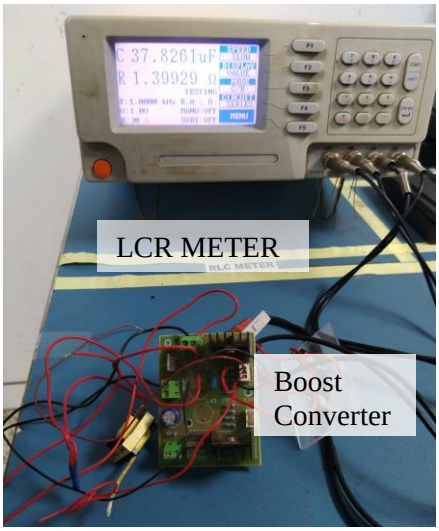
Table 2. Components list of the circuit under test.

Components	Value
N-type MOSFET	P80NF55
Inductor(L)	1mH
Inductor internal Resistance (R_L)	1.0 ohm
Current Transformer (CT)	ZMCT103C
CT Burdon Resistor	1k
Electrolytic capacitor	47mf 63V
Switching frequency	20kHz
Load Resistor(R)	220 ohm
Operational Amplifier	LT1252
High-Frequency Diode	UF4007

Table 3. Electrolytic capacitor failure diagnosis techniques using ESR value comparison chart.

Reference	Application	State variable to calculate ESR	Detection time	Detection Control	Cost
[1]	DC-DC converter	Capacitor voltage	$T_d < 1/2t_s$	Analog circuit	LOW
[17]	DC-DC Converter	Capacitor voltage and Trigger pulse	$T_d < 1/2t_s$	Simulation Matlab	LOW
[18]	DC-DC Converter	Capacitor voltage	$T_d = t_s$	Simulation Matlab	LOW
[19]	DC-DC Converter	Inductor current and voltage ripple	$T_d < t_s$	Analog circuits/DAQ	HIGH
[20]	DC to DC Converter	Input current and output ripple	$T_d < t_s$	Simulation Matlab	LOW
[21]	DC to DC Converter	Ripple voltage and inductor current	$T_d = t_s$	PCI DAQ	HIGH
[22]	DC to DC Converter	Magnetic field of current in I/O	$T_d < t_s$	LabVIEW/ Matlab	LOW
[23]	DC-DC Converter	Voltage /current Ripple	$T_d < t_s$	Simulation Matlab	LOW
[24]	Voltage Source Converter	Switching current	$T_d < t_s$	DSP	HIGH
[25]	capacitor(Offline)	Impedance spectroscopy	NA	Oscillator	LOW
[26]	DC-DC Converter	Capacitor voltage and current	$T_d < t_s$	Simulation Matlab	LOW
[27]	Fly back converter	Output current	$T_d < 1/2\ t_s$	DSP	HIGH
[28]	DC to DC Converter	Capacitor voltage and current	$T_d < 1/2\ t_s$	NI DAQ	LOW
[29]	DC to DC Converter Capacitor bank	Capacitor voltage and current	$T_d < t_s$	PC DAQ	HIGH
Proposed Method	**DC to DC Converter**	**Capacitor voltage**	**$T_d < 1/2t_s$ 25ns**	**FPGA**	**LOW**

T_d : failure detection duration.
t_s : Switching time.



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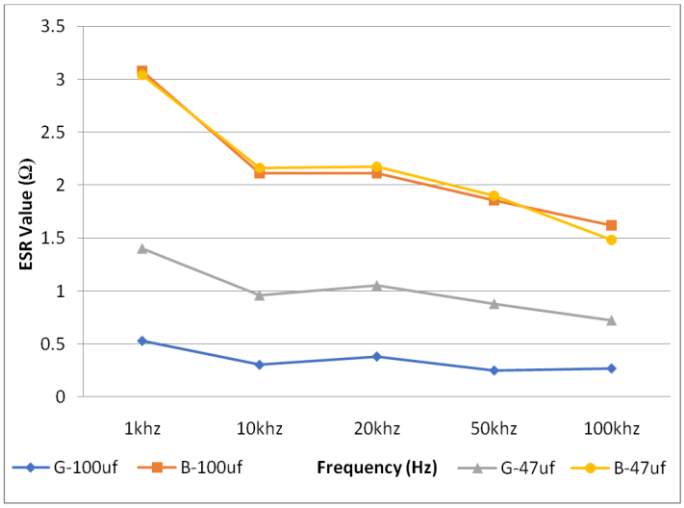

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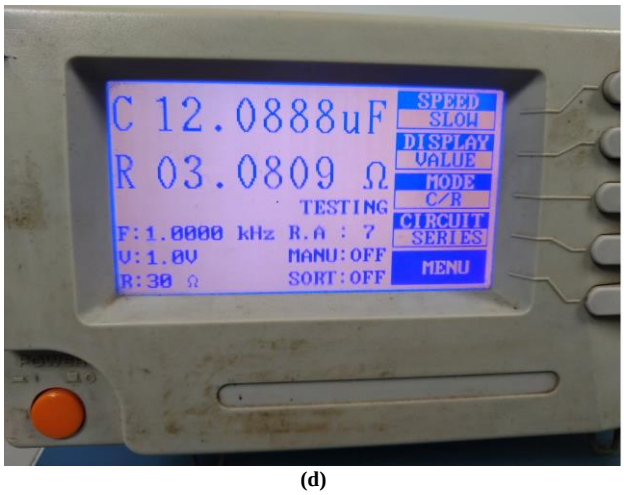

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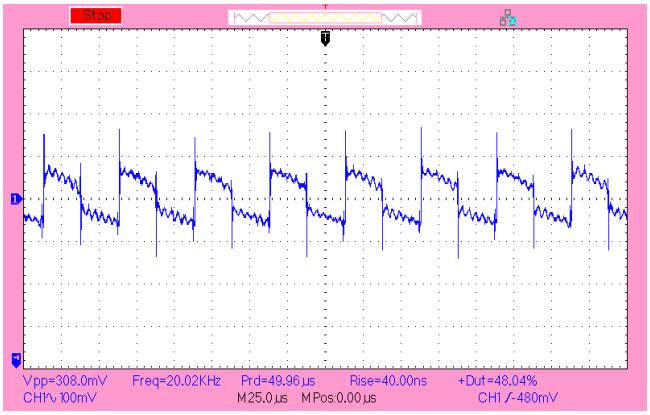

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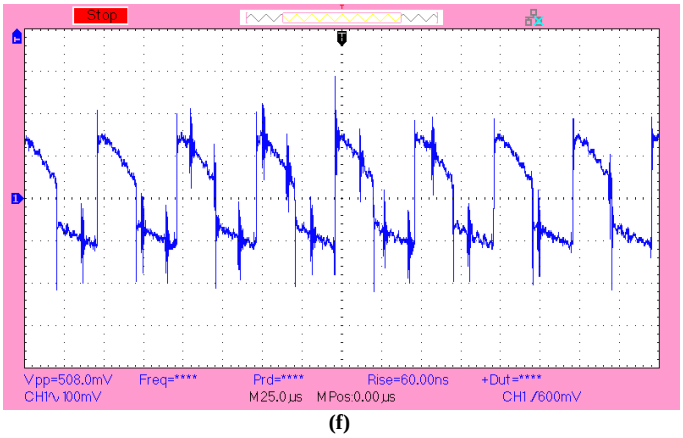

(f)

Fig. 7 (a) Experimental setup. (b) ESR vs Frequency chart (47µf, 100 µf). (c) ESR value of the fault-free capacitor (100µf). (d) ESR value of the degraded capacitor (100µf). (e) Output ripple due to fault-free capacitor (100µf). (f) Output ripple due to fault capacitor.

Fig.7(e) and (f) illustrate the changes in the output ripple of the converter circuit due to the degradation of the output filter capacitor (100µf). The peak amplitude of the output ripple is higher (508mV) in the fault condition compared to the fault-free condition (308mV) due to the change in ESR value. The reviewed electrolytic capacitor

failure detection techniques using ESR discussed at the beginning of this paper are compared with the proposed technique, with parameters such as state variables, detection time and detection control in Table 3. The comparison chart states that the failure is detected in half a switching cycle.

4. Conclusion

The fault identification method discussed above is implemented, and the output result is verified using a boost converter circuit in CCM under steady-state conditions. The SC and OC switch failure in the boost converter is identified by monitoring the inductor current within a threshold limit using the FPGA target and LabVIEW tool. The experimental results show that the SC and OC failures are detected at its earliest within one-fourth of the switching cycle. Similarly, the degradation of the capacitor is identified using the ESR value, which increases the output ripple. As far as the limitations are concerned, the threshold varies depending on circuit parameters. The work can be further extended by extracting the samples in the form of the dataset and using the Machine Learning model; the faults can be predicted, eliminating the threshold.

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