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Original Article

A Novel Reliable Five-Level Multilevel Inverter for Critical Loads

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Abstract - *This work discusses a Fault-Tolerant (FT), highly Reliable Five-Level (RFL) Multilevel Inverter (MLI) that can persist to function still if one or more power switches have an open single switch fault or a specific multi-switch fault. Consecutively to provide quality output voltage profile, the requirement of power switches such as IGBTs used in DC-AC converters is high in number; as a result, they are more likely to fail. Consequently, reliability is among the most critical challenges in MLIs in numerous applications. At the same time, while compromising crucial components (such as FT, charge balance management, and so on), reduced component MLIs may deliver the highest precision in output voltage waveform. For MLIs to function fault-tolerantly, redundant switching states have been stressed regarding switch failures. This work is aimed to provide a unique RFLI during an Open Circuit (OC) failure on a single or several switches for obtaining reliable operation. As a result, the suggested Reliable Five-Level Inverter (RFLI) structure is thought to have fewer components and must fulfill the functioning criteria for the time being. A suitable FT switching method is used in concurrence with appropriate fault clearing to obtain the requisite output voltage waveforms, resulting in dependability. The proposed RFLI architecture offers superior results regarding THD, cost, and efficiency during FT operation. The presented RFLI topology has been validated by using the MATLAB tool.*

Keywords - *Fault-tolerant, Reliability, Reduced switch count, Multilevel Inverter, Harmonic distortion.*

1. Introduction

One of the most critical and challenging tasks is maintaining the continuity and reliability of DC-AC converters in the industrial process and energy systems. This has resulted in fault-tolerant architectures focusing on reliability and system availability. Multi-Level Converters (MLI) are popular for medium-to-high-voltage applications due to their adaptability and high performance [1].

High-Voltage Direct Current (HVDC), renewable energy systems, variable-speed drives, hybrid electric vehicles, alternating current motor drives, solar diversification, and many applications all necessitate power electronic converters [2-5].

The block diagram of integrating renewable energy resources to critical loads using the reliable MLI is shown in Figure 1. Furthermore, because of the vast and rising demand in many applications, there is an issue with the overall dependability of the converter system. MLIs are more commonly used than two-level inverters because they can produce a range of voltages from medium to high power with a lower harmonic distortion, among other characteristics [6-11]. According to certain studies, 38% of total failures in inverters are caused by the inability of switches [10, 11], and new research indicates that any system dependability to be examined by using some system factors [12-15].

Several decades of research have been undertaken on the issue of fault-tolerant operation and fault detection of MLIs. The work in [16] establishes a fault-tolerant topology; nevertheless, all sorts of single switch failures are not addressed, and the component count is rather enormous. The architecture in [17] contains more redundant components and is unsuitable for multi-switch failure. [18] proposes a topology that does not accommodate all forms of individual switch failures. [18-21] topologies do not support multiple-switch failures, and the need for controlled power switches increases. To address the reliability issue of DC-AC converters, a range of FT topologies are proposed in [22].

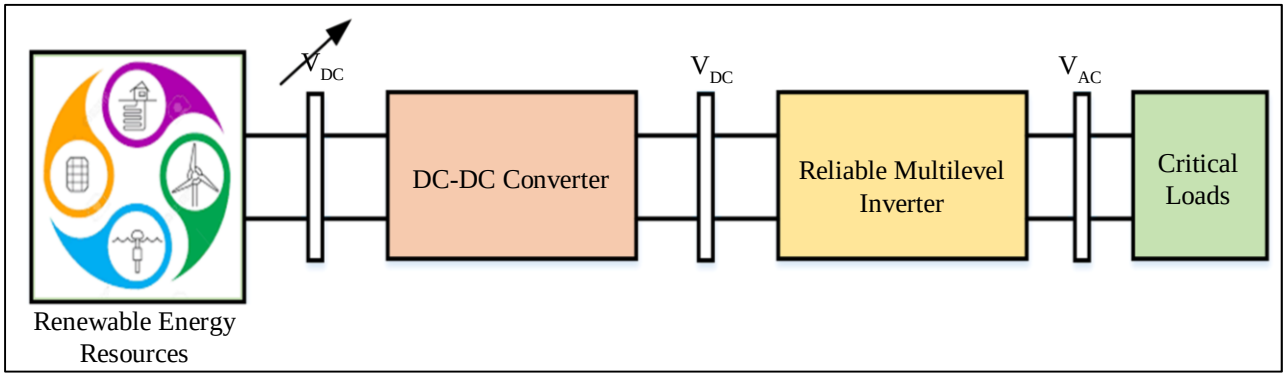

Fig. 1 Block diagram of integration of renewable energy resources to critical loads

The main problem with classical 2L inverters is their lack of reliability; MLIs are used instead of switches because of how vulnerable and standard switching devices are. A bidirectional controller is coupled to a CHB inverter so the affected cell can't be seen elsewhere.

Switching components can switch diodes and make NPC structures functional for faulty cases. The new version of the NPC 3L structure has one bidirectional power switch, a half-bridge, and one segment of diode-clamped inverter, all in a hybrid design, which adds up to more inverters and more cost. The FCFT structure is pretty detailed in [23-25].

The circuit can handle mistakes independently, but the complexity of balancing the capacitor and the number of devices is the leading cause of worry. You need to add extra circuitry to keep the inverter safe. Several modulation schemes for controlling MLIs are described in the literature [26-36]. To tackle these concerns, this paper presents a fault-resistant multisystem inverter capable of resolving all single-switch faults and specific multi-switch issues. In this work, only open circuit faults are analysed.

Consecutively, the proposed FTL MLI is presented as a single stage of this study to address the issues previously identified. The switching control scheme, Sinusoidal Pulse Width Modulation (SPWM) is adjusted minimally to improve MLI reliability. The lowest likely occurrence of a power equipment failure is presented in the tabulated version of the reported FTL MLI. In the case of an open switch fault, the output voltages generated by the fault are the minimum levels needed to keep the systems in working order. The suggested FTL MLI may offer a high degree of redundancy.

2. Proposed Reliable Five Level (RFL) Multilevel Inverter

As illustrated in Figure 2, the presented FT5L inverter includes four two-quadrant switches (S_1, S_2, S_5, and S_6) and two four-quadrant switches (S_3 and S_4). It also contains two capacitors, i.e., C_1 and C_2) across a DC source V_{DC}. Capacitors are utilized to split the voltage of the DC supply into two equal parts, allowing 02 four-quadrant switches to reach five voltage levels (i.e. $\pm V_{DC}$, $\pm 0.5V_{DC}$ and 0).

Table 1 shows the available switching combinations for obtaining different amounts of output voltage. The voltage levels of $+0.5V_{DC}$ and $-0.5V_{DC}$ have 02 switching states each, whereas the zero voltage has 03 changing conditions, indicating that the presented RFLI architecture provides switching state redundancy. When a fault is found in any of the switches, the gate pulse associated with the fault must be deactivated, and a symmetric output voltage can be achieved by utilizing the redundancy switching logic listed in Table 1.

The inverter provides output voltage with five levels in this mode, and ripple-less capacitor voltages must be attained using the suitable control scheme. Table 1 lists the switching instants of RFLI. In this table, logic '1' indicates the switch ON, while logic '0' indicates the switch OFF. To maintain the same level of stress and load between the switches, the zero voltage interval is divided into three possible combinations.

The faults investigated among the switches are open-circuit and are analyzed independently on every switch. The PWM modulation method shall be adjusted for all fault conditions considered to endure the RFLI faults, as outlined in Table 2. The fault cases shall be analyzed according to Table 2. In the faulty state of any power switch, the preferred voltage profile shall be obtained by the subsequent switching instants, as indicated in Tables 1 and 2. If S_1, S_2, S_3, or S_6 are defective, the RFLI can generate 3L on the output with a lower basic RMS value of output voltage. If the issue is in S_3, S_6, or S_7, the inverter shall provide the desired voltage and power, and the operation shall be restored to normal.

2.1. OC Fault in S_1 and/or S_2

The FLFLI cannot achieve a V_{DC} voltage level since this state contains just a single redundant state. Table 1 shows that the desired voltages of +0.5VDC, 0VDC, and -0.5VDC may be realized by employing state numbers c, e, and h. When this issue occurs, C_2 feeds the inverter to achieve fault tolerance. In this case, higher ripple voltage may be detected across C_1.

Table 1. Switching states of proposed RFLI

State	Voltage State	S_1	S_2	S_3	S_4	S_5	S_6
a	$+V_{DC}$	0	1	0	0	1	0
b	$+0.5V_{DC}$	0	1	0	1	0	0
c	$+0.5V_{DC}$	0	0	1	0	1	0
d	0	0	0	1	1	0	0
e	0	0	0	0	0	1	1
f	0	1	1	0	0	0	0
g	$-0.5V_{DC}$	1	0	1	0	0	0
h	$-0.5V_{DC}$	0	0	0	1	0	1
i	$-V_{DC}$	1	0	0	0	0	1

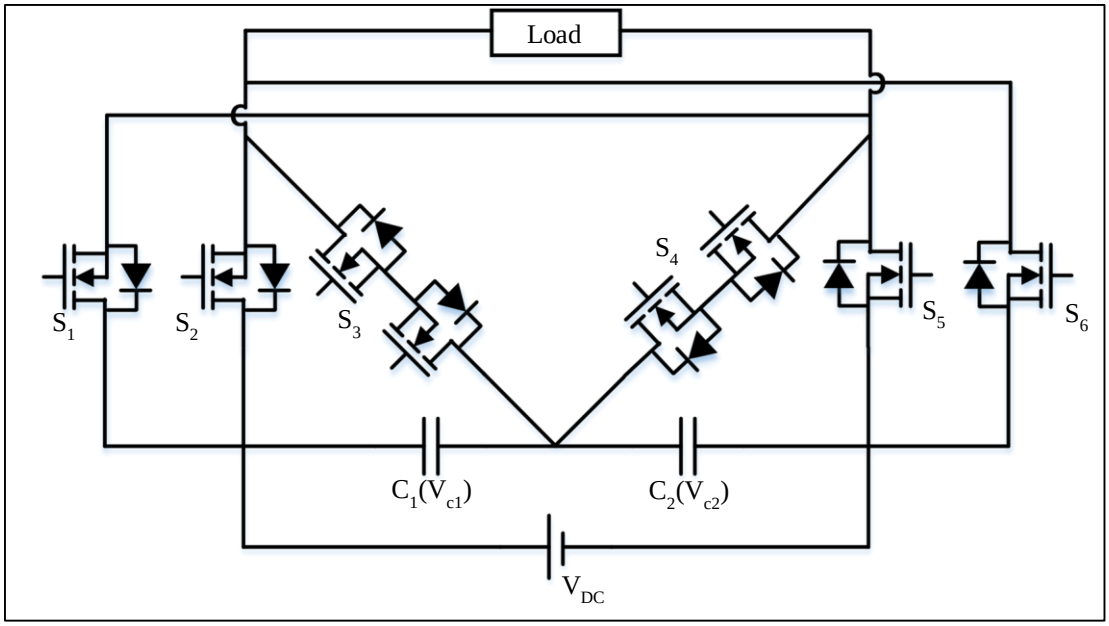

Fig. 2 Proposed Reliable Five Level Inverter (RFLI)

Table 2. Switching states under various fault conditions

Faulty Switch	Voltage State					Output Levels
	$+V_{DC}$	$+0.5V_{DC}$	0	$-0.5V_{DC}$	$-V_{DC}$	
Normal	a	b/c	d/e/f	g/h	i	5
S_1 and/or S_2	-	c	e	h	-	3
S_5 and/or S_6	-	b	f	g	-	3
S_3	a	b	e	h	i	5
S_4	a	c	f	g	i	5

2.2. OC Fault in S_5 and/or S_6

In this circumstance, the inverter can only provide three levels (+0.5V_{DC}, 0V_{DC}, and -0.5V_{DC}). These voltage levels are to be achieved using the state numbers b, f, and g, as shown in Table 1. When this happens, C_1 alone feeds the inverter to provide FT operation. As a result, under this circumstance, there is a higher ripple voltage across C_1.

2.3. OC Fault in S_3 and/or S_4

In this case, the inverter outputs all the voltage levels. The voltage states may be realized by employing state numbers a, b, e, h, and i for an open circuit in S_3 and a, c, f, g, and i for an open circuit in S_4, as shown in Table 1. When this happens, the two capacitors supply power simultaneously, so there won't be much voltage ripple in your output voltage.

2.4. Voltage Balancing of Capacitors

The voltage balance will be obtained here by employing multiple redundant states of the suggested inverter, which has two redundant states during no-fault conditions, such as +0.5V_{DC} and -0.5V_{DC}. The method was devised by supposing a specific switch (Sf) malfunction and monitoring voltages across two capacitors. S_f, V_{C1} and V_{C2} are used as inputs to the method.

If V_{C1} is greater than V_{C2}, C_1 must be discharged until V_{C1} equals V_{C2} to preserve the capacitor voltage balance. So, to generate +0.5V_{DC} and -0.5V_{DC} voltage levels, C_1 will be employed as the source (state numbers b and g in Table 1). If V_{C2} is greater than V_{C1}, V_{C2} is used as a source to create +0.5V_{DC} and -0.5V_{DC} voltage levels (state numbers c and h, respectively, in Table 1) until V_{C1} equals V_{C2}. Voltage balancing is only possible under healthy conditions due to the availability of various redundant states for +0.5V_{DC}, -0.5V_{DC}, and 0V_{DC} voltage levels, but voltage balancing is not possible under S_3 and/or S_4 failure because there is only one redundant state for +0.5V_{DC}, -0.5V_{DC}.

3. Control Strategy

The control technique includes pre-calculated output current and voltage statistics for switch malfunction combinations. S_f serves as a control indicator for the level generation blocks. If S_f is 0/3/4, the inverter may function in 5-level mode; otherwise, if S_f is 1 and/or 2 (or) 5 and/or 6, the inverter can work in 3L mode. The sinusoidal PWM approach is employed in all modes to create control pulses. To make 'n' levels in output side AC voltage, this approach requires one orientation and 'n' levels shifted in-phase carriers.

4. Results and Discussion

The DC voltage is 330V to create an AC voltage of 230V at an inverter side the simulation parameters of C_1=C_2=220µF, F_c=1500Hz, R_L=75Ω and L_L=50mH. FTMLI's performance is calculated in terms of efficiency and losses. The loss study was performed by building a thermal model of the IGBT switch. MATLAB/Simulink software in the proposed RFLI gives efficiency of 95.5% and THD of 20.96%. Figures 3 and 4 show the capacitor voltages (V_{C1}, V_{C2}) and voltage difference waveforms under typical operating conditions. Figures 5-10 illustrate the corresponding output voltages and voltages, as well as the defective switch currents, for the default and post-failure scenarios. Faulty S_1, S_2 and S_5, S_6 and S_4 switches are assumed at the 0.06-second mark, and associated problematic modules are replaced at the 0.14-second mark. Table 3 displays the total component count for the proposed architecture, which includes switching devices, diodes, capacitors and DC sources. It was observed that the component count was higher in [10, 11] than in [13, 16].

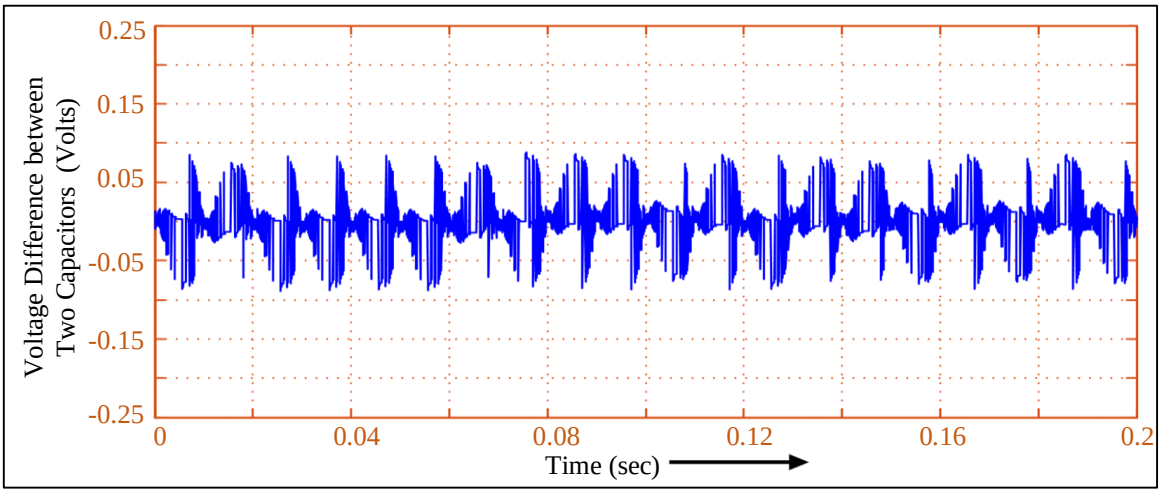

Fig. 3 Capacitor voltage differences during normal conditions

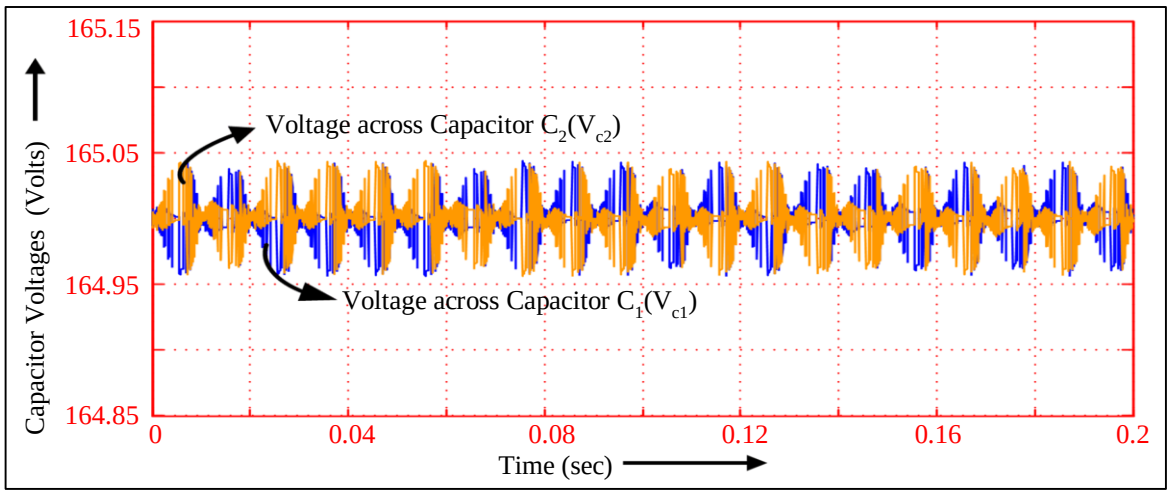

Fig. 4 Capacitor voltages during normal conditions

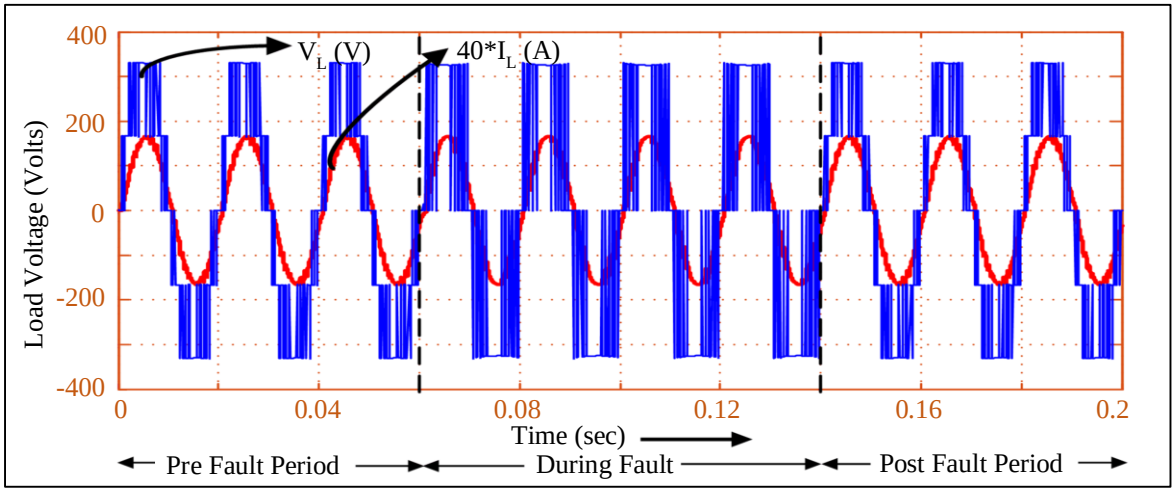

Fig. 5 Load current and load voltage waveforms for fault in S_1 and/or S_2

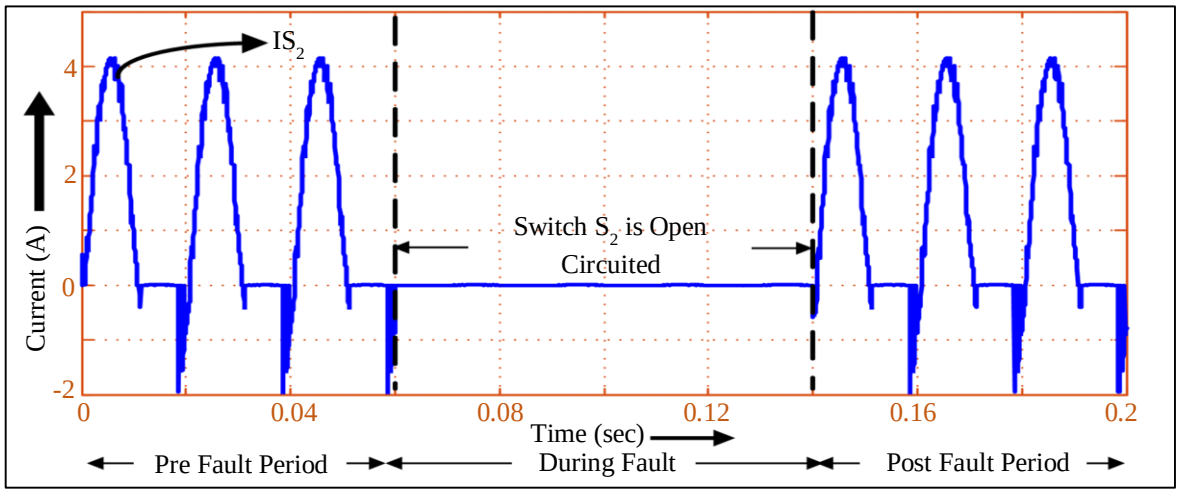

Fig. 6 Switch S_2 current waveform for fault in S_1 and/or S_2

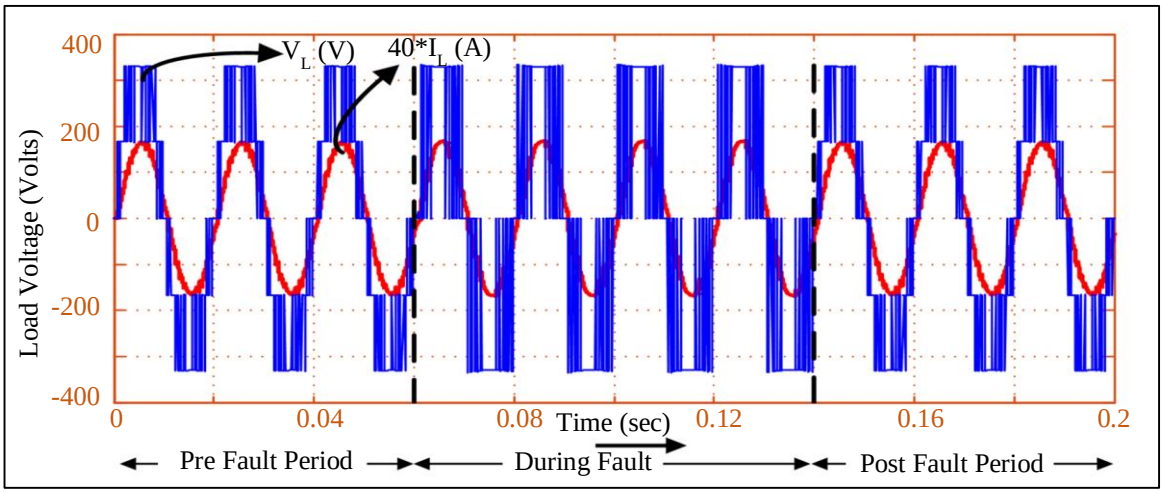

Fig. 7 Load current and load voltage waveforms for fault in S_5 and/or S_6

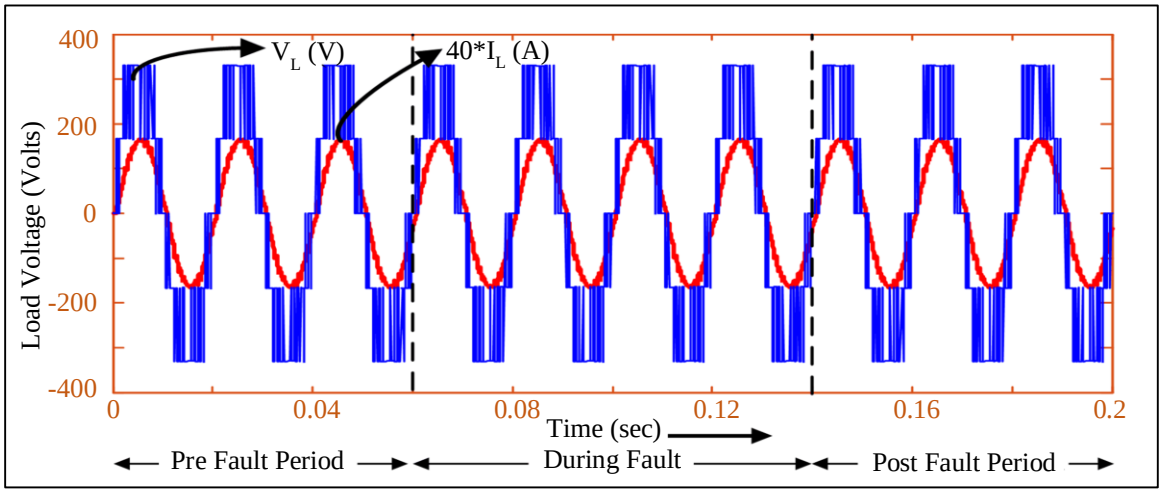

Fig. 8 Load current and load voltage waveforms for fault in S_3

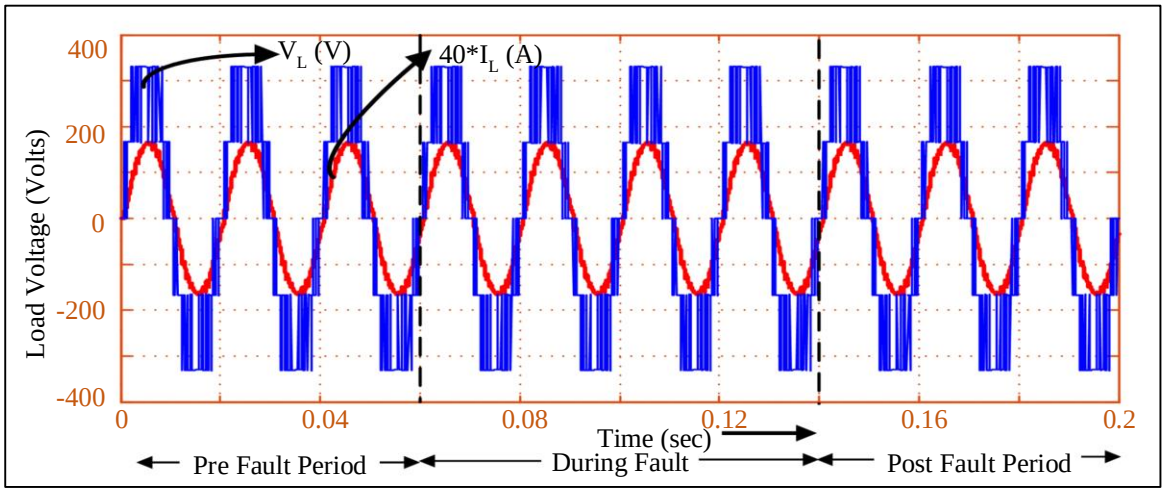

Fig. 9 Load current and load voltage waveforms for fault in S_4

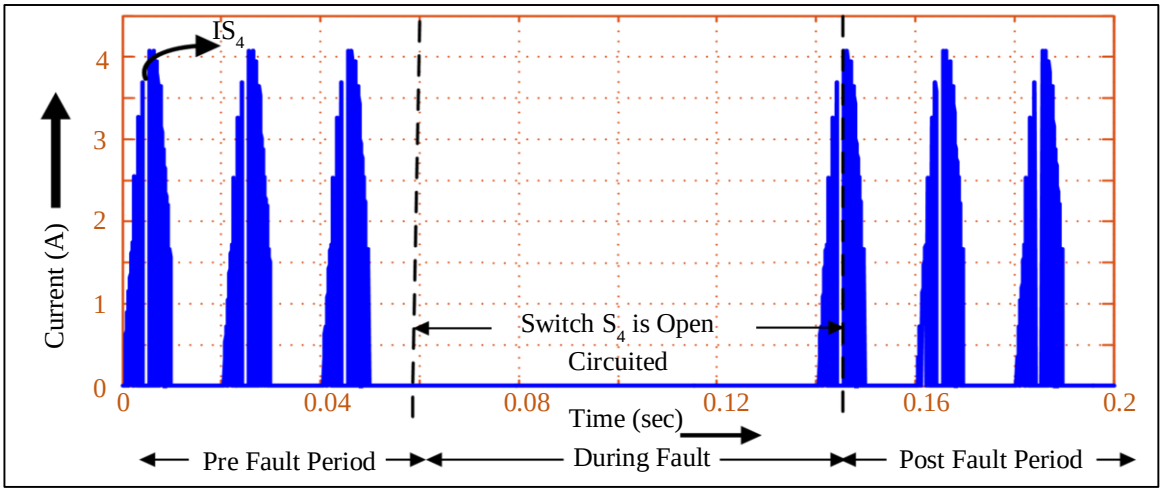

Fig. 10 Switch S_4 current waveform for fault in S_4

Table 3. Comparison of RFLI with existing topologies

Topology	IGBTs	4 Quadrant Switches	Diodes	Capacitors	DC Sources	Reliability
[17]	6	9	2	0	2	No
[19]	6	1	12	0	4	Yes
[20]	20	0	0	0	4	Yes
[22]	22	0	0	7	1	Yes
RFLI	4	2	0	2	1	Yes

5. Conclusion

This paper proposes a novel architecture for an increased Reliability fault tolerant single phase Five Level Inverter (RFLI). It can withstand an open circuit failure in any switch and certain multiple switch combinations. For capacitor voltage balancing, a control algorithm is incorporated. The capacitor voltages are correctly balanced, with a voltage differential of roughly 0.1 volts between the two capacitor voltages. An inverter's output voltage is always equal to the rated voltage. The proposed RFLI is validated in MATLAB Simulink platforms for various single/multiple open switch faults. A valid fault tolerant switching strategy is utilized with adequate fault clearance to obtain the necessary output voltage waveforms to achieve the reliability of the RFLI. The suggested FTFL inverter contains fewer devices than existing similar FTMLI topologies.

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