

Original Article

Design and Analysis of Low Power Hybrid Logic Adder for Signal Processing Applications

Amgoth Laxman¹, N. Siva Sankara Reddy², B. Rajendra Naik³

^{1,3}Department of ECE, Osmania University, Telangana, India.

²Department of ECE, Vasavi College of Engineering, Hyderabad, Telangana, India.

¹Corresponding Author : amgothlaxman@gmail.com

Received: 18 August 2023

Revised: 20 September 2023

Accepted: 16 October 2023

Published: 31 October 2023

Abstract - The primary objectives of VLSI design have been to enhance efficiency, reduce power consumption and delay, and minimize area. The current investigation outlines our suggested approach for analyzing a 1-bit hybrid adder compared to different adders concerning power consumption, transistor count, and delay. Recent research introduces a novel method for designing a 1-bit adder utilizing hybrid logic. An evaluation of the circuit's efficiency has been carried out using the Mentor Graphics tool set. A statistical comparison has been conducted to examine the parameters of the course concerning the parameters of already-present adder circuits. The adder under consideration has been extended to support a width of four bits, thereby enabling an assessment of its potential for scalability. Simulation findings suggest that the proposed architecture demonstrates noteworthy performance enhancements regarding power usage and delay, leading to a comparatively low power delay product. The results obtained from the simulation illustrate that the suggested hybrid adder circuit offers a viable option for the data path structure in contemporary applications that operate at high speeds.

Keywords - Adder, Delay, Hybrid logic, Power consumption, Transistor count.

1. Introduction

The rapid advancement regarding transistor scaling has led to a significant increase in efforts to conduct research focused on the low-power implementation of electronic circuits. According to academic literature [1], there has been a substantial increase in the need for efficient electronic circuitry design. Contemporary image processing procedures, Digital Signal Processing (DSP) IC chips, and multiple other uses require substantial computation [2].

The investigation of crucial arithmetic computing components, such as adders, in approximate computation has been conducted. The issue of extended carry propagation strands is frequently encountered in traditional adders. The power consumption attributed to a substantial amount of glitches resulting from carry propagation has been identified as a crucial factor [3-5]. Given a uniform independent input distribution, triggering these extended carry chains is infrequent, resulting in their length being typically shorter than the adder's complete width [6].

Consequently, this leads to the impetus to re-evaluate current adder designs to introduce alternative versions that exhibit increased velocity and decreased power consumption, as cited in references [7, 8]. Addition constitutes a fundamental arithmetic operation extensively utilized in

contemporary computing applications. The 1-bit Full Adder (FA) has been widely recognized as the core component of binary addition, serving as the basic building block for designing adders with more considerable word lengths [9, 10]. Therefore, optimizing the functionality of FA is vital for enhancing the overall efficacy of microprocessors.

The adder circuit has been developed and operated using a singular logic style in the framework of pass transistor logic, with variations including the 10-dependency FA [11], the 12T adder [12], and the conventional CMOS logic-dependency FA [13]. Implementing pass transistor logic requires the inclusion of additional buffers to compensate for voltage degradation and recover the electrical signal to its original voltage supply levels [14]. The issue of voltage loss does not correspond with CMOS Adder.

Nevertheless, the substantial input impedance poses a significant challenge in CMOS full adder. Contemporary researchers are inclined to employ a hybrid design methodology incorporating the advantageous features of multiple logic designs within a single FA cell. The utilization of Transmission Gates (TGs) in the architecture is observed in the TG Adder (TGA), as documented in references [15, 16], as well as in the Transmission Function Adder (TFA), as reported in relation [17]. Although TGA and TFA exhibit



immunity to voltage degradation, their limited capability remains a significant issue. Subsequently, numerous studies on hybrid full adders have been reported with the aim of minimizing area, latency, and power consumption [18-22]. Utilizing static inverters at the outputs yields improved driving capacity and increases power consumption. This architecture exhibits deficiencies regarding energy economy and complete logic swing unless buffers are employed.

Nevertheless, most hybrid adder architectures exhibit enhancement in one performance characteristic, such as power, area, and speed, at the cost of compromising the others. Due to the lack of current 1-bit adder architectures in the research that demonstrate reliable functioning in delivering a complete logic swing while being area and energy-efficient at Ultra-Low Voltage (ULV) levels, it is necessary to investigate alternative design techniques.

The present study introduces a novel hybrid adder that employs the cross-coupled logic of PMOS and NMOS transistors based on XOR and XNOR gates. The implementation of the FA has been carried out utilizing 45 nm technology along with Mentor graphics tools. A comparative analysis of the performance factors is conducted on the suggested and existing FA designs using various supply voltages to assess their reliability.

Furthermore, adders have been expanded to encompass adders with extensive word lengths to evaluate their performance characteristics in circuits of significant size. The efficacy of the proposed hybrid logic adder was observed to be remarkable when compared to the presently accessible FAs. Section 2 presents the literature survey related to the adders. In section 3, the proposed hybrid logic adder is explained. In section 4, simulation results are demonstrated, followed by a conclusion in section 5.

2. Literature Survey

In previous years, various logic models have been suggested to build 1-bit adder modules [9-22]. There have been two different sorts of 1-bit full adders regarding their logic architecture. One style is characterized as static, while the other is considered dynamic. Static full adders have been typically characterized by their superior reliability, simplicity, and reduced power consumption compared to dynamic 1-bit full adders.

Dynamic logic is a logical style that can be used as a substitute to build a logic operation. Compared to the static method, the dynamic approach has several benefits, including quicker switching rates, no idle power usage, complete swing potential levels, and reduced transistors. A logic circuit with N inputs necessitates $N+2$ transistors, whereas the conventional CMOS logic needs $2N$ transistors.

A dynamic CMOS gate's size advantages arise from using a single transistor in its PMOS network. Additionally, this leads to a decrease in the capacitance load at the outputs, which forms the groundwork for the delay benefit. The 1-bit full adder is primarily associated with several concerns, including power usage, efficiency, area, noise immunity, and driving capability.

Several researchers have integrated these two architectures and suggested hybrid static-dynamic 1-bit full adders. Various ways have been examined for implementing adders utilizing CMOS technology, each with advantages and disadvantages. The low-area approximation full adder suggested by Seyed Erfan Fatemeh et al. [18] is based on static CMOS circuitry.

In this paper, a low-power approximation complete adder cell featuring the needed energy scalability is constructed. The suggested cell was created using a 1-bit adder to create a 4-bit RCA. The area and energy use were then analyzed using various supply values. The temperature was also an essential aspect of the conceptual framework to ensure that the addition process ran well. Nevertheless, the approximation adder produces results with significant deterioration owing to supply voltage variations.

Mehedi Hasan et al. [19] suggested a flexible, low-power, 1-bit hybrid adder for rapid processing. FA was accomplished in this study using pass transistors and the transmission gate using CMOS semiconductor technology. Cadence software was used for modelling execution as well as design.

The suggested FA was created for 64-bit word width, and its ability to scale is often verified. To maintain the interim data, intermediary buffer phases were built. The FA architecture has been generated for several voltage settings ranging from 0.4 volts through 1.2 volts. The 64-bit word size caused a significant delay (523.8 ps) at a voltage of 0.4 V, affecting the design operation.

Jyothi Kandpal et al. [20] demonstrated an integrated logic full adder based on a 10T circuit. This study used the FA circuitry's effectiveness to determine the area, power, and delay. The transistor functions depend on the input values supplied to the transistors' gate terminals.

This study implemented the suggested model in cadence software using 90nm technology. Compared to existing modules, the result in terms of power and latency was lowered by up to 7.5%. Similarly, the PDP has been reduced by 2% to 28.13% compared to traditional systems. The amount of power used in the suggested design is substantial (30.4 uW) for a single-bit architecture because of exceptionally high threshold voltage transistors.

Mohammad Mirzaei and Siamak Mohammadi [21] suggested a process variation-aware full adder for imprecision-tolerant applications. In this study, three approximation adder circuits have been developed and used in the ripple carry adder, including the Sobel edge detection algorithm. According to the simulation findings, the suggested approach decreased power and latency by 6.2% and 42.3%, respectively. After detecting the sobel edge, the peak signal-to-noise proportion was calculated. The signal voltage has been reduced in the center of the circuit due to extra fan-out connectors.

Shivani Bathala and colleagues [22] suggested simulation-based criteria to assist power savings in digital circuits. The propagating glitches were avoided during the logic-level simulation in this study. The glitch elimination procedure was executed quickly and with a low iteration count. The circuit was simulated in the cadence genus of 55nm technology, and the results were confirmed. Python-level programming was used to implement the algorithm. The program generated the runtime data, and timing analysis was also done. However, it was not feasible to eliminate the faults to increase system performance.

Based on the research review, two primary categories of solutions are commonly discussed: technology solutions and architectural approaches. The technological process offers a novel approach to circuit architecture, while the architectural approach involves adjusting the circuitry to accommodate the required modifications in the scaling technologies.

Diverse methodologies are documented in the research to surmount the design obstacles encountered with low supply voltages. To address the challenges and issues faced within CMOS sub-micron technological advances, novel technological developments and architecture circuitry have been devised while ensuring minimal increase in complexity.

The literature describes many modifications to adder designs to effectively manage and improve efficiency characteristics like power and area according to the specific application requirements. Currently, most applications prioritize minimal power consumption, as numerous devices are designed to be battery-powered.

Furthermore, the advancement in healthcare electronics has led to a significant role being played by implanted devices. The power usage of the electronic circuitry is a critical factor for both battery-operated and embedded devices. As CMOS technology scales down, the supply voltage decreases, restricting the maximal voltage swing. Furthermore, with CMOS submicron innovations, the scaling

down of the threshold voltage does not occur at an identical rate as the technological advances and the supply voltages.

Implementing adders within CMOS sub-micron technologies has numerous obstacles and challenges in obtaining low power consumption at low supply voltages.

While various architectures are employed in Integrated Circuits (ICs) for diverse purposes, developing novel architectures or adapting current ones to enhance performance attributes and tackle varied challenges is imperative

3. Proposed Design of 1-Bit Adder

The design methodology utilized for the proposed functional architecture is illustrated in Figure 1. The proposed FA’s design has been categorized into four primary components, with two dedicated to the generation of carry. In comparison, the remaining two components are allocated to sum computation. Figure 2 depicts the schematic of the adder architecture proposed. The subsequent sub-sections furnish the design methodologies and a comprehensive delineation of the components.

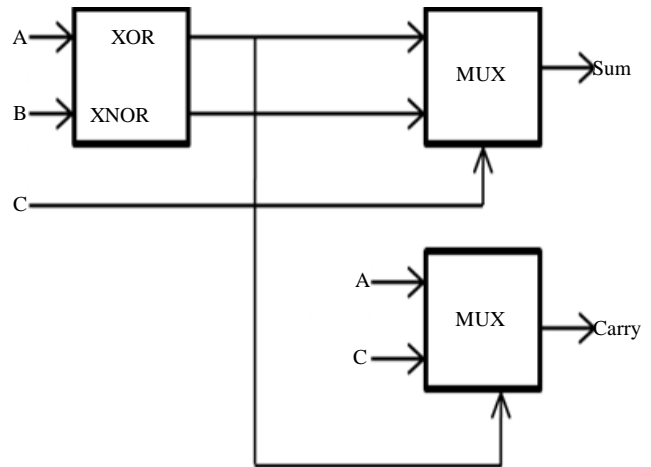


Fig. 1 Block diagram representation of proposed hybrid logic 1-bit adder

The sum of the proposed hybrid adder has been generating the following equation:

$$SUM = \overline{(A \text{ XOR } B)} C + (A \text{ XOR } B)\overline{C} \quad (1)$$

The sum result produced by the hybrid adder design is achieved through the sequential connection of the hybrid XOR/XNOR and multiplexer modules. The XOR and XNOR operations are carried out in the hybrid XOR and XNOR module, followed by a mux.

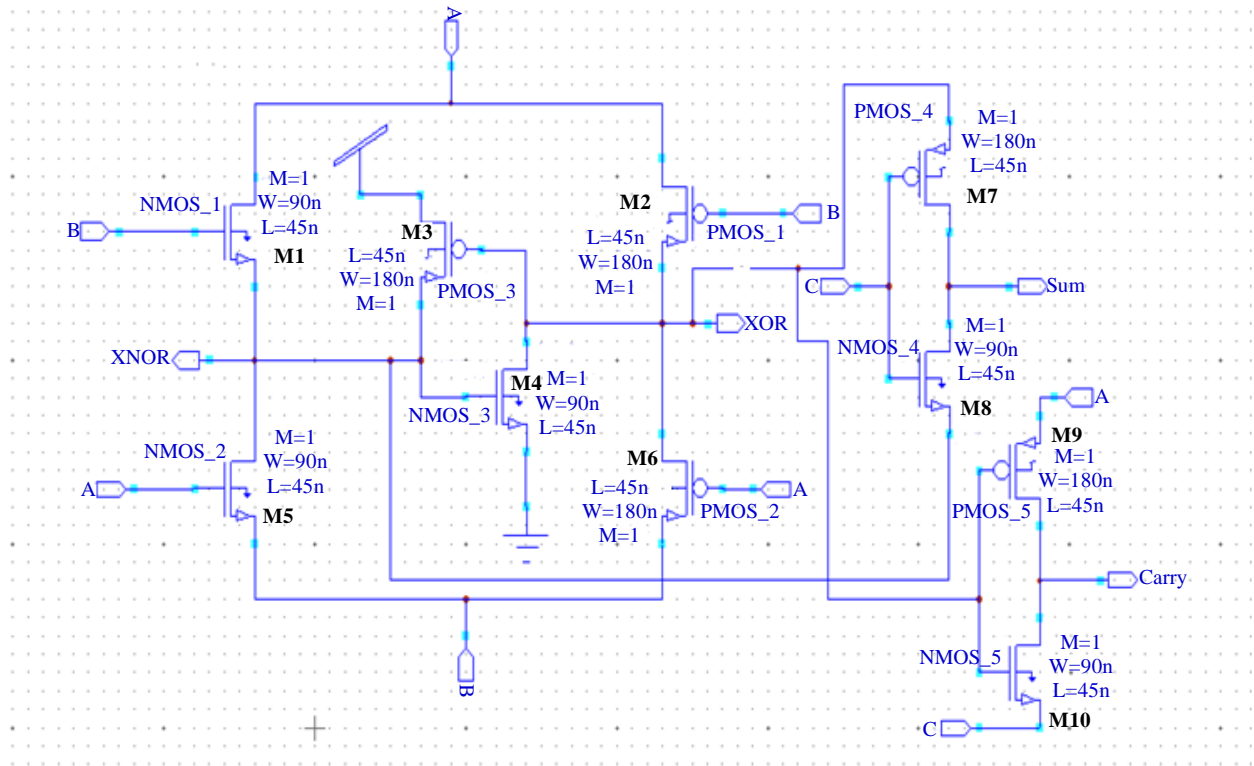


Fig. 2 Proposed schematic of hybrid 1-bit adder

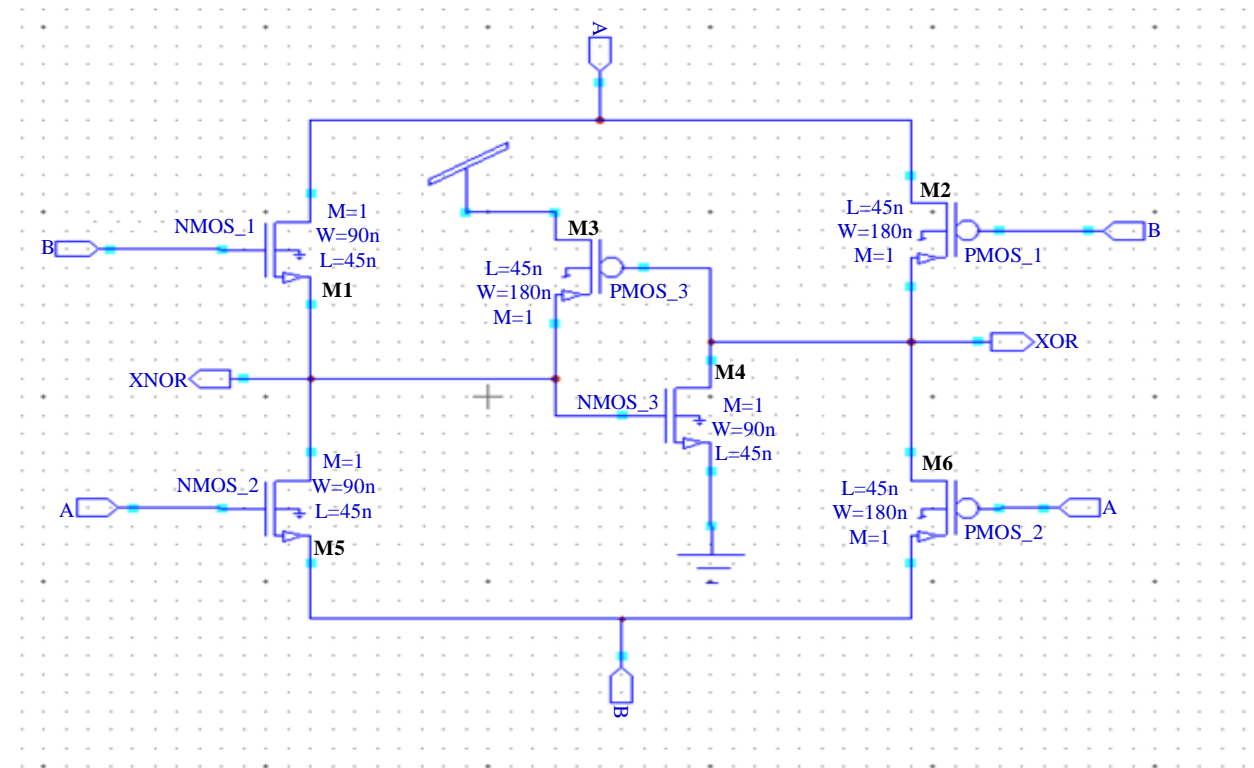


Fig. 3 Proposed hybrid XOR/XNOR module

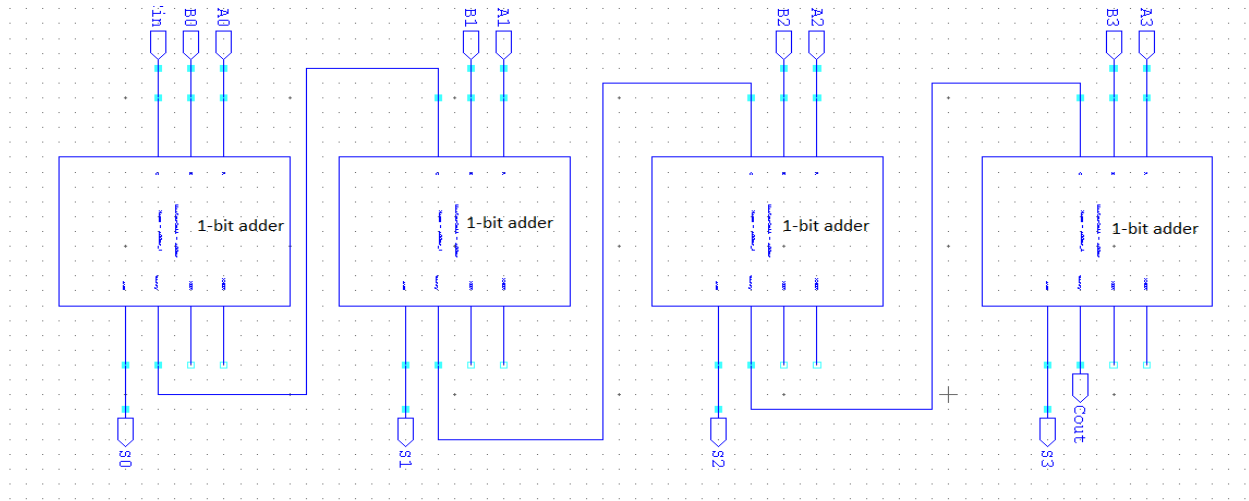


Fig. 4 Schematic diagram of 4-bit adder

The transistors M1–M6 form the hybrid XOR/XNOR module, whereas the transistors M7 and M8 act as the 2–1 MUX. The carry of the proposed hybrid adder has been generating the following equation:

$$\text{Carry} = \overline{A \text{ XOR } B} + C \text{ (A XOR B)} \quad (2)$$

The (A XOR B) output signal acts as the selection input for the MUX, with the two inputs of the mux being A and C. The transistors M9 and M10 act as the 2 to 1 Mux. Figure 3 illustrates the hybrid XOR/XNOR module that has been implemented. Figure 3 depicts a cross-coupled logic circuit comprising NMOS and PMOS transistors. The XNOR output can be obtained through the use of NMOS logic, while the XOR logic output can be achieved through the use of PMOS logic. The M3 and M4 transistors function as pass transistors, allowing the relevant logic output of M1 and M2 and M5 and M6 to pass through. To evaluate the scalability of the proposed method, it has been expanded into 4 bits using the Ripple Carry Adder method, as illustrated in Figure 4. An intermediate buffer was not incorporated during the process of cascading adders. The hybrid design under consideration is capable of functioning effectively when scaled up to a 64-bit configuration.

3.1. Design Considerations

The implementation of the proposed comparator involves the consideration of the following design factors.

3.1.1. Region of Operation

The current design utilizes the subthreshold operation region of MOSFETs to decrease supply voltage and power consumption. The progress of adders in ultra-deep submicrometer CMOS technologies is impeded by the low supply voltages, primarily caused by the absence of proportional scaling between the threshold voltages of the devices along with the supply voltages of current CMOS

processes [11]. Hence, the challenge of designing adders becomes progressively more complex with the reduction in supply voltage. Transistors are commonly operated within weak or moderate inversion regions to regulate low-power circuits effectively. The drain current is demonstrated as,

$$I_D = \frac{W}{L} I_{D0} e^{\frac{qV_{GS}}{nKT}} \quad (3)$$

The ratio of width to length of the transistor is denoted as W/L. The drain voltage is represented by ID, while ID0 refers to the reverse saturation current. The variable n represents the slope factor. The gate to source voltage is denoted as VGS. Additionally, the Boltzmann constant is defined by the symbol K, and T represents the room temperature. Utilizing a transistor within an inversion region has been explored in the unified all-regional framework, commonly called the ‘EKV model’. The model optimises Comparator noise and power, as described in references [13, 15, 17, 23]. The EKV configuration utilizes the following formulas to calculate the MOS device.

$$IC = \frac{I_D}{I_S} \quad (4)$$

$$I_S = 2\mu C_{ox} \frac{W}{L} \phi_t^2 \quad (5)$$

$$g_m = \frac{I_D}{\eta \phi_t} \frac{1 - \exp(-\sqrt{IC})}{\sqrt{IC}} \quad (6)$$

- Where, I_D - Drain Current
 I_S - Normalization Current
 C_{ox} - Oxide Capacitance
 η - Slope Factor is Taken as 1
 ϕ_t - Thermal Voltage
 IC - Inversion Coefficient

In this study, the value of IC is selected as 0.1 to ensure that the transistors operate within the weak inversion region. The determination of transistor dimensions is based on the model provided. Based on the EKV model, the transistor dimensions in the comparator are determined as demonstrated in Table 1.

Table 1. Dimensions of the transistors

Name of the Transistor	W/L Ratio
M1, M4, M5, M8, M10	2/1
M2, M3, M6, M7, M9	4/1

4. Simulation Results

This subsection provides the simulated outcomes and performance assessment of the recommended 1-bit full adder. The simulations have been conducted with the Mentor Graphics software, employing a 45 nm CMOS technological node with an Ultra-Low Voltage (ULV) of 0.8v to 1 V. The performance metrics of delay power, acquired from the simulated results, are examined with the corresponding metrics of other architectures documented in the research. Table 2 displays the simulated outcomes of the 1-bit full adders, including the quantity of transistors used. The entire 1-bit complete adder circuitry described in Figure 2 is consistently performed at a frequency of 20 KHz and a temperature of 27°C to ensure consistent comparisons. No supplementary buffers are included in either of the 1-bit full adder architectures to ensure equitable outcomes. The suggested 1-bit adders exhibit substantial enhancements in

delay and power characteristics. The subsequent analysis compares the efficiency of the 1-bit adders concerning each of these characteristics. The findings reveal that the recommended circuit performs better than the previously proposed circuits. Therefore, we will evaluate the performance in this section by comparing it with different simulation results. The investigation has effectively designed a new hybrid ten transistor 1-bit adder circuitry, including a hybrid XOR/XNOR unit and two 2X1 multiplexer circuits. The computations were performed using CMOS technology at a processing node of 45 nm and an operational potential of 0.8 V.

The objective is to use as little Power Delay Product as feasible. The simulations performed regarding delay, power, and Power Delay Product (PDP) at supply voltages of 0.8 V and 1.2 V are shown in Table 2, Figures 5 and 6. According to the findings, the proposed adder excelled in power and PDP. Even though perhaps the proposed architecture does not reach the fastest possible speed, this value is small enough even for practical application on modern CPUs. This has also been demonstrated: whenever the supply voltage for FA cells goes below 0.8 V, delays become much longer. With the advancement of technological advances, the efficacy of connections is increasingly dependent on resistance as opposed to capacitance. The acquired results contrast with various well-established 1-bit adder concepts, including TGA, CMOS, and other hybrid adders, 10T adders, and GDI adder architectures reported in current literary work, as illustrated in Table 2.

Table 2. Comparative analysis of exiting adders compared to the proposed hybrid adder

References	No. of Transistors	Delay (ns)		Average Power (μ W)		PDP(10^{-15} J)	
		0.8V	1.2V	0.8V	1.2V	0.8V	1.2V
[11]	32	84.8	37.3	1.72	3.89	145.9	145.1
[13]	28	125.8	39.7	0.68	1.91	85.5	75.8
[15]	20	139.7	58.3	0.64	1.41	89.4	82.2
[17]	16	145.6	66.8	0.61	1.33	88.8	88.8
[23]	24	128.4	65.9	0.76	1.68	97.6	110.7
[24]	22	91.9	45.6	0.87	2.11	79.9	96.2
[24]	20	132.3	50.4	0.7	1.79	104.5	90.2
[25]	24	193.6	71.5	0.77	2.04	149.1	145.9
[26]	24	189.1	60.2	0.78	2.31	145.6	139
[27]	22	101.3	48.6	0.68	1.53	68.9	74.4
[28]	16	81.6	38.7	0.44	0.98	35.9	37.9
[29]	21	96.8	43.9	0.58	1.31	56.1	57.5
[29]	23	81.4	35.1	0.54	1.35	43.9	47.4
[30]	18	98.8	31.8	0.46	1.09	43.5	34.7
[30]	22	77.3	28.6	0.63	1.49	48.7	42.6
[19]	21	90.53	39.7	0.61	1.32	55.2	52.4
[19]	22	65.7	25.3	0.48	1.17	31.5	29.6
Proposed Hybrid Adder	10	50.10	27.86	0.0141	0.0479	0.706	1.334

By incorporating a hybrid logical xor/xnor circuitry and utilising GDI methodology-dependent multiplexers, the recommended design significantly improves overall efficiency, particularly regarding delay, power consumption and number of transistors.

The recommended method demonstrates a power usage which is at minimum 10% lower with a delay which is 25% less in comparison to the earlier documented systems. Furthermore, the proposed architecture accomplishes a full voltage range using exactly ten transistors. The main objective is to minimise the PDP as much as possible. The experimental outcomes indicate that the evaluated adder architecture demonstrated enhanced performance regarding delay and power. We have rippled the suggested 1-bit GDI-

HTL adder design to build 4-bit ripple carry adder structures, as illustrated in Figure 4, to test the efficiency of the proposed hybrid adder architecture in actual situations.

Carry propagation occurs from the very first to the final adder block. The layout of the proposed adder has been demonstrated in Figure 7.

As technology size has shrunk and fabrication complexity has risen, it has become essential to replicate comparators in several process corners, including FF, FS, TT, SF, and SS. Figure 8 compares the influence of process corner variation on delay and power consumption to demonstrate that the adder’s performance parameters vary very little across all process corners.

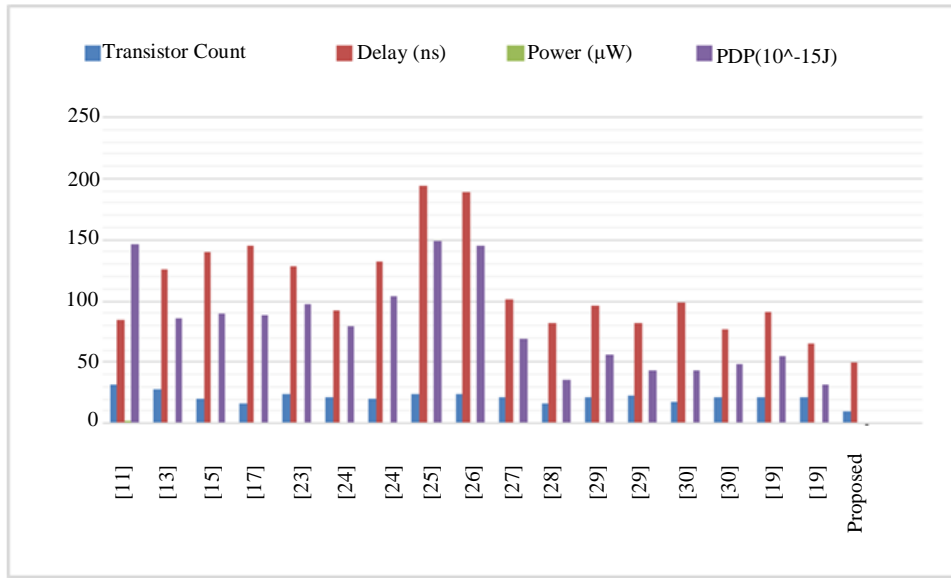


Fig. 5 Comparative analysis of exiting adder’s w.r.t to a proposed hybrid adder at a supply voltage of 0.8V

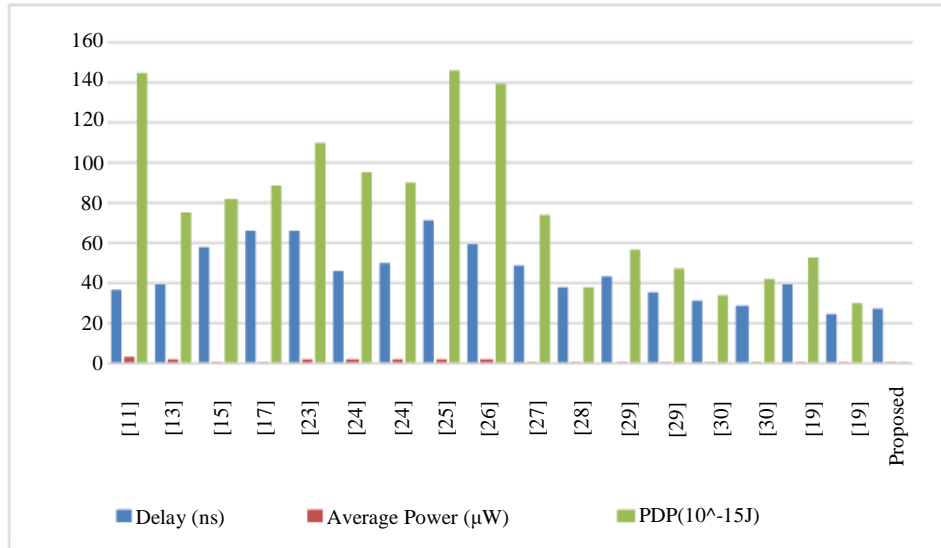


Fig. 6 Comparative analysis of exiting adders w.r.t to a proposed hybrid adder at a supply voltage of 1.2V

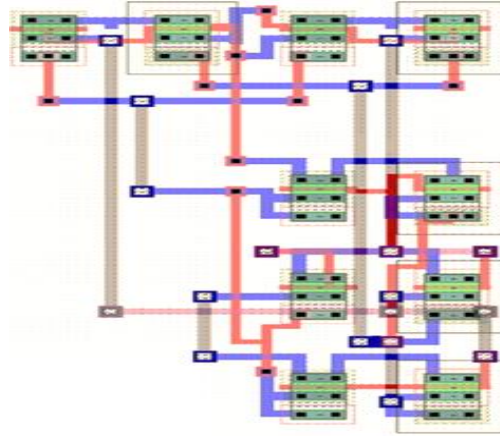


Fig. 7 Layout of proposed adder

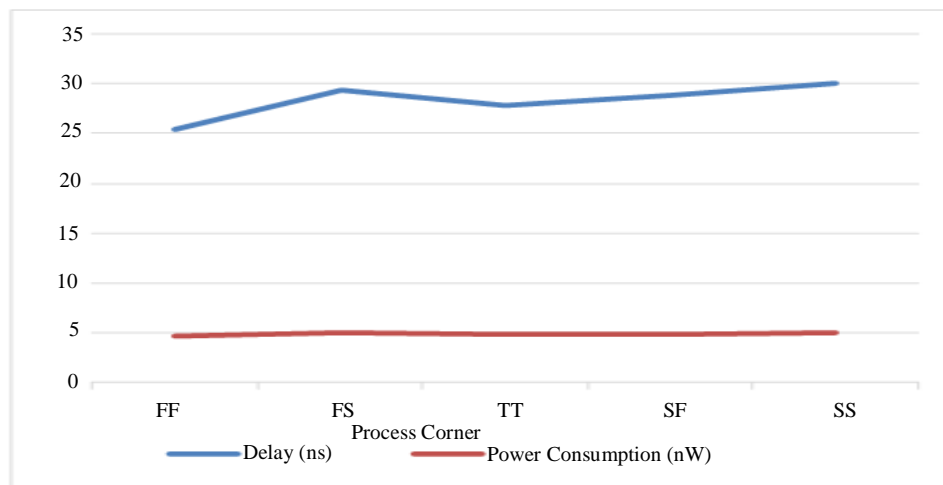


Fig. 8 Process corner variation on delay and power consumption for proposed adder

5. Conclusion

The current research introduces a newly developed hybrid adder design that exhibits significantly enhanced performance. A comparative analysis has been conducted between the proposed method and pre-existing adders to identify their respective characteristics. A simulation was carried out to assess performance utilizing the Mentor graphics toolset. According to the simulation outcomes, the

suggested adder exhibits exceptional efficiency in terms of speed and PDP when functioning as an isolated cell. Furthermore, the adder has been expanded to accommodate a maximum word length of 4 bits to assess its scalability. The findings derived from the performance metrics demonstrate that the proposed design is better suited for performing adders with more considerable word lengths in a cascading configuration.

References

- [1] Fabio Frustaci et al., "Designing High-Speed Adders in Power-Constrained Environments," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 2, pp. 172-176, 2009. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [2] Ajit Pal, *Low Power VLSI Circuits and Systems*, Springer India, New Delhi, 2015. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [3] Ning Zhu, Wang Ling Goh, and Kiat Seng Yeo, "An Enhanced Low-Power High-Speed Adder for Error Tolerant Application," *Proceedings of the 2009 12th International Symposium on Integrated Circuits*, Singapore, pp. 69-72, 2009. [[Google Scholar](#)] [[Publisher Link](#)]
- [4] Alberto A. Del Barrio et al., "Applying Speculation Techniques to Implement Functional Units," *2008 IEEE International Conference on Computer Design*, Lake Tahoe, CA, USA, pp. 74-80, 2008. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [5] B. Krishna Naga Deepthi, and M.V. Subramanyam, "Analysis and Optimization of Power Consumption and Area of Domino Full Adder," *SSRG International Journal of VLSI & Signal Processing*, vol. 2, no. 2, pp. 14-19, 2015. [[CrossRef](#)] [[Publisher Link](#)]

- [6] Kai Du, Peter Varman, and Kartik Mohanram, "High Performance Reliable Variable Latency Carry Select Addition," *2012 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Dresden, Germany, pp. 1257-1262, 2012. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [7] Darjn Esposito et al., "Variable Latency Speculative Han-Carlson Adder," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 5, pp. 1353-1361, 2015. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [8] Omid Akbari et al., "RAP-CLA: A Reconfigurable Approximate Carry Lookahead Adder," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 8, pp. 1089-1093, 2018. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [9] Basant Kumar Mohanty, "Efficient Fixed-Width Adder-Tree Design," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 2, pp. 292-296, 2019. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [10] Sohan Purohit, and Martin Margala, "Investigating the Impact of Logic and Circuit Implementation for Full Adder Performance," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 20, no. 7, pp. 1327-1331, 2012. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [11] R. Zimmermann, and W. Fichtner, "Low-Power Logic Styles: CMOS Versus Pass-Transistor Logic," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 7, pp. 1079-1090, 1997. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [12] Yingtao Jiang et al., "A Novel Multiplexer-Based Low-Power Full Adder," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 51, no. 7, pp. 345-348, 2004. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [13] Neil H.E. Weste, and David Money Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed., Addison-Wesley, Boston, MA, USA, 2010. [[Google Scholar](#)] [[Publisher Link](#)]
- [14] Amrutavarshini S.H., and S. Pramod Kumar, "High-Speed and Energy-Efficient Carry Skip Adder Functioning under a Extensive Range of Supply Voltage Levels," *SSRG International Journal of VLSI & Signal Processing*, vol. 4, no. 2, pp. 1-5, 2017. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [15] A.M. Shams, T.K. Darwish, and M.A. Bayoumi, "Performance Analysis of Low-Power 1-Bit CMOS Full Adder Cells," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 10, no. 1, pp. 20-29, 2002. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [16] Chip-Hong Chang, Jiangmin Gu, and Mingyan Zhang, "A Review of 0.18- μ m Full Adder Performances for Tree Structured Arithmetic Circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 13, no. 6, pp. 686-695, 2005. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [17] M. Alioto, G. Di Cataldo, and G. Palumbo, "Mixed Full Adder Topologies for High-Performance Low-Power Arithmetic Circuits," *Microelectronics Journal*, vol. 38, no. 1, pp. 130-139, 2007. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [18] Seyed Erfan Fatemieh, Samira Shirinabadi Farahani, and Mohammad Reza Reshadinezhad, "LAHAF: Low-Power, Area-Efficient, and High-Performance Approximate Full Adder Based on Static CMOS," *Sustainable Computing: Informatics and Systems*, vol. 30, 2021. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [19] Mehedi Hasan et al., "Design of a Scalable Low-Power 1-Bit Hybrid Full Adder for Fast Computation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 8, pp. 1464-1468, 2020. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [20] Jyoti Kandpal et al., "High-Speed Hybrid-Logic Full Adder Using High-Performance 10-T XOR-XNOR Cell," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 6, pp. 1413-1422, 2020. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [21] Mohammad Mirzaei, and Siamak Mohammadi, "Process Variation-Aware Approximate Full Adders for Imprecision-Tolerant Applications," *Computers & Electrical Engineering*, vol. 87, 2020. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [22] Shivani Bathla, Rahul M. Rao, and Nitin Chandrachoodan, "A Simulation-Based Metric to Guide Glitch Power Reduction in Digital Circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 2, pp. 376-386, 2019. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [23] Chiou-Kou Tung et al., "A Low-Power High-Speed Hybrid CMOS Full Adder for Embedded System," *2007 IEEE Design and Diagnostics of Electronic Circuits and Systems*, Krakow, Poland, pp. 1-4, 2007. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [24] Mariano Aguirre-Hernandez, and Monico Linares-Aranda, "CMOS Full-Adders for Energy-Efficient Arithmetic Applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 19, no. 4, pp. 718-721, 2011. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [25] Sumeer Goel, Ashok Kumar, and Magdy A. Bayoumi, "Design of Robust, Energy Efficient Full Adders for Deep-Submicrometer Design Using Hybrid-CMOS Logic Style," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 12, pp. 1309-1321, 2006. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [26] Ilham Hassoune et al., "ULPFA: A New Efficient Design of a Power-Aware Full Adder," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 8, pp. 2066-2074, 2010. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [27] Reza Faghieh Mirzaee et al., "A New Robust and Hybrid High-Performance Full Adder Cell," *Journal of Circuits, Systems and Computers*, vol. 20, no. 4, pp. 641-655, 2011. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]

- [28] M.C. Parameshwara, and H.C. Srinivasaiah, “Low-Power Hybrid 1-Bit Full Adder Circuit for Energy Efficient Arithmetic Applications,” *Journal of Circuits, Systems and Computers*, vol. 26, no. 1, pp. 1-15, 2017. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [29] Pankaj Kumar, and Rajender Kumar Sharma, “An Energy Efficient Logic Approach to Implement CMOS Full Adder,” *Journal of Circuits, Systems and Computers*, vol. 26, no. 5, pp. 1-20, 2017. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]
- [30] Mohan Shoba, and Rangaswamy Nakkeeran, “GDI Based Full Adders for Energy Efficient Arithmetic Applications,” *Engineering Science and Technology, an International Journal*, vol. 19, no. 1, pp. 485-496, 2016. [[CrossRef](#)] [[Google Scholar](#)] [[Publisher Link](#)]