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Original Article

Dynamic Voltage Control in Multilevel Inverters with TAR PWM for Non-Uniform DC Inputs

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Abstract *- This research presents a significant advancement in inverter technology, potentially greatly enhancing voltage quality and reducing harmonic distortions in power systems. This research introduces a novel Pulse Width Modulation (PWM) strategy to improve the operational efficiency of a 7-Level Unequal Source Inverter (7LUSI) employing two DC sources in a 1:2 sequence. In contrast to the conventional Sinusoidal Pulse Width Modulation (SPWM) technique, this innovative PWM approach is intricately designed to improve voltage quality and overall harmonic spectra. The gate signal generation for this proposed PWM technique involves a modified PWM scheme that combines a Trapezoidal waveform with a Rectangular one (TAR) alongside a traditional triangular carrier waveform. These TAR level-shifted PWM schemes generate triggering pulses for the 7LUSI. Various performance metrics are evaluated across different modulation indices, and comparative results are presented in contrast to conventional PWM methods. The findings consistently demonstrate the superior performance of the proposed TAR PWM method over traditional SPWM. The simulation study is conducted using MATLAB-SIMULINK as the primary computational tool. This research represents a significant advancement in inverter technology, offering substantial potential to enhance voltage quality and reduce harmonic distortions in power systems.*

Keywords *- MLI, PWM, SPWM, TAR, THD.*

1. Introduction

Multilevel inverters are characterized by their ability to generate output voltages with more than two levels across their poles. This distinctive feature places Multilevel Inverters (MLIs) in the category of high-power inverters, as they can exceed the typical voltage levels of power semiconductor switches, offering advantages such as reduced distortion, lower dv/dt stress, and mitigation of common-mode voltage issues [1-4].

The cascaded H-bridge inverter stands out among various MLI topologies due to its modular structure. Nevertheless, it has a notable drawback: it requires many isolated DC supplies [5-8].

To address this limitation, the concept of hybrid multilevel inverters has emerged. These hybrid systems are constructed by cascading smaller, dissimilar inverter circuits, allowing for higher voltage levels without a proportional increase in the number of H-bridge cells in the cascade topology [9-12]. In recent developments [13], a multilevel inverter was designed by connecting sub-multilevel inverters in series, classifying it as 'Unequal'.

In this setup, varying DC sources were utilized within these sub-multilevel inverters. Another significant contribution [14] introduced an efficient hybrid optimal modulation technique tailored for multilevel inverters. A multi-carrier PWM-based single-phase inverter was developed, with real-time implementation using Xilinx FPGA.

Simultaneously, [15] introduced a hybrid multilevel inverter with fewer switches designed for PV power conditioning systems, while [16] presented a modified multilevel inverter design, effectively reducing the number of switches involved.

In [17], various carrier pulse width modulation techniques were explored to minimize Total Harmonic

Distortion (THD) and enhance inverter output voltages. Finally, in [18], novel multilevel inverter topologies were investigated, strategically reducing the multitude of power switches compared to traditional configurations. This innovative approach harnesses the potential of floating input DC sources, each capable of making a unique contribution, independently or collectively in series with other sources, for the intricate synthesis of multilevel waveforms [19-23]. This article focuses on investigating a single-phase 7LUSI employing a TAR modulating strategy.

The study encompasses comprehensive simulations using MATLAB-SIMULINK, including harmonic analysis and evaluating various performance metrics under varying modulation indices. The research findings are then meticulously reported and discussed.

2. Arrangement of 7LUSI

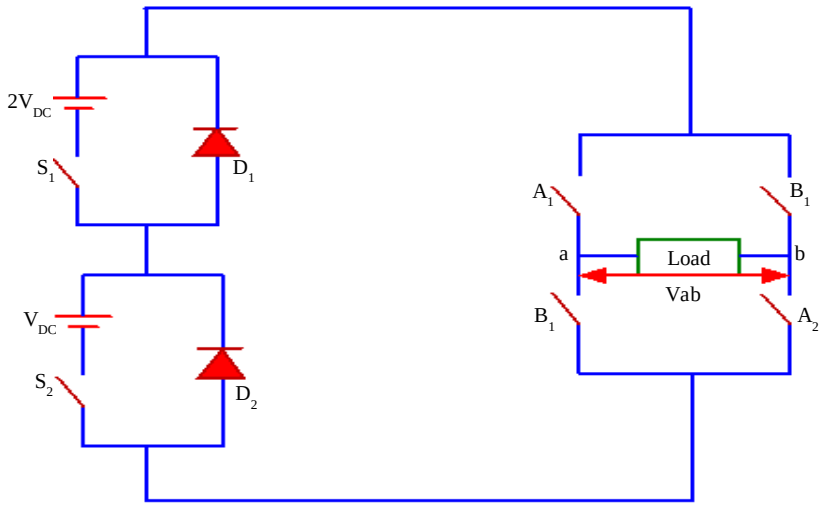


Fig. 1 Developed 7LUSI system

An asymmetric Multilevel Inverter (MLI), while sharing some similarities with the traditional cascaded H-bridge multilevel inverter, exhibits distinct characteristics that result in several significant advantages. Chief among these is its ability to expand significantly the available output voltage range, offering several valuable benefits:

- Reduced DC Sources: Notably, it accomplishes this with fewer DC sources, simplifying the system's overall complexity.
- Minimal Switching Loss: Asymmetric MLIs minimize switching loss, leading to improved efficiency in the conversion process.
- High Conversion Efficiency: This design naturally lends itself to high conversion efficiency, a crucial factor in power electronics.
- Output Standard Flexibility: The asymmetric setup provides a high degree of flexibility, allowing for adjustments in output standards to suit various applications.
- Reduced Circuit Complexity and Cost: With fewer components and switches, asymmetric MLIs can significantly reduce circuit complexity and overall cost.

In this study, we focus on a specific configuration known as the 7LUSI, composed of sub-multilevel inverters (referred to as low-power cells) in conjunction with an H-bridge inverter (serving as the high-power cell). These sub-multilevel inverters can be interconnected in a series arrangement to achieve the desired voltage levels.

Each sub-multilevel inverter has its dedicated DC source labelled as V_{DC} and $2V_{DC}$ and is constructed with two power devices: S_1 and D_1 for the first sub-multilevel inverter, and S_2 and D_2 for the second sub-multilevel inverter, as depicted in Figure 1. It's worth noting that switches S_1 to S_2 operate at lower voltage levels, using MOSFET technology, while the switches within the H-bridge (A_1, A_2, B_1, B_2) function at higher voltage levels, employing GTO technology.

The output voltage generated by the sub-multilevel inverters, either individually or in series, remains positive or zero. To function as an inverter, it is essential to reverse the voltage polarity in each half cycle. To achieve this, an H-bridge inverter is added to the output of the series of sub-multilevel inverters.

It's crucial to emphasize that the H-bridge switches must be designed to withstand higher voltage levels, a critical consideration in the inverter's design process. However, it's important to note that these switches undergo a single toggling event within a fundamental cycle, indicating their operation as high-voltage, low-frequency switches. The sub-multilevel inverter predominantly generates voltage levels around zero and in the positive domain. To attain zero output

voltage, switches A_1 and B_1 are simultaneously activated. In contrast, the various other voltage levels are produced by precisely manipulating the switch states, as detailed in Table 1, which provides the switch configurations required for generating each specific output voltage level.

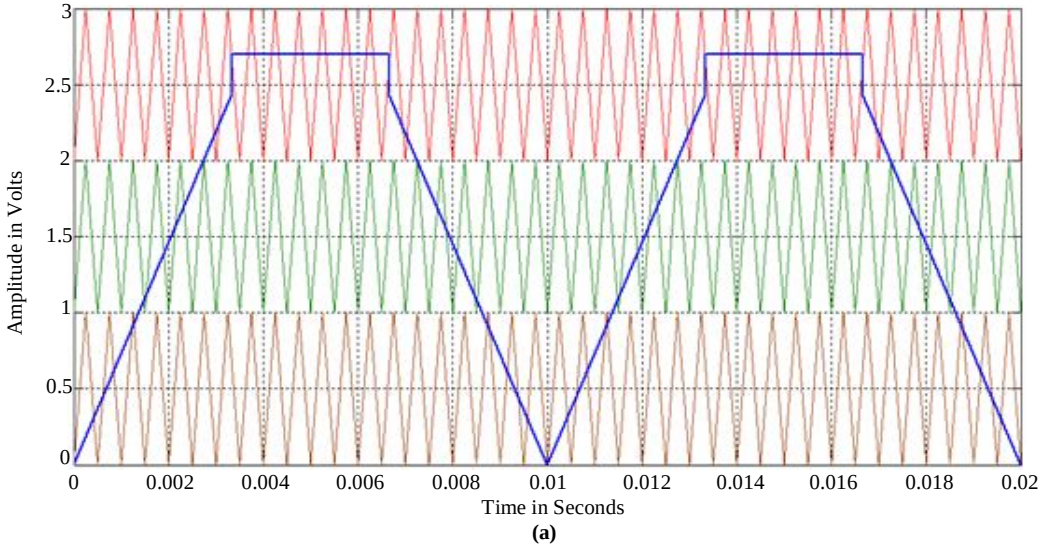
Table 1. Switching positions corresponding to positive levels

S1	S2	D1	D2	A1	A2	B1	B2	Vout
✓	✓	X	X	✓	✓	X	X	+3 V_{DC}
✓	X	X	✓	✓	✓	X	X	+2 V_{DC}
X	✓	✓	✓	✓	✓	X	X	+1 V_{DC}

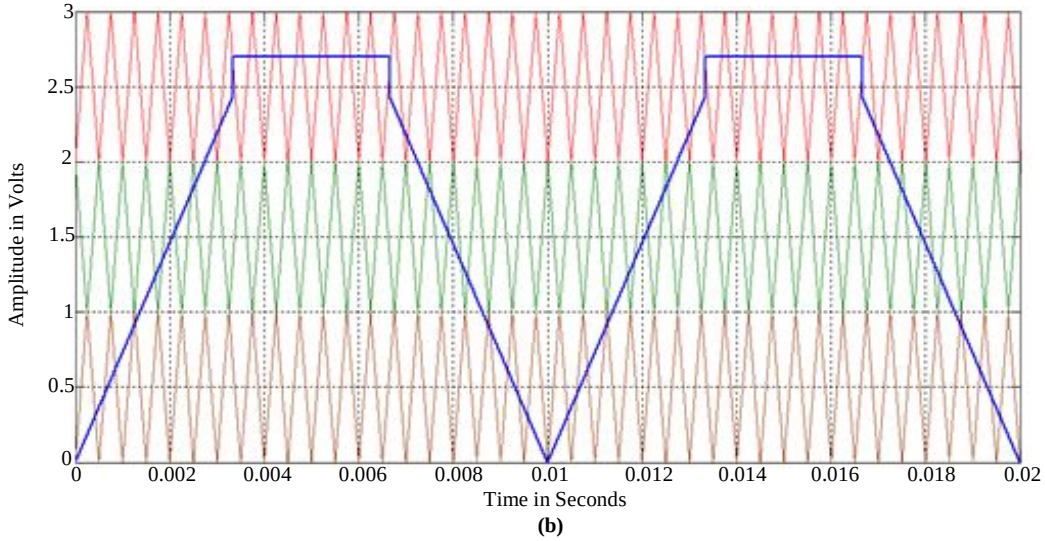
3. Employing the TAR PWM Method

In the proposed methodology, the generation of firing pulses for a 7-Level Unequal Source Inverter (7LUSI) relies on a rectified trapezoidal combined with a rectangular reference waveform, coupled with a triangular carrier, as visually depicted in Figure 2. What distinguishes this TAR PWM technique is its efficiency, as it necessitates only seven carriers tailored for the 7LUSI configuration. These carriers all operate at a consistent frequency, yet each possesses a distinct maximum magnitude compared to the others. Notably, the reference waveform is intentionally positioned exclusively above the zero-time line. Consequently, each carrier signal undergoes continuous comparison with the reference waveform. An initial driving pulse is generated whenever the modulating waveform surpasses the amplitude of the carrier signal. By employing appropriate logical circuits, these initial driving pulses are further processed to yield the precise firing pulses necessary for the operation of the 7LUSI.

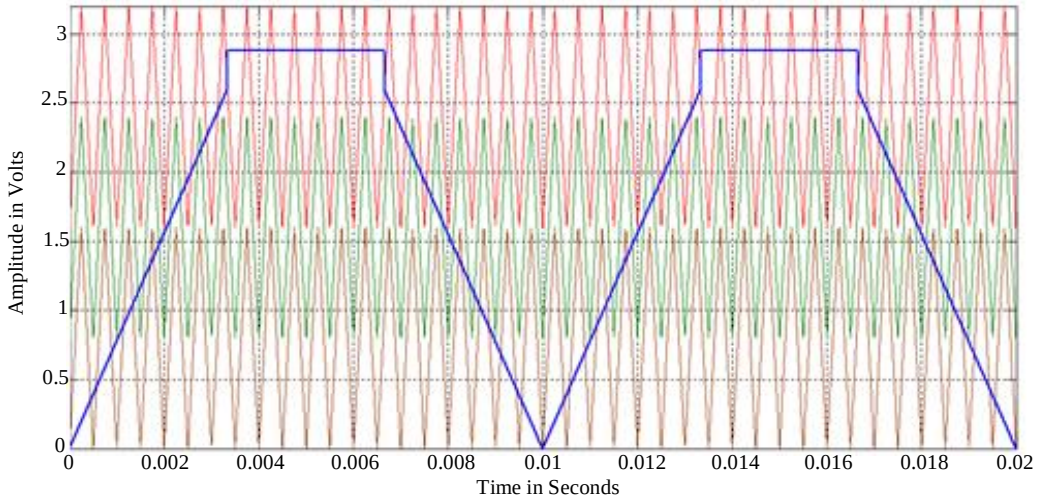
In this study, we have considered various Pulse Duration (PD), Amplitude Pulse Overlap Duration (APOD), Common Offset (CO), and Variable Frequency (VF) level-shifted PWM techniques. These techniques play a pivotal role in shaping the performance and behaviour of the 7LUSI, enhancing the depth and versatility of our investigation.



(a)



(b)



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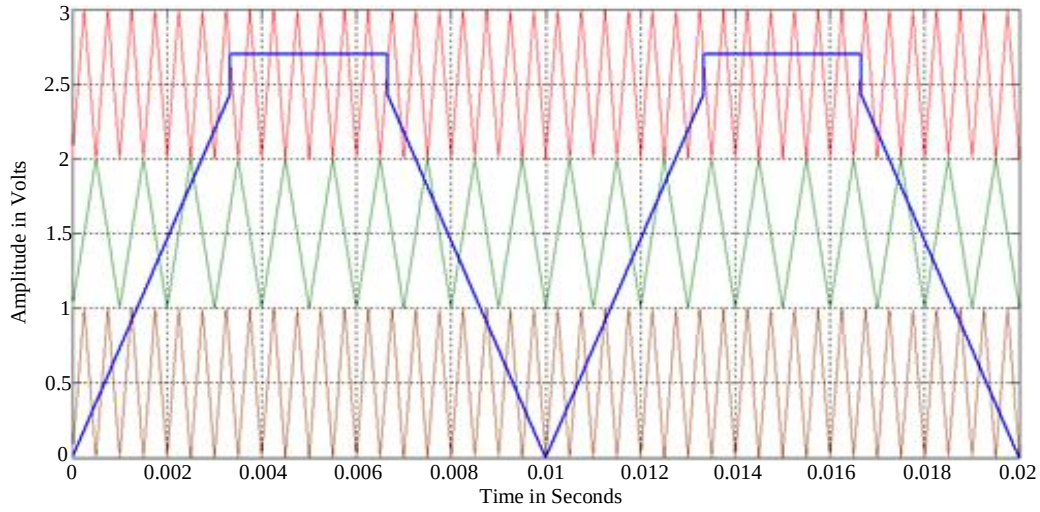

(d)

Fig. 2 TAR reference and carrier configurations of a) PD, b) APOD, c) CO, and d) VF approach.

4. Simulation and Experimental Results

In this research, we conducted a comprehensive simulation of a 7-Level Unequal Source Inverter (7LUSI) using MATLAB's SIMULINK, incorporating the power system block set. As previously discussed, the study generated switching signals through various multi-carrier unipolar Pulse Width Modulation (PWM) techniques. Simulations were carried out across a range of modulation indices (m_a) from 0.8 to 1.

The primary focus of the analysis was to evaluate the Total Harmonic Distortion (% THD) and Root Mean Square (RMS) values of the output voltage, with results tabulated for comparative purposes.

The essential simulation parameters included V_{dc} = 100V, R = 100 ohms (load), fc = 2000 Hz, and fm = 50 Hz. We employed the TAR PWM method and used conventional Sinusoidal PWM (SPWM) for reference.

We presented the simulation results as PWM output waveforms and Fast Fourier Transform (FFT) plots for the chosen 7LUSI configuration. To effectively illustrate the findings, we selected results for a sample m_a at 0.9 for all the considered references, emphasizing the PWM strategy with the least THD. Figures 3(a) and 3(b) depict the voltage output produced by the VF-PWM method, accompanied by its FFT plot.

Similarly, Figures 4(a) and 4(b) present the 7-level output voltage generated by APOD-PWM and its FFT plot. Figure 5 illustrates the prototype model of the proposed inverter. Additionally, Figure 6 showcases the output voltage achieved through CO-PWM and its FFT plot.

Lastly, Figures 7 and 8 reveal the output voltage obtained through Variable Frequency (VF-PWM) alongside its FFT plot. We summarized the THD results in Table 2, providing further insight into the Root Mean Square (V_{RMS}) of the

7LUSI output in Table 3 and the output voltage's Distortion Factor (% DF) in Table 4. For experimental validation, it has scaled down the simulation values to align with laboratory conditions. The peak-to-peak output voltage was measured at 36V in the lab, as demonstrated in Figures 7-10 and detailed in Tables 5 to 7.

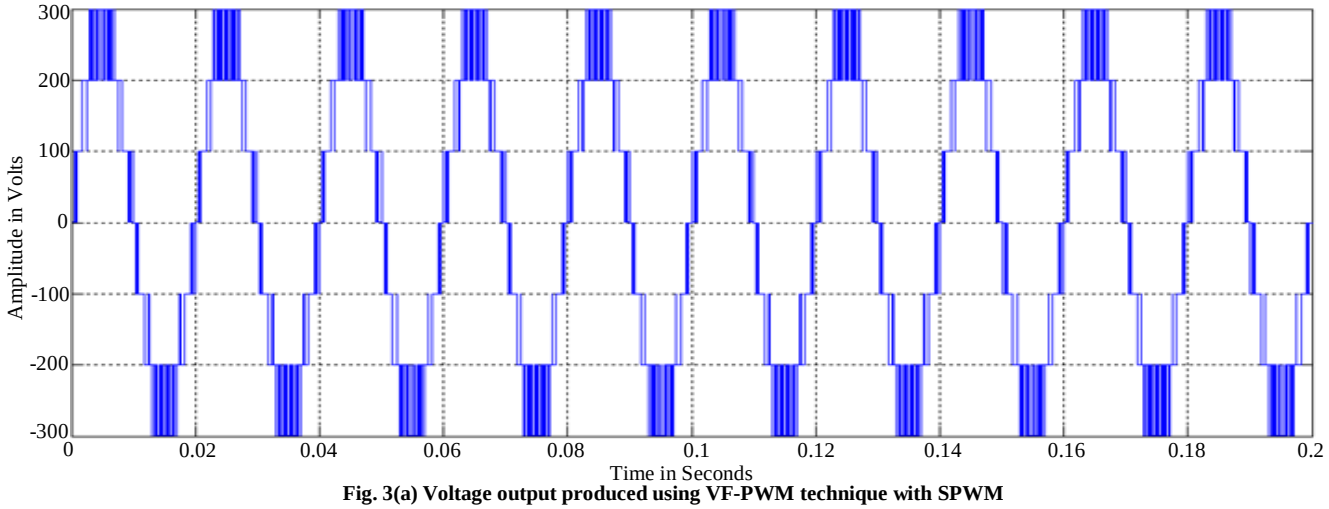

Fig. 3(a) Voltage output produced using VF-PWM technique with SPWM

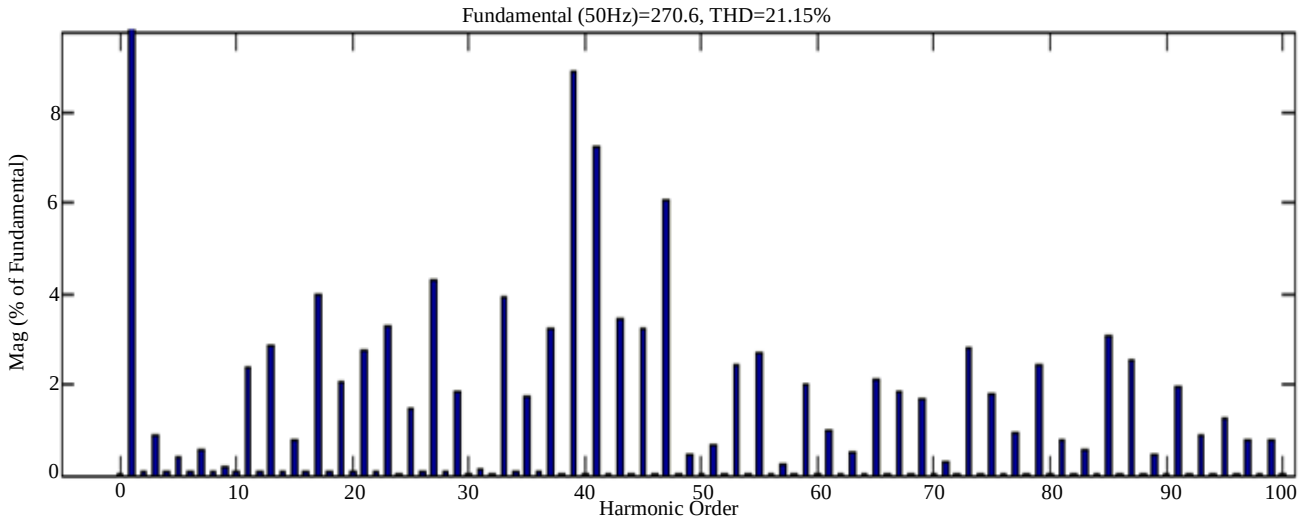

Fig. 3(b) Voltage FFT using VF-PWM

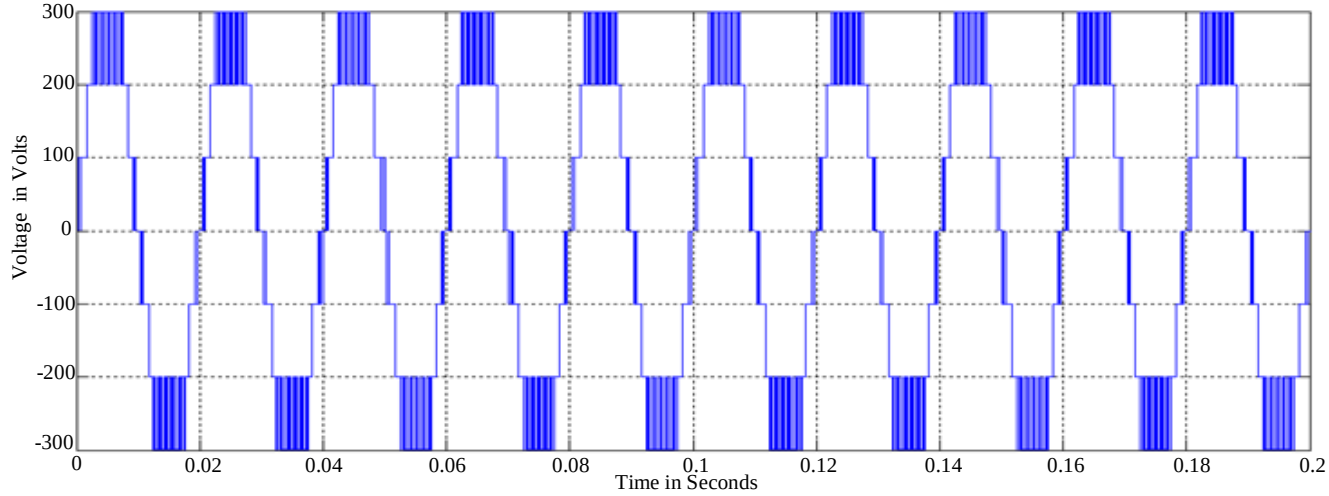

Fig. 4(a) Voltage output produced using VF-PWM technique with SPWM with TAR

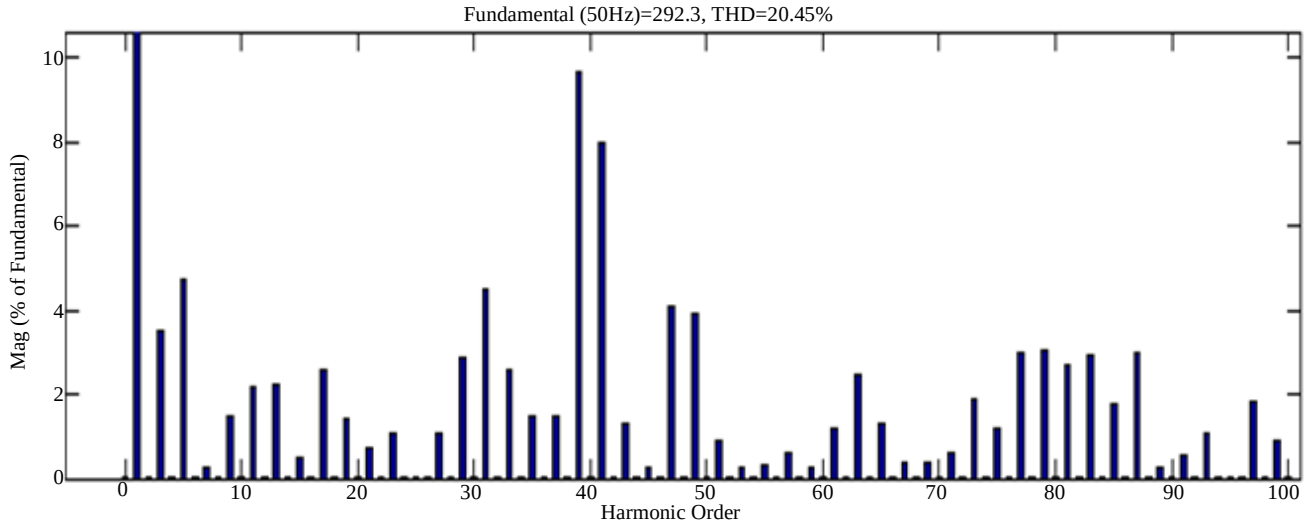

Fig. 4(b) Voltage FFT

Table 2. %THD in output voltage

m_a	Sine Reference				TAR Reference			
	PD-PWM	APOD-PWM	CO-PWM	VF-PWM	PD-PWM	APOD-PWM	CO-PWM	VF-PWM
1	17.29	18.22	22.49	16.58	15.53	15.67	21.16	14.15
0.95	20.41	20.22	25.21	18.85	19.14	19.08	23.55	17.94
0.9	22.10	22.04	27.6	21.15	21.54	21.19	26.01	20.45
0.85	23.41	23.22	29.81	23.55	23.52	23.42	28.35	23.13
0.8	24.22	24.15	32.36	24.53	24.71	24.82	30.43	25.21

Table 3. Output voltage of RMS

m_a	Sine Reference				TAR Reference			
	PD-PWM	APOD-PWM	CO-PWM	VF-PWM	PD-PWM	APOD-PWM	CO-PWM	VF-PWM
1	212.31	212.11	218.32	212.112	223.42	223.18	225.61	222.82
0.95	201.41	201.62	209.35	202.34	212.32	211.79	217.43	212.45
0.9	191.21	190.92	199.83	191.54	200.54	200.65	207.93	202.42
0.85	180.61	180.33	189.91	180.36	189.67	189.46	198.26	190.56
0.8	169.73	169.74	179.93	169.78	178.58	178.48	188.97	178.58

Table 4. Output voltage of DF

m_a	Sine Reference				TAR Reference			
	PD-PWM	APOD-PWM	CO-PWM	VF-PWM	PD-PWM	APOD-PWM	CO-PWM	VF-PWM
1	0.030	0.022	0.204	0.104	0.180	0.176	0.311	0.025
0.95	0.018	0.013	0.256	0.071	0.175	0.174	0.341	0.023
0.9	0.039	0.016	0.395	0.068	0.160	0.174	0.428	0.022
0.85	0.036	0.018	0.556	0.072	0.165	0.171	0.572	0.020
0.8	0.024	0.029	0.700	0.064	0.180	0.170	0.705	0.015

Significantly, Table 2 underscores that the VF-PWM approach utilizing the TAR reference achieves the lowest harmonic content in the output voltage.

Additionally, Table 3 reveals that the Carrier Overlapping (CO-PWM) technique with TAR reference optimizes the utilization of the DC bus, in contrast to other strategies that exhibit relatively lower utilization rates. Furthermore, Table 4 emphasizes that the VF-PWM method with TAR reference consistently maintains lower harmonics, significantly beyond the second-order attenuation, as indicated by % DF. We calculated the Crest Factor (CF) for all the strategies across various modulation indices to assess the stress imposed on the devices.

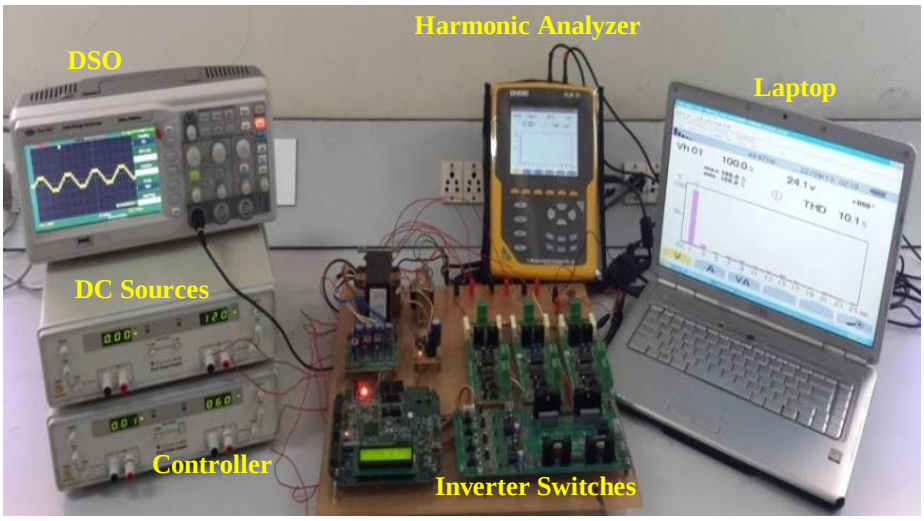

Fig. 5 Prototype representation of 7LUSI

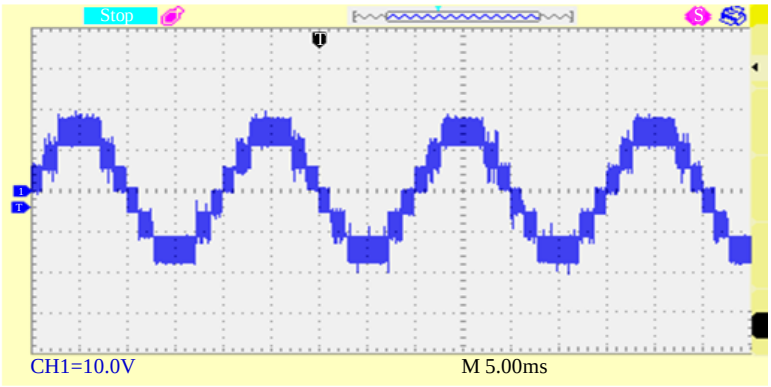

Fig. 6 Voltage output produced through PD-PWM method

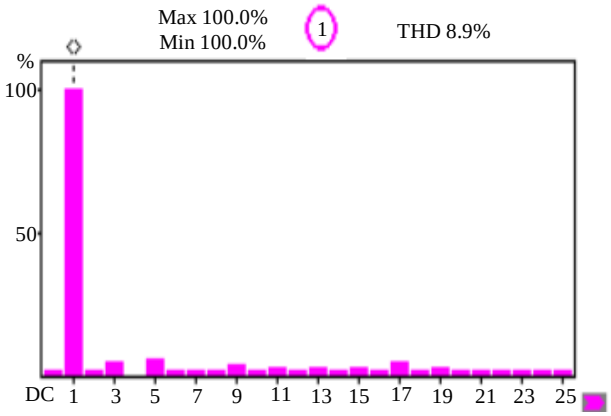

Fig. 7 Voltage FFT with PD-PWM

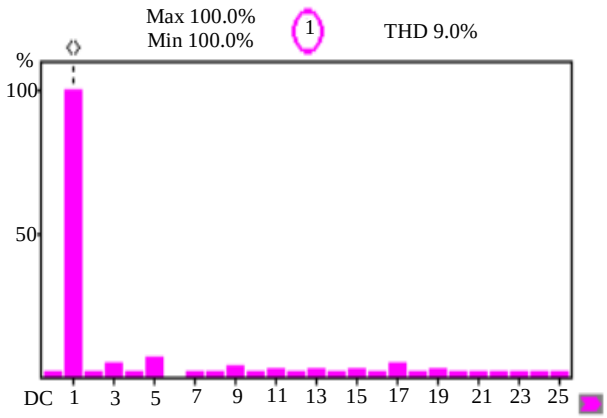

Fig. 8 Voltage FFT with APOD-PWM

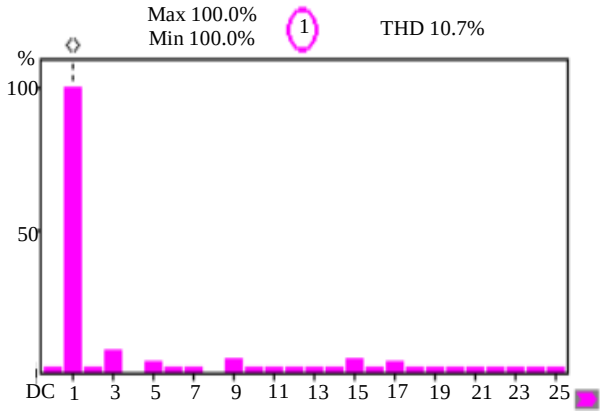

Fig. 9 Voltage FFT with CO-PWM

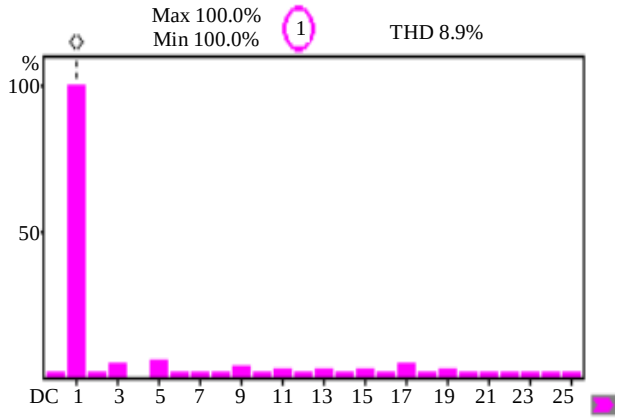

Fig. 10 Voltage FFT with VF-PWM

Table 5. %THD of output voltage with experimental results

m_a	PD-PWM	APOD-PWM	CO-PWM	VF-PWM
1	8.1	8.4	9.3	8
0.95	8.6	8.8	9.8	8.4
0.9	8.9	9	10.7	8.9
0.85	9.5	10	10.9	9.5
0.8	9.7	10.2	11.1	9.7

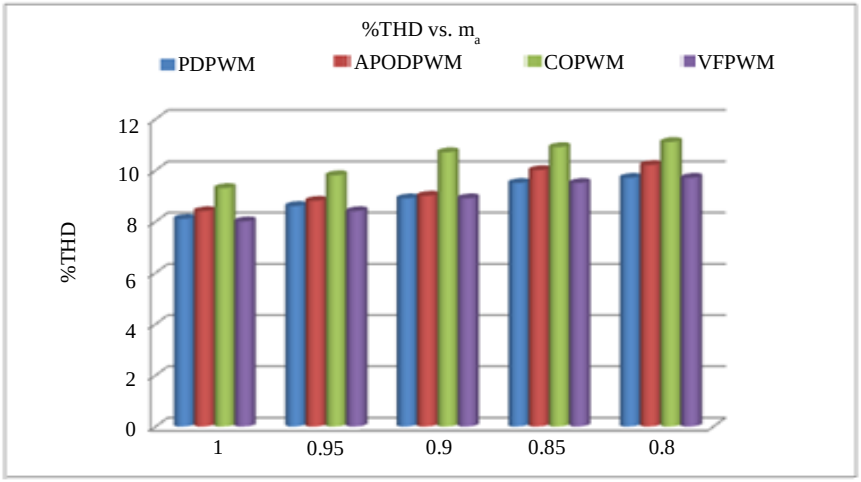

Fig. 11 Total Harmonic Distortion percentage in output voltage as a function of output current (experimental data)

Table 6. Output voltage RMS concerning output current

m_a	PD-PWM	APOD-PWM	CO-PWM	VF-PWM
1	9.5	8.5	9.7	8.4
0.95	8.6	8.6	8.7	7.8
0.9	7.7	7.7	7.8	7.5
0.85	7.6	7.5	7.60	7.4
0.8	7.4	7.2	7.55	7.1

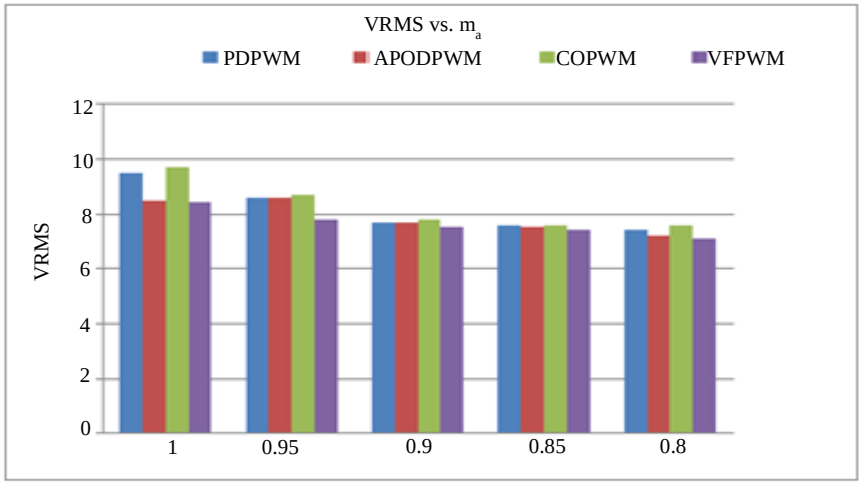

Fig. 12 Root Mean Square output voltage (fundamental component) concerning output current (experimental data)

Table 7. DF of output voltage with experimental results

m_a	PD-PWM	APOD-PWM	CO-PWM	VF-PWM
1	0.090	0.085	0.087	0.082
0.95	0.091	0.092	0.084	0.087
0.9	0.104	0.101	0.094	0.099
0.85	0.100	0.102	0.100	0.101
0.8	0.100	0.105	0.104	0.102

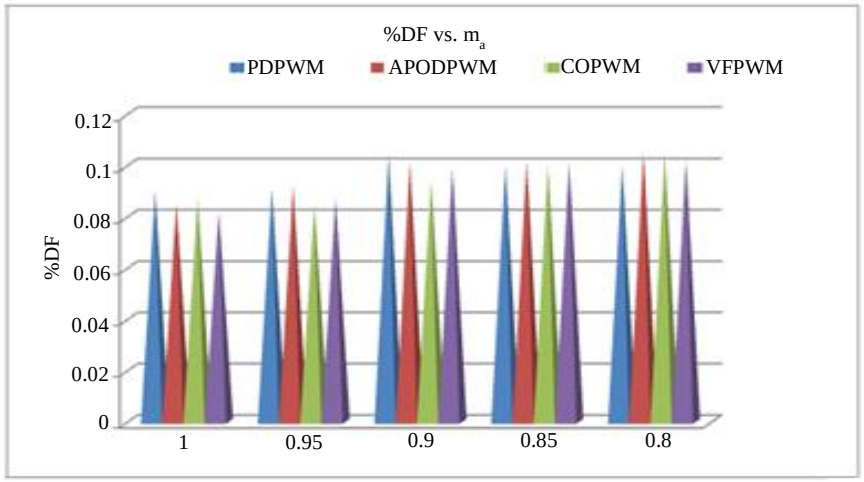

Fig. 13 Percentage of distortion factor in output voltage as a function of output current (experimental data)

Table 5, in conjunction with Figure 11, underscores the notably reduced harmonic content in the output voltage achieved by the VF-PWM strategy. In contrast, Table 6 and Figure 12 demonstrate that the VRMS output voltage of the CO-PWM strategy surpasses that of the other PWM strategies.

Lastly, Table 7, complemented by Figure 13, indicates that the VF-PWM strategy exhibits a lower % DF. These collective results offer valuable insights into the performance and attributes of diverse PWM strategies when applied to the 7LUSI configuration under examination.

5. Conclusion

This study demonstrates the 7-Level Unequal Source Inverter (7LUSI) employing the TAR PWM method. The results highlight that this recommended inverter reduces switching demands and yields significantly higher output

voltage levels while concurrently minimizing harmonic distortions. A comprehensive assessment of several performance metrics, encompassing Total Harmonic Distortion (% THD), Voltage Root Mean Square (VRMS), Crest Factor (CF), Form Factor (FF), and Distortion Factor (DF), was meticulously conducted, reported, and subjected to thorough scrutiny. The Comparative Offset (CO-PWM) strategy emerged as the frontrunner, delivering notably higher fundamental RMS voltage output and remarkably lower % THD values than the Variable Frequency (VF-PWM) strategy. Interestingly, all PWM techniques exhibited nearly identical CF and FF results. However, the VF-PWM technique demonstrated a relatively low DF. Both simulation and prototype results affirmed the feasibility of the 7LUSI configuration and the proposed advanced PWM method.

Furthermore, the study underscores the effectiveness of the TAR PWM approach in enhancing the inverter's performance and improving the harmonic spectra of the resulting output voltage, in stark contrast to the conventional Sinusoidal PWM (SPWM) technique. This research showcases promising advancements in inverter technology, promising greater efficiency and improved voltage quality for various applications.

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