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Original Article

VLSI Architecture of Efficient Hybrid Multiplier Using Hybrid Adder

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Abstract *- With the proliferation of digital signal processing systems and embedded systems in the VLSI era, multipliers have emerged as pivotal components. Their performance greatly influences computational speed, system area, and power consumption, impacting the overall system cost. Multipliers predominantly involve logical operations in computing additions for partial product generation. To enhance the efficiency of these multipliers, it is essential to minimize switching activity and reduce the architectural area using combinational optimization techniques. This research paper presents the development of hybrid multiplier architecture by employing hybrid adders and adopting optimizing strategies. The proposed hybrid multiplier architecture has been synthesized and simulated using Xilinx Vivado 2017.2, with subsequent hardware implementation conducted on the Zedboard. Experimental findings reveal a notable speed improvement when comparing the proposed hybrid multiplier to alternative multiplier designs.*

Keywords *- Hardware implementation, Optimization, High-speed architecture, VLSI multiplier, Hybrid multiplier.*

1. Introduction

In the realm of digital signal processing, two widely utilized filter types for noise reduction are Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters. In the context of FIR filters [1], a significant portion of the resources is dedicated to generating partial products and optimizing their combination through reduction techniques to reduce the overall number of additions performed by adders. This quest for efficiency has given rise to various multiplication architectures, with the array multiplier, wallace tree multiplier, and Vedic multiplier being prominent examples. Among these, the array multiplier, while widely used, tends to be cost-efficient due to the substantial number of gates it employs [2].

On the other hand, the wallace tree multiplier offers efficiency through a regular tree structure but faces hardware complexity challenges as the number of operands increases. The "Urdhva Tiryagbhyam" sutra-based Vedic multiplier design stands out as one of the fastest multipliers, boasting remarkable speed in its operations [3-19]. A. Khan et al. [3] used Vedic formulas to design a self-multiplier and square calculator in the context of Quantum-dot Cellular Automata (QCA) technology, focusing on coplanar designs and performance analysis. Sridevi Sathya Priya S. et al. [4] experimented to design a 4-bit Vedic multiplier using the 'URDHVA TRIYAGBHYAM' sutra. They found that it excels in speed and efficiency compared to traditional array multipliers.

Avinash Kumar Singh et al. [5] designed a butterfly structure using a combination of a Vedic multiplier and a Carry Look-Ahead (CLA) adder and observed that Vedic multiplication offers significant performance improvements compared to the Booth multiplier technique. Khubnani, R., Sharma, T., & Subramanyam, C. [6] discussed the utility and potential applications of Vedic Mathematics, highlighting the concurrent calculation of partial products as a critical efficiency contributor.

Tangam .C et al. [7] implemented a Vedic multiplier with a barrel shifter, which reduced delay compared to conventional multipliers, potentially improving speed and efficiency in applications requiring fast arithmetic operations. A. Sai Kumar et al. [8] integrated a Brent Kung adder with the Vedic multiplier to minimize latency using the 'Urdhva

Tiryagbhyam' sutra. Aditi Awasthy et al. [9] utilized Vedic mathematics algorithms and detector and compressor circuits to address delay and complexity challenges in digital circuits, aiming to optimize mathematical operations.

Anbumani V et al. [10] replaced traditional adders with multiplexer-based alternatives to minimize gate delay and reduce power consumption, achieving more efficient circuit operation. Arti Kumari et al. [11] designed and implemented a 12-bit Vedic Multiplier using an optimized decoder-based adder, enhancing resource utilization. Combining the Vedic Multiplier with Kogge-Stone Adders for multiplication operations can improve the efficiency and speed of digital systems, especially in signal processing and image processing [12]. However, it may come at the cost of increased area usage.

Ramin Barati et al. [13] experimented with a vedic multiplier combined with a proposed reversible kogge-stone adder, achieving the lowest delay and least power consumption. Abhijeet Patil et al. [14] present a comprehensive assessment of multiple multipliers integrated with a carry-look-ahead adder, likely focusing on various performance parameters to improve the efficiency of multiplication operations.

A. Haripriya et al. [15] designed a Vedic multiplier incorporating a Carry Select Look-Ahead (CSLA) adder to enhance multiplication speed and efficiency. The use of the Urdhva-Tiryakbhyam algorithm for breaking input operands into sub-blocks and computing intermediate products is a notable approach.

However, the CSLA adder may not be the most area-efficient choice due to its dual Ripple Carry Adder (RCA) design. These studies continue to explore Vedic multiplication techniques in different application areas, emphasizing the need for improved speed, efficiency, and performance through algorithm optimization and specialized adders [16-18].

The research spans diverse fields, from quantum-dot cellular automata to digital signal processing, demonstrating the versatility and potential of Vedic mathematics in modern computational systems. Researchers are actively working on adapting Vedic multiplication for various bit lengths and proposing innovative solutions to address complexity and delay challenges. These studies contribute to understanding the trade-offs involved in hardware and design complexity when implementing Vedic multiplication techniques. However, this efficiency comes at the cost of an increased adder requirement when dealing with substantial numbers.

In this context, a comprehensive survey of various adders is being conducted [19-24]. In contrast to counterparts like CLA and other parallel-prefix adders, the Ling adder boosts speed and minimizes power consumption [19]. Its ability lies in reducing logic levels needed for carry computation, setting it apart in rate and reduced carry propagation delay. The Weinberger adder is renowned for its minimal area, attributed to utilizing the Weinberger Recurrence algorithm for carry computation. To enhance circuit speed, the Weinberger adder incorporates the concept of parallel carry computation [20]. The Han-Carlson Adder adopts a tree-based structure with a balanced design, offering commendable performance, although with the requirement of potentially being less area-efficient than some competing adders [21].

In contrast, the Brent-Kung Adder excels in striking a harmonious balance between speed and area efficiency, making it a prominent choice in high-performance processors [22]. Meanwhile, the Kogge-Stone Adder leverages a binary tree structure that is both simple and regular. This design choice and its inherent balance between speed and area efficiency solidify its standing as a preferred solution in digital circuit design [23].

In summary, these parallel-prefix adders exhibit distinctive architectural features. The selection of the most suitable adder depends on various factors, including the specific application's requirements, the desired trade-offs between speed and area efficiency, and the available implementation resources. Each adder has advantages and disadvantages, rendering them fit for diverse scenarios in digital circuit design [24].

Nonetheless, this enhanced efficiency comes with the trade-off of an increased demand for adders, particularly when handling large numbers. The multiplier relies on adders to execute the crucial task of summing partial products. By incorporating advanced adders, mitigating the delay time associated with the multiplier becomes possible.

The identified research gap pertains to the role of adders in multipliers, focusing on how advanced adder designs can be selected and optimized to mitigate delays in multiplication operations. Further research is needed to evaluate adder performance, scalability, application-specific optimization, and trade-offs in various digital signal processing contexts.

This paper aims to introduce a hybrid multiplier adopting Vedic mathematics that leverages optimization techniques to enhance key performance metrics. The subsequent sections of this paper are organized as follows: Section 2 presents the proposed hybrid multiplier, and Section 3 and Section 4 delve into the discussions of the obtained results.

2. Proposed Hybrid Multiplier

The proposed hybrid multiplier architecture comprises three distinct stages visually depicted in Figure 1. These stages integrate the previously discussed hybrid adders. Now, let's delve into a detailed breakdown of each stage and the specific requirements for the adders involved.

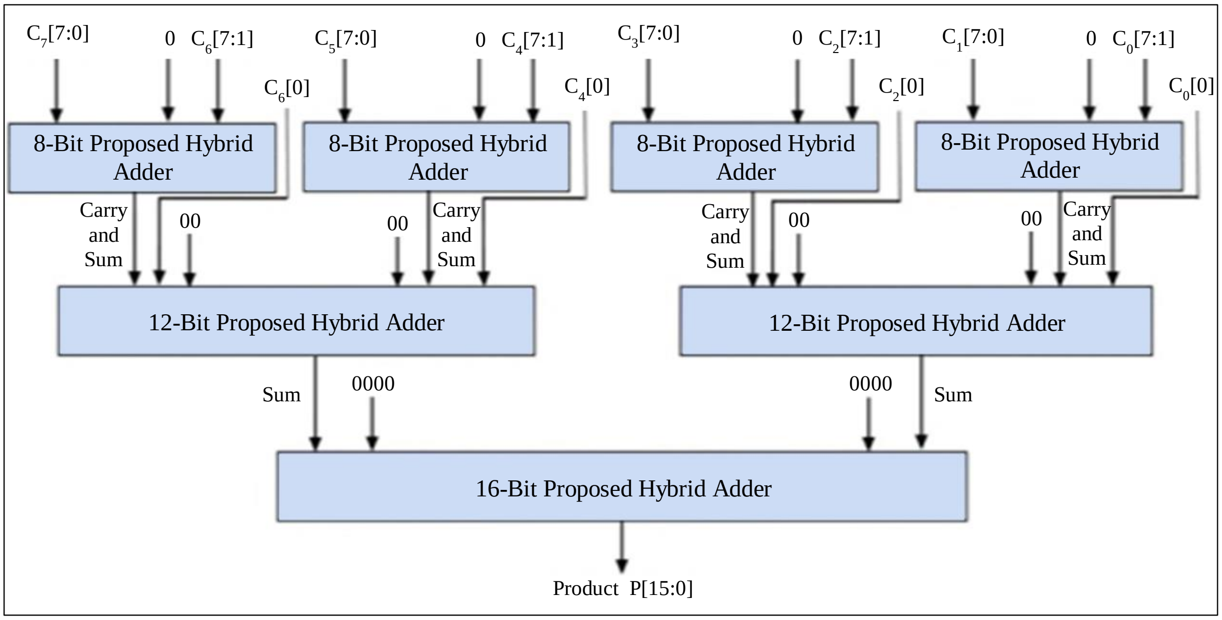

C7[7:0]
0
C6[7:1]
C6[0]
C5[7:0]
0
C4[7:1]
C4[0]
C3[7:0]
0
C2[7:1]
C2[0]
C1[7:0]
0
C0[7:1]
C0[0]
8-Bit Proposed Hybrid Adder
8-Bit Proposed Hybrid Adder
8-Bit Proposed Hybrid Adder
8-Bit Proposed Hybrid Adder
Carry and Sum
00
00
Carry and Sum
Carry and Sum
00
00
Carry and Sum
12-Bit Proposed Hybrid Adder
12-Bit Proposed Hybrid Adder
Sum
0000
0000
Sum
16-Bit Proposed Hybrid Adder
Product P[15:0]

Fig. 1 Architecture of proposed hybrid multiplier

- First Stage: This stage requires four 8-bit proposed hybrid adders.
- Second Stage: Two 12-bit hybrid adders are employed in the second stage.
- Last Stage: The final stage contains a 16-bit hybrid adder.

The output of the 16-bit hybrid proposed adder in the last stage represents the ultimate product of the inputs A and B. This three-stage architecture and the specified adder configurations are crucial in achieving the desired multiplication operation. The proposed hybrid adder concept aims to harness the strengths of different addition techniques to achieve a balance of high-speed operation and minimal area utilization.

Several notable algorithms are integrated within this hybrid adder to optimize its functionality. Specifically, the Hancarlson-based SQRT Carry Select Adder (SQRT-CSELA) exhibits a reduced delay. At the same time, the Ling-based SQRT CSELA [8-11] offers lower power consumption, both of which are superior to most other adder configurations, except for the Ripple Carry Adder (RCA). Additionally, the Weinberger-based Linear CSELA demonstrates efficient utilization of Look-Up Tables (LUTs).

The 6-bit hybrid adder is structured into two distinct groups, illustrated in Figure 2. In the first group, a 4-bit Hancarlson adder is employed for addition, which involves adding addend and augend of bits 0 through 3. The second group, comprised of addend and augend of bits 4 and 5, incorporates a 2-bit Ling adder. Additionally, this second group utilizes a BEC (Binary to Excess-1 Converter) and a MUX (Multiplexer) unit to select the output from the Ling adder or the BEC.

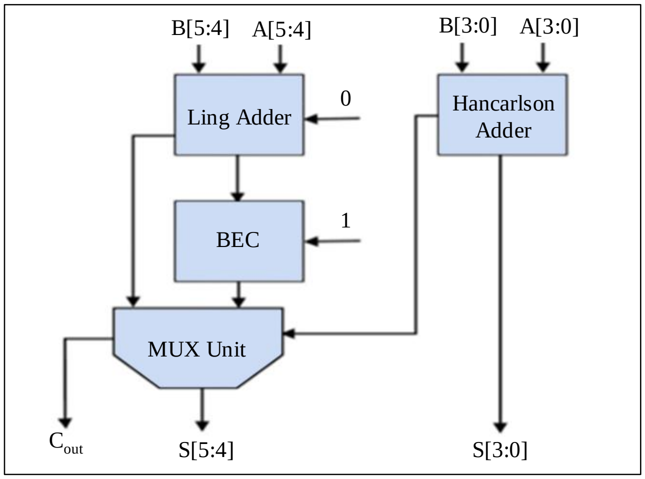


Fig. 2 Architecture of 6-bit proposed hybrid adder

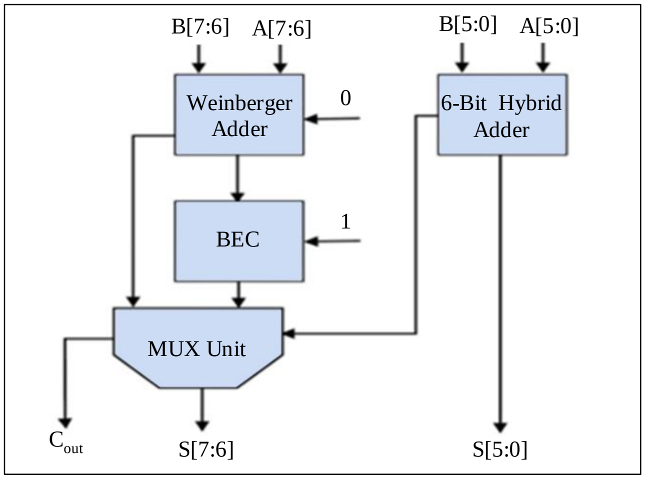


Fig. 3 Architecture of 8-bit proposed hybrid adder

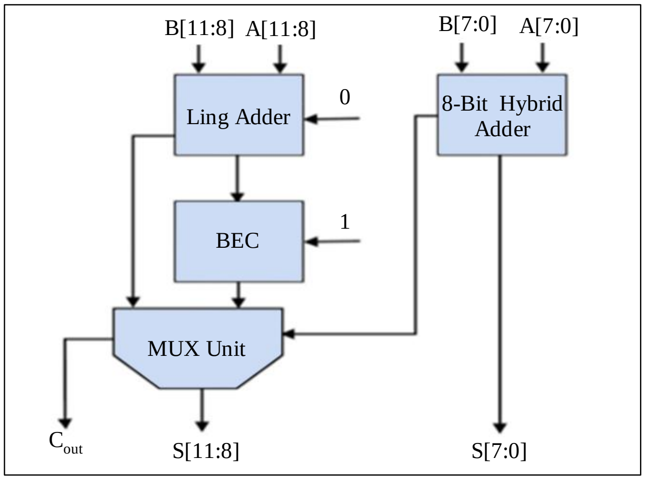


Fig. 4 Architecture of proposed 12-bit hybrid adder

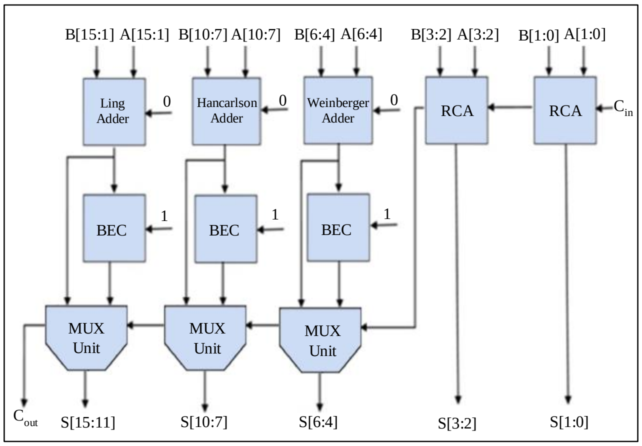


Fig. 5 The architecture of proposed 16-bit hybrid adder

The architecture of the 8-bit hybrid adder, as depicted in Figure 3, is composed of two groups. The first group, consisting of a 6-bit hybrid adder, processes addition for addend and augend bits of 0-5. The second group performs addition for addend and augend bits from 6-7. It employs a 2-bit Weinberger adder with input carry ‘zero,’ a Binary to Excess-one Converter (BEC) adder, and a Multiplexer (MUX) unit to select the output.

The 12-bit hybrid adder is similarly divided into two groups: an 8-bit hybrid adder for bits 0-7 and a 4-bit Ling adder for ‘carry zero,’ BEC ‘ and a MUX unit for output selection for bits 8-11, as shown in Figure 4.

The 16-bit proposed hybrid adder, illustrated in Figure 5, is based on the SQRT CSELA architecture and features five groups. The first two groups, handling augend and addend bits 0-1 along with Cin and bits 2-3, utilize 2-bit Ripple Carry Adders. The third group employs a 3-bit Weinberger adder and BEC and MUX units to add inputs from augend and addend bits 4-6. The fourth and fifth groups function similarly to the third group, except that they employ a 4-bit Hancarlson adder used to perform addition for augend and addend bits of 7-10 and a 5-bit Ling adder is used to perform addition for augend and addend bits of 11-15.

This comprehensive design results in a high-performance 16-bit hybrid adder architecture. The formation of the adder involves integrating various adders creating a Hybrid adder. The proposed hybrid adder’s conceptualisation combines the above mentioned techniques to construct a hybrid adder structure, aiming to achieve elevated speed while minimizing the required area.

Among these, Hancarlson based SQRT CSELA adder has less delay, and Ling based SQRT CSELA provides low power consumption compared to other adder configurations except RCA. And, Weinberger-based Linear CSELA has less utilization of LUTs. The adder mentioned above algorithms [4-12] are integrated into different modules of the hybrid adder to improve the performance. Utilizing the previously mentioned hybrid adders, the partial products are combined or summed.

3. Theoretical Evaluations

The carry propagation chain is the primary factor influencing the critical path delay of the multiplier. Theoretical assessments were conducted on various multipliers, encompassing the Array Multiplier (AM), Wallace Tree Multiplier (WTM), Multiplier Using Compressor (MUC), Vedic multiplier using RCA (VRCA), Vedic multiplier using CLA (VCLA), Vedic multiplier using HCA with BEC (VHCA BEC), and the Proposed Hybrid Multiplier (PHM). The evaluation involved parameters “T” for the delay and “A” for the area.

Specifically, the assessment included T_{XOR}, T_{AND}, T_{OR}, T_{MUX}, T_{NOT}, and T_{XOR} for the delay, representing the propagation delay for 2-input XOR, AND, OR gates, and 2:1 multiplexers.

Table 1. Theoretical analysis of area for various multipliers and the proposed hybrid multiplier

Multiplier	Theoretical Area
AM	$104A_{XOR} + 216A_{AND} + 96A_{OR}$
WTM	$235A_{MUX} + 17A_{XOR} + 81A_{AND} + 94A_{NOT}$
MUC	$104A_{XOR} + 152A_{AND} + 96A_{OR}$
VRCA [5]	$209A_{XOR} + 290A_{AND} + 162A_{OR}$
VCLA [15]	$209A_{XOR} + 438A_{AND} + 152A_{OR}$
VHCABEC	$52A_{MUX} + 213A_{XOR} + 376A_{AND} + 98A_{OR} + 16A_{NOT}$
PHM	$88A_{MUX} + 156A_{XOR} + 276A_{AND} + 109A_{OR} + 7A_{NAND} + 7A_{NOR} + 30A_{NOT}$

Table 2. Theoretical analysis of delay for various multipliers and the proposed hybrid multiplier

Multiplier	Theoretical Area
WTM	$24T_{MUX} + 2T_{XOR} + 2T_{AND} + T_{NOT}$
MUC	$20T_{XOR} + 12T_{AND} + 16T_{OR}$
VRCA [4]	$9T_{XOR} + 13T_{AND} + 24T_{OR}$
VCLA [14]	$9T_{XOR} + 15T_{AND} + 10T_{OR}$
VHCABEC	$4T_{MUX} + 11T_{XOR} + 6T_{AND} + 3T_{OR}$
PHM	$6T_{MUX} + 6T_{XOR} + 7T_{AND} + 5T_{OR}$

Additionally, A_{AND}, A_{OR}, A_{MUX}, A_{NOT}, and A_{XOR} were considered for the area, representing the area occupied by 2-input AND, OR gates, 2:1 Multiplexers, NOT gates, and 2-input XOR gates, respectively The computation of area and delay has been done using a theoretical approach and tabulated in Table 1 and Table 2. From Table 1 and Table 2, it has been concluded that these multipliers' complexity and theoretical delay vary. Multipliers with more gates in their critical path tend to have higher theoretical delays.

4. Results and Discussions

The conventional architectures and the proposed design are modelled using Verilog HDL. For simulation and synthesis, the Vivado 2017.2 ISIM is employed. The tool ran on an INTEL Core i5 processor with a 64-bit operating system and 16GB of RAM and operated at a clock frequency of 2.50GHz. The LUTs, power consumption, and delay after synthesis are tabulated in Table 3. Figure 6 presents the comparative analysis of PDP (Wns). It is evident from the figure that AM stands out with the highest PDP value, which indicates that it is likely associated with the highest power consumption and delay product. Conversely, PHM is shown to have the lowest PDP value in the analysis, suggesting that it is possibly the most power-efficient and features the shortest delay among the entities considered.

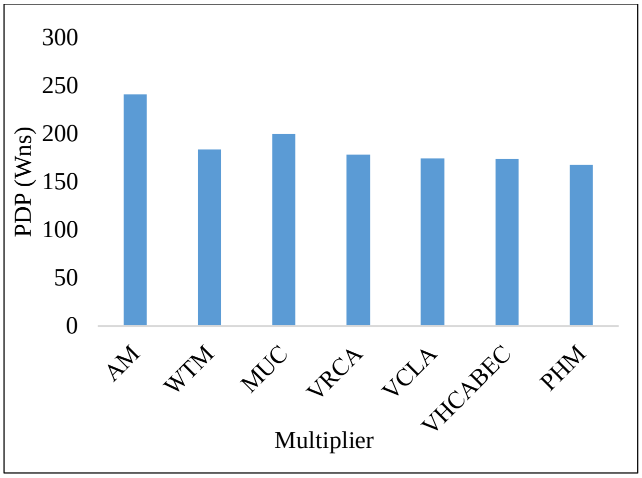


Fig. 6 Comparison of PDP (Wns)

The process of implementing and verifying the proposed hybrid multiplier on a ZedBoard zync evaluation and development kit with part number xc7z020clg484-1 is described as follows:

Hardware Setup: The ZedBoard zync evaluation and development kit with part number xc7z020clg484-1 is utilized.

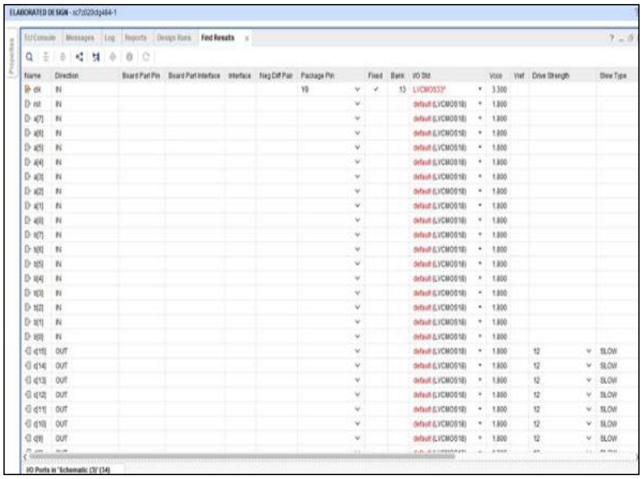
Usage of VIO and ILA Packages: The Virtual Input Output (VIO), and Integrated Logic Analyzer (ILA) packages are selected from the IP Catalog to facilitate the design verification.

Port Mapping: A verilog file is created and modified for port mapping. In this step, the internal signals of the design are connected to the appropriate pins on the FPGA.

Clock Pin Selection: The clock pin is designated as a Y9 package pin, likely as the clock input for the multiplier design, as shown in Figure 7.

Table 3. Practical comparative of delay, power, LUTs and PDP for various multipliers and the proposed hybrid multiplier

Multiplier	LUTS	Practical Delay		Power (W)	PDP (Wns)
		Setup Delay (ns)	Hold Delay (ns)		
AM	80	17.227	2.423	13.982	240.87
WTM	81	13.370	2.698	13.735	183.637
MUC	82	14.553	2.547	13.729	199.80
VRCA [4]	87	13.233	2.586	13.459	177.97
VCLA [14]	103	12.536	2.675	13.909	174.36
VHCABEC	96	12.755	2.783	13.632	173.88
PHM	134	11.759	2.776	14.238	167.42



ELABORATED DESIGN - xc7z020clg484-1

Name	Direction	Board Part Pin	Board Part Interface	Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type
clk	IN					Y9	✓	13	LVCMOS33*	3.300			
rst	IN								default (LVCMOS18)	1.800			
a[7]	IN								default (LVCMOS18)	1.800			
a[6]	IN								default (LVCMOS18)	1.800			
a[5]	IN								default (LVCMOS18)	1.800			
a[4]	IN								default (LVCMOS18)	1.800			
a[3]	IN								default (LVCMOS18)	1.800			
a[2]	IN								default (LVCMOS18)	1.800			
a[1]	IN								default (LVCMOS18)	1.800			
a[0]	IN								default (LVCMOS18)	1.800			
b[7]	IN								default (LVCMOS18)	1.800			
b[6]	IN								default (LVCMOS18)	1.800			
b[5]	IN								default (LVCMOS18)	1.800			
b[4]	IN								default (LVCMOS18)	1.800			
b[3]	IN								default (LVCMOS18)	1.800			
b[2]	IN								default (LVCMOS18)	1.800			
b[1]	IN								default (LVCMOS18)	1.800			
b[0]	IN								default (LVCMOS18)	1.800			
d[15]	OUT								default (LVCMOS18)	1.800		12	SLOW
d[14]	OUT								default (LVCMOS18)	1.800		12	SLOW
d[13]	OUT								default (LVCMOS18)	1.800		12	SLOW
d[12]	OUT								default (LVCMOS18)	1.800		12	SLOW
d[11]	OUT								default (LVCMOS18)	1.800		12	SLOW
d[10]	OUT								default (LVCMOS18)	1.800		12	SLOW
d[9]	OUT								default (LVCMOS18)	1.800		12	SLOW

I/O Ports in "Schematic (3)" (34)

Fig. 7 Clock pin selection

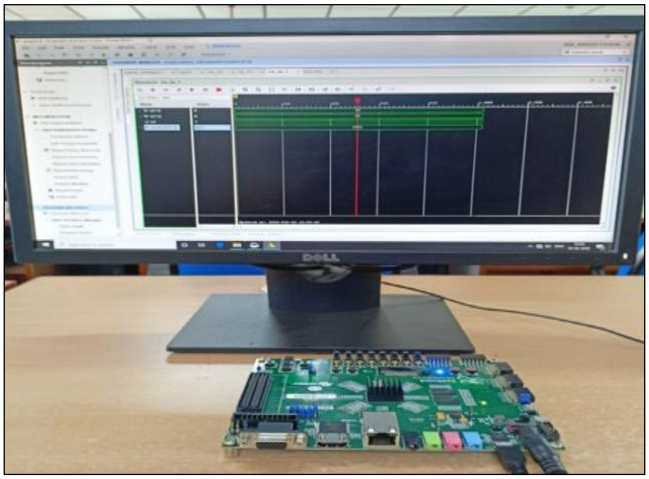


Fig. 8 Implementation of PHM on Zedboard

I/O Standards: The I/O standards are specified as LVCMOS33, defining the voltage levels and signaling standards for inputs and outputs. LVCMOS33 typically corresponds to Low-Voltage CMOS with a 3.3V supply voltage.

Bitstream Generation: The bitstream is successfully generated after configuring and mapping the design. This bitstream file contains the configuration data required for the FPGA to implement the design.

Hardware Connection: The ZedBoard is powered on and connected through the hardware management interface, allowing the loading of the generated bitstream onto the FPGA.

Implementation on ZedBoard: The proposed hybrid multiplier architecture is implemented on the ZedBoard zync evaluation and development kit, with Figure 8 illustrating the implementation.

Verification: Probes are set up in the Integrated Logic Analyzer (ILA) package to monitor signals within the design, enabling the analysis of the multiplier's behaviour.

Testing: With the hardware and software setup in place, tests are conducted for different combinations, and the functionality of the proposed hybrid multiplier is analyzed.

5. Conclusion

In our research, an energy-efficient hybrid multiplier has been developed that exhibits notable improvements in speed and the Power Delay Product. This enhancement is achieved by incorporating a hybrid adder as a fundamental component within the design of the energy-efficient hybrid multiplier.

The effectiveness of this architecture has been evaluated through synthesis and simulation, aiming to meet predefined criteria for efficiency and functionality. Facilitating these processes involved relying on the instrumental Xilinx Vivado 2017.2 ISIM tools. These tools are instrumental in enabling us to thoroughly analyze and assess the performance and behavior of our design, ensuring that it meets the desired criteria for efficiency and functionality.

The viability and potential of the energy-efficient hybrid multiplier and its associated components have been validated using Xilinx Vivado 2017.2 ISIM tools. Significantly, the design has been translated into hardware on the Zedboard platform, providing substantial evidence of its practical viability.

The results demonstrate noteworthy improvements in multipliers' speed and Power Delay Product, enhancing their energy efficiency. These findings are significant as they can potentially improve the performance and efficiency of various applications that rely on multiplication operations.

Moreover, the highlighted adaptability of this approach enables the seamless integration of new filter architectures. This flexibility creates opportunities for optimized solutions across various domains, including digital signal processing, multimedia, and cryptography. As a result, the research carries promising implications for a broad spectrum of applications and industries.

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