SSRG International Journal of Electrical and Electronics Engineering
ISSN: 2348-8379/ https://doi.org/10.14445/23488379/IJEEE-V10I12P105

Volume 10 Issue 12, 37-53, December 2023

Original Article

Distinct ρ-Based DGMOSFET Analysis for Ternary Content Addressable Memory at Sub-nm VLSI Technology

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Received: 05 October 2023 Revised: 08 November 2023 Accepted: 06 December 2023 Published: 23 December 2023

Abstract *- A leading-edge sub-nm digital logic technology related to Ternary Content Addressable Memory (TCAM) based binary-memory cell by scaling the CMOS technology has increased the implications of leakage-current and power-analysis for memory design. Conventional TCAM designs have a dynamic CMOS circuit architecture to improve matching speed; however, these implementations have to overcome design limitations, such as process variations of Short-Channel Effects (SCEs). To minimize the SCEs, in this work, a distinct ρ-based DGMOSFET TCAM circuit, binary-memory cell for low-power, available speed-and-area TCAM, using a particular ρ-based binary-memory switch for non-volatile memory data storage is designed. Simulation-based on a distinct ρ-based binary-memory mathematical model analyzed by sub-nm-MOS model parameters. The proposed design analysis and simulation results show better value improvement in delay and energy/bit/search for 64x64-bit TCAM comparatively.*

Keywords *- TCAM, SCE, DGMOSFET, Sub-nm, Low power.*

1. Introduction

TCAM process through parallel search operation in comparing the search content-data in memory with all stored during one cycle of TCAM operation. TCAM is popularly used for similar data search operations, providing a better way to search content data in the memory and results in a contentdata-addressed one-clock state of TCAM operation.

Conventional TCAM architecture uses a dynamicparallel design to improve the content-data matching speed with a high density of content data; however, for such designs, there is a requirement for system clocks with high-speed analysis, which suffers from design limitations in timing violations and charge sharing.

Based on TCAM having a better pre-charge circuit and improved stability for practical operations: a distinct ρ-based DGMOSFET Low Power circuit TCAM cell for read and write operations is proposed. The particular ρ-based DGMOSFET TCAM cell can reduce the delay problem by introducing distinct ρ-elements at the sense amplifier used to detect small changes in the pre-charge circuit, as Bit Line (BL) or Match Line (ML) voltages reduce during the pre-charge state of operation. Here, during the state of the operation cycle, the Search Line (SL) and compliment value of the Search Line (SL) are pre-charged with the Ground (GND) value, and ML is pre-charged with the supply Voltage (V_{DD}) value.

The distinct ρ-elements used are for memory, and the search operation has to increase the number of cells based on TCAM design with density parameters of the cells.

The main challenge is with the system clocks, which are limited; further timing violations are to be determined. To do this, a more adaptable way is to design a distinct ρ-based DGMOSFET TCAM cell with a 4T4M static-based architecture using a binary-memory switch for non-volatile data storage for an improved content-data-search-operation on search speed improvement and search energy limitations, this is made possible through proposed work approach.

In this research paper, authors propose a novel staticbased architecture for TCAM cells designed with distinct ρelements based TCAM memory cells using distinct ρ-based DGMOSFET because of its compatibility and less search delay with less search energy.

a) Contributions of this paper at Sub-nm VLSI Technology
   1. Increased the implications of leakage-current and power analysis for memory design.
b) It can be limited by reasonable electrostatic control over the channel.
   1. The limitation arises from using system clocks, which suffer from timing violations.
   2. It can be limited by a static-based architecture using a binary-memory switch for non-volatile data storage.

Section 2 overviews previous works on designs related to DGMOSFET and TCAM. Section 3 presents the method for designing the proposed distinct ρ-elements in the TCAM cell, implemented through distinct ρ-based DGMOSFET. Section 4 discusses the results of the designed method from TCAD simulations. Finally, the conclusion of the proposed model is given in Section 5, with a discussion of its future scope.

2. Previous Work

With the scaling of CMOS technology, the challenges in device design have increased in gate control, process variations, and SCEs. DGMOSFET, known to be a better technology device, could control these challenges. Based on DGMOSFET having better electrostatic control over the channel and robust electrical characteristics in better switching, a distinct ρ-based silicon N-channel double gate MOSFET model is proposed. The distinct ρ-based DGMOSFET limits the short channel effects of the device through a better channel control and double gate control mechanism from the source; the channel's formation can increase the current flow when the device is switched on. Here, the gate controls the switching operation, with the device body required to provide enough control over the channel.

The distinct ρ-based DGMOSFET uses the back entrance to adjust the front gate's threshold voltage (Vt), which can improve the design of circuits in reducing delay and power. The main challenge is leakage current, which is limited; further, the sub-threshold gate leakage is to be determined. To do this, a more adaptable way is to design a distinct ρ-based DGMOSFET device with reasonable electrostatic control over the channel by controlling the gate-to-source voltages with the threshold voltage; this is made possible through the proposed work approach.

At the earliest design, the binary and ternary-based TCAM cells included CMOS-based [1], with emerging memory-based TCAM cells [2]. Few TCAM designs have soft-error tolerance memory redundancy, and match sense amplifiers are replaced with an analog comparator [3]. The approximate search CAMs method uses a hashing method by storing data and query patterns [4], which requires hashing of content data to keep and search, which results in low search capability [5]. Methods based on memristor for memory crossbar-based designs are proposed in [6]. In [7], nearmemory logic is presented to measure the similarity between content-data vectors for data word differences in calculating the sum of squares.

The short circuit current path reduces short circuit power consumption during mismatch conditions, addressed in conventional CAM through a pre-charge-free method. The output control self-controlled pre-charge CAM is designed to limit the power consumption by varying charges. In CAM memory, array elements are analyzed through volatile and non-volatile modes. The maximum power consumption is in the pre-charge phase compared to the evaluation phase to reduce the power consumption by limiting the SC current path.

Recently, TCAM cells have been using a single Nanoelectromechanical (NEM) memory switch [8] for lowpower applications, and this device is operated through [9] validations. The Search Line (SL) transistor is removed in [10] for further power reduction. The CMOS-based CAMs were implemented in [11] for area and density reduction through electromechanical principle. For delay, a pre-charge circuit is used in [12], where BL or ML voltage is reduced, causing the sense amplifier to minimize the changes in detection. Using the pre-charge-free CAM circuit reduces the power consumption during the mismatch condition [13], and even bit does not match during the logic operation.

Pre-stored content search in a parallel process is realized through in-memory computation. For similar procedures, the input search query is considered by CAM, and it compares with the stored data patterns and returns to contentaddressable data. In traditional approaches, the memory elements hold the pre-stored encoded data, which has a comparator to integrate the data with encoded data, increasing power consumption in the search process.

In [14], resistive component-based memory elements were designed and implemented for the specified search content representations for computational operations to perform, which are stored in the memory. In [15, 16], the resistive-based memory cells are used for threshold voltagebased memristor for additivity; here, the fitting parameters have achieved distinction between matching and mismatching cases.

In TCAM, the primary focus on power consumption is in the design of Match Lines (ML), Search Lines (SLs), and clock and control circuits. To limit this problem [17, 18], with reduced dynamic power consumption and by controlling static power consumption, which is a non-limiting factor as technology progress. Also, scaling of bulk CMOS devices might increase circuit performance but increase the short channel effect.

Several TCAM designs were proposed to provide minimum energy-delay products. For multi-level search and data-content comparison, a level of content to deliver with a better data-content match is essential, made possible by sensing the discharging lines: to pre-charge ML first, next ML feels the decreasing slope of ML voltage through output sense amplifier available. For the remaining, ML starts discharging rapidly. These clock timing comparisons are essential for device characteristics, making a scalability-low cell. The clock timing speed limitation is solved through a capacitiveelement-based search method for TCAM cells [19].

In capacitive-based-TCAM cells, the charge coupling and charge distribution-based multi-level content searching schemes are proposed [20, 21], having two capacitor model methods: one is having a capacitor to short its top plate with an initial voltage, i.e., GND, and the other is having capacitor top plate floating by keeping the bottom container at voltage input, making the average voltage is available at capacitance setting time. In the design of DGMOSFET for scaling limitations [22-24], the short channel effect uses multi-gate transistors, making it more difficult for sub-nm technology nodes. Here, at 90 nm technology device scaling, the proximity between source and drain reduces the control of the gate over the channel between drain and source, leading to a high value of Short Channel Effects (SCEs) [25]. In 90 nm technology, distinct ρ-based DGMOSFET-based designs provide better control over SCEs for low power and delay arrangements and overcome the scaling challenges by reducing the gate oxide thickness.

3. Proposed Works

Scaling the device gate length with gate oxide is the most effective strategy to improve performance while lowering costs. Scaling the gate length lowers cost-per-chip, whereas scaling the gate oxide improves drive current and lessens the short-channel effects caused by gate-length scaling. However, as the gate oxide reduces, the device power required to run DGMOSFET rises due to increased gate oxide leakage current. To address the problem of high-gate-oxide leakage, the mechanism of carrier tuning by gate-dielectric is analyzed. When the oxide voltage (V_{ox}) in a Metal-Insulator Semiconductor (MIS) stack has a lower metal-insulator with its barrier height, electrons tunnel through the metal-electrode into another semiconductor-electrode via the insulator, called tunnelling.

Considering the physical thickness of the gate-oxide SiO_2: T_{ox} with insulator's dielectric-constant: k are the most critical factors influencing the direct tunnel current density. Generally, every 0.5 nm of SiO_2 thickness increases gate leakage by 100 times. The gate-leakage density for SiO2 having 1.1 nm can reach 10 x 10^4 Amp/cm^2. The increased standby power usage is due to the significant gate leakage.

Increasing an insulator's dielectric constant significantly reduces direct-tunnelling current. Having the Equivalent Oxide-Thickness (EOT) correlates with gate-oxide-physical thickness with insulator-dielectric-constant, and with these, an insulator material with a dielectric constant more time larger than SiO_2 needs a physical thickness of more times bigger-SiO_2 to maintain the same EOT-as-SiO_2. Because the tunneling-leakage-current decays exponentially as the insulator thickness increases, the device-tunneling-current employing this device-insulator has orders of magnitude lower than a device-SiO_2. Issues have been raised about using polysilicon-gate-electrodes having high-dielectric-constant, represented as high-k insulators.

Two preferable metal gate options are suitable with a "front gate first" or a "back gate last" approach and have a low sheet resistance. For better-performance and less-power semiconductor devices, the SiO_2 stack with polysilicon is replaced by the high-k insulators stack. Implementing high-k insulator stacks has two key benefits: they help lower gateleakage-current and scale the EOT of modern DGMOSFET. Table 1 displays the different dielectric materials along with their characteristics.

Table 1. Properties of dielectric high-K materials

Gate Dielectric Material	Dielectric Constant (k)	Energy Band Gap E_g (eV)	Conduction Band Offset ΔE_c (eV)	Valence Band Offset ΔE_c (eV)
SiO_2	3.9	9	3.5	4.4
Al_2O_3	8	8.8	3	4.7
TiO_2	80	3.5	1.1	1.3
ZrO_2	25	5.8	1.4	3.3
HfO_2	25	5.8	1.4	3.3
Ta_2O_5	25	6	1.5	3.4
Y_2O_3	13	6	2.3	2.6
Ya_2O_3	27	4.3	2.3	0.9

3.1. Distinct ρ-Based Device Structure Design and Simulation

Using the conventional Silicon Integrated chip manufacturing method, we built an n-channel polysilicon gate symmetric DG-MOSFET with a 90nm gate length in this research work. The electrical performance of the device was assessed using the LTSpice circuit simulator. Spacers are utilized on both sides in addition to the gate oxide material, SiO2, to lessen the fringing field effect. Figure 1 schematically depicts the construction of the distinct-based DG MOSFET designed and employed in this work. Table 2 lists the design parameters for this device.

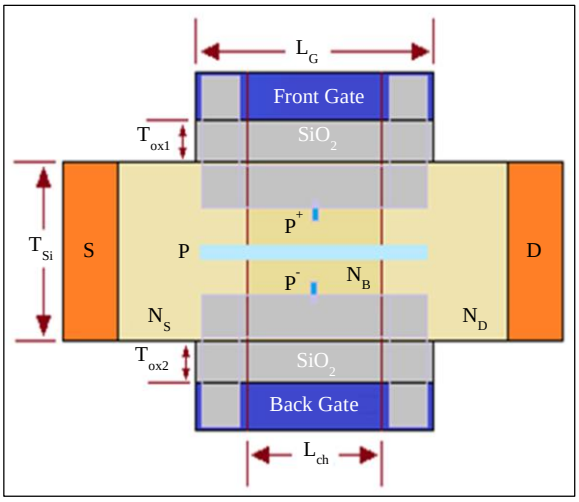


Fig. 1 Proposed DG-MOSFET ρ-distinct slots structure

A homogeneous p-strained-Si layer with a thickness of 1 nm is also layered on top of the bottom SiO_2 interfacial layer. Figure 1 depicts the construction of the DG MOSFET.

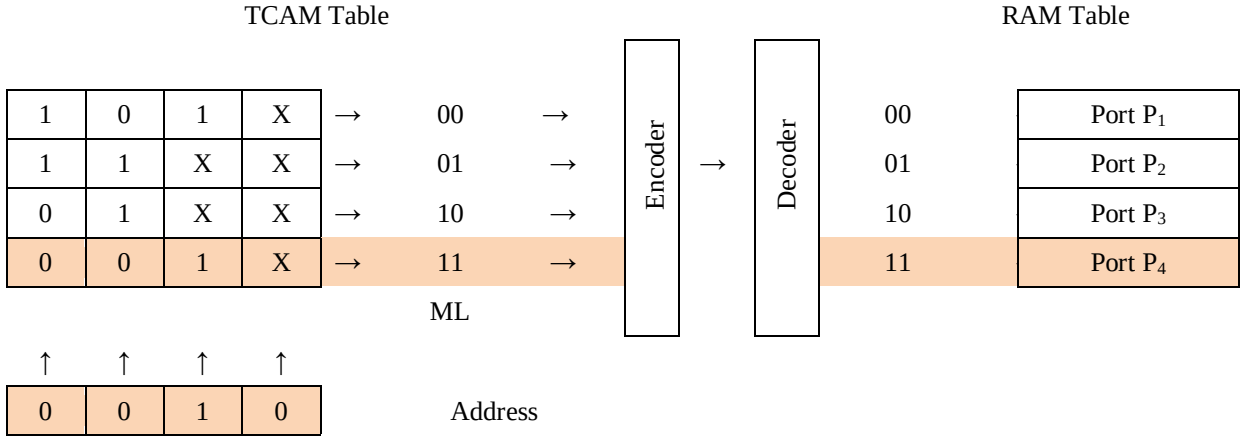
Table 2. Device parameters considered for proposed distinct ρ-based DGMOSFET

Device Parameters	Distinct ρ-Based DGMOSFET
Minimum Channel Length (μm)	0.2
Gate Width (μm)	0.345
Doping ($x10^{18}/cm^3$)	2.0
Threshold Voltage (V)	0.2

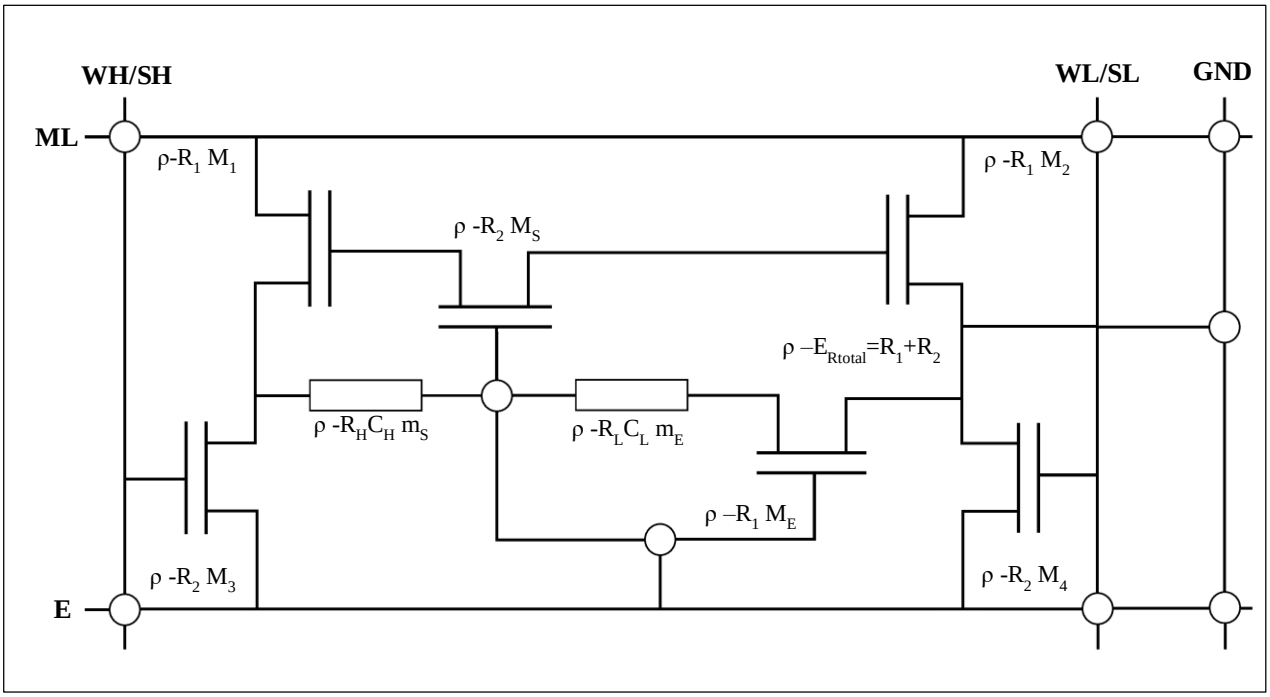
3.2. Distinct ρ-Based DGMOSFET Device TCAM Cell Design

The proposed distinct ρ-based DGMOSFET device TCAM cell consists of two binary-memory distinct ρ-elementmemory components, m_E and m_S, and two transistors, M_E and M_S, as enable and search logics are shown in Figure 2, which illustrates the design analysis at sub-nm (90 nm) VLSI technology.

- Here, we have two binary-memory distinct ρ-elements, m_E and m_S, and two transistors, M_E and M_S, as Enable and Search logics.
- For logic-1 bit to write: m_S is 1. For a logic-0 bit to write: m_E is 1.
- Here, WH and WL lines, and shared search operations SH and SL, through ML and its G, where WH: Write high and WL: Write Low, SH: Search High, SL: Search Low, ML: Match Line and it is Ground (G).
- The distinct ρ-elements are suitable electrostatic materials to control the timing violations.



(a) TCAM memory architecture with RAM ports (P_1- P_4)



(b) TCAM distinct ρ-based binary-memory circuit

Fig. 2 Schematic of binary-memory-transistor ternary content addressable memory cell

The m_E and m_S ρ-element-resistor-charge components pair is connected in parallel position, which makes a memory storage cell of the designed proposed distinct ρ-based DGMOSFET device TCAM. The particular ρ-elementresistor component is used for writing the data in the TCAM cell; for this logic-1 write operation, the m_E logic-1-high bit is set with the equivalent high resistance, i.e., E_{Rtotal} = HIGH making R_H=1 and the m_S logic-0-low bit is charged with the equivalent low resistance, i.e., E_{Rtotal} = LOW making R_L=0.

For this logic-0 write operation, the m_E logic-0-low bit is set with the equivalent low resistance, i.e., E_{Rtotal} = LOW, making R_H=0 and the m_S logic-1-high bit is charged with the equivalent high resistance, i.e., E_{Rtotal} = HIGH making R_L=1.

To reduce delay, the distinct ρ-element-charge component is used to write and read the TCAM cell data transition through the different ρ-element-resistor transitions from LOW to HIGH and HIGH to LOW. In Figure 2, M_E and M_S, as Enable and Search transistors, are connected to distinct ρ-element-memory component pairs.

The M_E separates the TCAM cell from other TCAM cells to reduce the delay path effect. The M_E transistor gate through TCAM cell E: enable pin is connected to control the search and write operation of the TCAM cell. The M_S gate terminal through the M_E transistor is connected, as output, to TCAMcell, and it's tied between two binary-memory distinct ρelement-memory components, m_E and m_S. The M_S drain terminal through the ML-M_S source terminal is grounded.

In write-operation, WH and WL are through the M_S and M_E with m_S and m_E in parallel circuit connection. These two lines, WL and WH, are used to write logic 0 and logic 1 values as ternary data in the TCAM memory cell. In the search operation, the SH and SL lines were connected in the same line of WH and WL as a shared line to search the content data in the TCAM cell. These two lines, SL and SH, are used to search logic 0 and logic 1 content-data values as ternary data in the TCAM memory cell.

The function of the proposed distinct ρ-based DGMOSFET device TCAM cell is shown in Table 3. For search input logic-0, SL is provided with VSEARCH, and SH is supplied with low (GND); by enabling E=HIGH, the output voltage appears across the device, where $E_{Rtotal}=R_1+R_2$, with R_1 and R_2 values, vary based on R_H and R_L values of State 1 and State 0 logic values respectively.

For search input logic-1, SH is provided with VSEARCH, and SL is supplied with low (GND); by enabling E=HIGH, the output voltage appears across the device, where $E_{Rtotal}=R_1+R_2$, with R_1 and R_2 values varying based on R_L and R_H values of State 1 and State 0 logic values respectively. For search input logic-X, low (GND) is provided for SH and SL; by enabling E to HIGH, the output voltage appears across the device with a low (GND) value as SH and SL. This makes the ML remain charged region (ON) and search transistor M_S in the cutoff region (OFF), where $E_{Rtotal}=R_1+R_2$, with R_1 and R_2 values varying based on R_L and R_H values of State 0 and State 1 logic values, respectively.

Table 3. Functions of proposed distinct ρ-based DGMOSFET device TCAM cell

For Input Search (S_{In})		For Data Stored (D_{St})		For Match Line
S_{In} (Logic)	S_{In} (SH, SL)	D_{St} (Logic)	D_{St} (mS, mE)	
0	(0,1)	0	(0,1)	1 (match)
0	(0,1)	1	(1,0)	0 (mismatch)
1	(1,0)	0	(0,1)	0 (mismatch)
1	(1,0)	1	(1,0)	1 (match)
X	(0,0)	Any	Any	1 (match)
X	(1,1)	Any	Any	1 (match)

Table 4. Device simulation parameters

Device Parameter	Values
Channel doping	10^{15} cm^3
Channel length (Lg)	13 nm and 25 nm
Doping- source and drain	1 x 10^{20} cm^3
Channel thickness (t_channel)	4 nm
Top oxide thickness (t_top_ox)	1 nm
Bottom oxide thickness (t_bottom_ox)	1 nm
Distinct ρ-spacing along the channel (dx)	0.2 nm
Distinct ρ-spacing perpendicular to the channel (dy)	0.2 nm
The work function of the metal gate	4.45eV and 4.90eV
Number of ρ-slots in the channel (ρ_slots)	3

4. Results and Discussions

This paper compares the proposed model DGMOSFET's 25 nm and 13 nm channel lengths and gate oxide thickness of 1.5 nm to those of earlier techniques utilizing high dielectric permittivity SiO_2, HfO_2, and ZrO_2 materials. Table 4 provides an overview of the main parameters employed for the device in our simulations.

4.1. Proposed DGMOSFET 2-D Simulation

The conduction band and electrostatic potential curves are displayed in 2D using the suggested model in Figures 3, 4, 5, and 6 for channel lengths of 13 nm and 25 nm, respectively. These graphs demonstrate the changes in drain current for DG MOSFET devices as a function of gate voltage. Table 4, Table 5, and Table 6 provide a summary of circuit device operation parameters obtained from device attributes. These metrics typically comprise leakage current at V_{GS}=0, sub-threshold slope, and DIBL. Table 7, Table 8, and Table 9 show that the sub-threshold slope also decreases due to employing the suggested model, almost decreasing by 14% compared to the prior model. Since channel length affects threshold voltage, threshold voltage rises as channel length (L_G) grows.

4.2. Effects on the Short Channel

Scaling has received more attention in MOSFETs to improve device performance and speed. The gatecontrollability over the channel depletion area, however, declines to a large extent as the channel shrinks [3] as a result of the greater charge sharing from the relevant source and drain depletion areas.

The influence of threshold voltage on channel length is one of the main issues caused by SCEs. Leakage-current and a drop in threshold voltage are SCEs' fundamental issues. SCE likewise impacts the gate controllability over the drain current, affecting the sub-threshold slope and the drain-leakage current. In MOSFETs, there are multiple SCEs. The following SCEs have been analyzed in this paper:

4.2.1. Leakage Current

Is defined as:

$$I_{DS} = 100\left(\frac{w}{L}\right)e^{\frac{q(V_{GS}-V_{th})}{\eta KT}} \quad (1)$$

Where V_{GS} - Gate-to-source-voltage,
V_{th} - Threshold-voltage,
I_{DS} - Drain-to-source-leakage-current,
T - Temperature,
W - Width,
L - Gate length.

4.2.2. Drain-Induced Barrier Lowering (DIBL)

The gate of long-channel-DGMOSFETs controls the channel and provides most of the charge. Additionally, there is a possible barrier between the source and the channel area for the weak inversion regime [7]. This barrier's height suggests balance among float and dispersion current between the two locations. To achieve maximum ON Current, however, the subsequent gate voltage should be used to regulate the barrier height for channel carriers. The DIBL impact appeared when this boundary level changed because of Short-channel impact through the utilization of high-channel voltage.

The equation typically provides DIBL is,

$$DIBL = -\left[\frac{V_{th2}-V_{th1}}{V_{d2}-V_{d1}}\right] \quad (2)$$

Where V_{th2} is saturated-threshold-voltage,
V_{th1} is linear-threshold-voltage,
V_{d2} is drain-voltage-applied in saturation-region,
V_{d1} is drain-voltage-applied in linear-region.

4.2.3. Sub-Threshold Slope

The Sub-threshold Slope [9] is:

$$SS = \left[\frac{d(log_{10}I_{ds})}{dV_{gs}}\right]^{-1} = \frac{KT}{q}\left(1+\frac{c_d}{c_i}\right) \quad (3)$$

Where C_d= depletion-layer-capacitance,
C_i=gate-oxide-capacitance.

Table 5. Device simulation parameters at Vg =0.5V

Simulation Parameters	Value
Gate Voltage	0.5 V
Initial Drain Voltage	0.05V
Final Drain Voltage	0.5V
Number of Voltage Levels	12

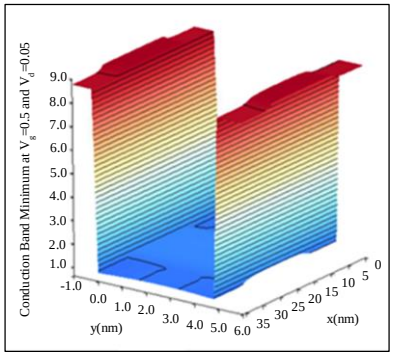


Fig. 3 2D plot of the conduction band at V_g=0.5 and V_d=0.05

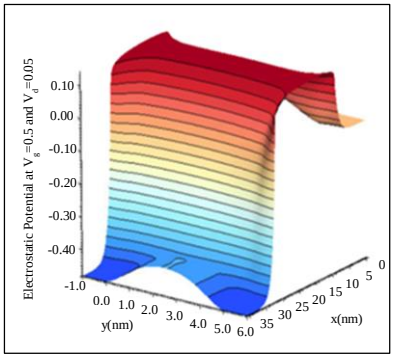


Fig. 4 2D plot of the electrostatic potential at V_g=0.5 and V_d=0.05

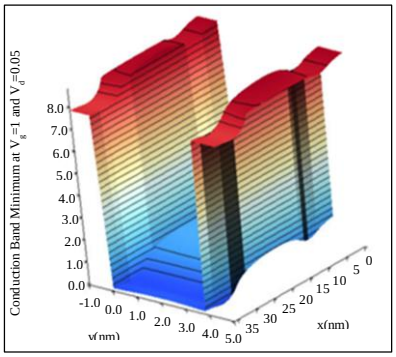


Fig. 5 2D plot of the conduction band at V_g=1 and V_d=0.05

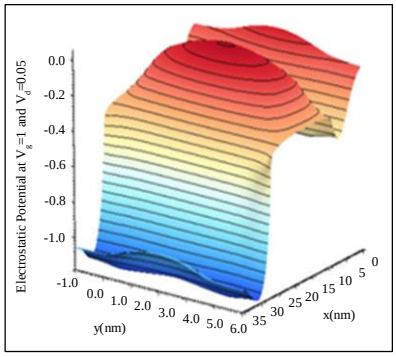


Fig. 6 2D plot of the electrostatic potential at V_g=1 and V_d=0.05

Table 6. Device simulation parameters at Vg =1V

Simulation Parameters	Value
Gate Voltage	1 V
Initial Drain Voltage	0.05V
Final Drain Voltage	0.5V
Number of Voltage Levels	12

Furthermore, when L_G = 25nm compared to the prior model for the gate dielectrics HfO_2 and ZrO_2, we found a leakage-current-significant-reduction: 90% and 82%, respectively. And leakage currents are reduced by around 23% and 35%, respectively, when L_G = 13nm. Figures 3, 4, 5, and 6, together with Tables 7, 8, and 9, make it abundantly evident that the DIBL decreases as the channel length increases. However, when the channel length is reduced, DIBL rises due to an improved work function while the sub-threshold slope falls.

Table 7. Comparative proposed work simulation: SiO_2 dielectric with EOT=1.5nm

	L_G = 25nm		L_G = 13nm	
Parameter	**Conventional Method**	**Proposed Method**	**Conventional Method**	**Proposed Method**
S Slope (mV/decade)	119	110	219	217
Leakage-Current (A/µm)	1.48 e-06	1.41 e-06	3.4 e-05	3.31 e-05
DIBL (eV)	0.0419	0.0345	0.055	0.054

Table 8. Comparative proposed work simulation: HfO_2 dielectric with EOT=1.5nm

	L_G = 25nm		L_G = 13nm	
Parameter	**Conventional Method**	**Proposed Method**	**Conventional Method**	**Proposed Method**
S Slope (mV/decade)	82	81	94	93
Leakage-Current (A/µm)	2.83 e-07	3.01 e-07	5.53 e-06	5.51 e-06
DIBL (eV)	0.018	0.0171	0.0199	0.0160

Table 9. Comparative proposed work simulation: ZrO_2 dielectric with EOT=1.5nm

	L_G = 25nm		L_G = 13nm	
Parameter	**Conventional Method**	**Proposed Method**	**Conventional Method**	**Proposed Method**
S Slope (mV/decade)	63.4	61.3	84.67	83.21
Leakage-Current (A/µm)	9.6 e-08	8.98 e-08	2.99 e-07	2.20 e-07
DIBL (eV)	0.014	0.013	0.055	0.041

4.3. Small-Signal Common-Source-DGMOSFET Analysis RC Coupled Amplifier with a Base: An Application of Proposed Distinct ρ-Based DGMOSFET through High Pass Filter

Due to its high input impedance, low output impedance, high current gain, and voltage gain that is just higher than unity, the common-source DGMOSFET makes an effective amplifier for tiny signals. CS-DGMOSFET has been the subject of several studies to determine its suitability for creating high-speed switching circuits, memory cells, logic gates, buffer amplifiers, power amplifiers, and transconductance amplifiers.

The AC sweep function has been used to illustrate Figures 7 and 8, and a thorough investigation of the constructed amplifier has been conducted. This makes it possible to see the whole response of the CS-DGMOSFET constructed throughout the frequency range of 1 Hz to 10 MHz. Figure 9 and Figure 10 depict the frequency responses for the CSDGMOSFET-based amplifiers for different voltage levels.

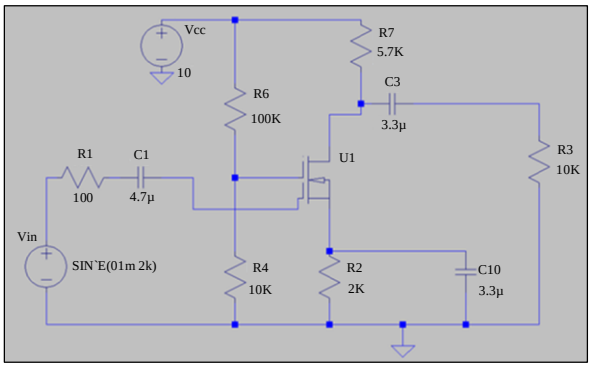


Fig. 7 Proposed distinct ρ-based DGMOSFET common source small signal amplifier with input sine (01m 2k) voltage levels

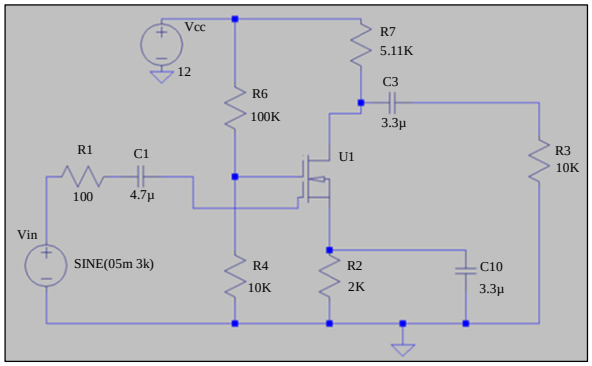


Fig. 8 Proposed DISTINCT ρ-based DGMOSFET common source small signal amplifier with Sine (05m 3k) voltage levels

4.3.1. Frequency Response

The analysis shows that the mid-band and -3 dB gains of the conventional DGMOSFET-based amplifier are equal to those of the proposed distinct ρ-based DGMOSFET common source small signal amplifier. As seen in Figure 9, for back gate design, the value of low-frequency Cutoff Frequency (f_c) is around 0.22 KHz, demonstrating the greater bandwidth of DG MOSFET in the amplifier application. The Lower Cutoff Frequency (f_L) for the proposed DG MOSFET-based amplifier is indicated as 3 dB in Figure 9, and the higher passband frequency is 2.4 KHz in Figure 9.

The f_L is the -3 dB gain at the lower slope of the frequency response. The presence of input high pass RC determines the lower cutoff frequency filter at the input. Thus, the observed passband bandwidth is 2.18 KHz.As seen in Figure 10, for front gate design, the value of low-frequency cutoff frequency (fc) is around 0.22 KHz, demonstrating the greater bandwidth of DG MOSFET in the amplifier application. The Lower Cutoff Frequency (f_L) for the proposed DG MOSFETbased amplifier is indicated as 3 dB in Figure 10, and the higher passband frequency is 2.4 KHz in Figure 10.

The f_L is the -3 dB gain at the lower slope of the frequency response. The presence of input high pass RC determines the lower cutoff frequency filter at the input. Thus, the observed passband bandwidth is 2.18 KHz. The above scenarios for back gate and front gate design: Illustration of observed passband bandwidth of 2.18 KHz at both the gate locations, as shown in Figure 9 and Figure 10; shows that the proposed design is a balanced gate design and can be utilized for amplifier design in electronic circuits.

4.3.2. Phase Response

As seen in Figure 9 and Figure 10, the phase response, when combined with the magnitude response, shows the system's stability. Analysis of amplifier outputs regarding phase response has been considered to drive the DG MOSFET. Between 1 Hz and 2 kHz, the directions of both amplifier circuits are analyzed. The first direction of the amplifier shown in Figure 9 has a phase shift of -145 degrees, while the DG MOSFET amplifiers have phase shifts of -90 degrees. The mid-band gain is less than unity for both amplifier architectures at f=180 with phase shift at -180°.

However, one could notice a more significant phase margin for the DG MOSFET-based amplifier than the SG MOSFET-based amplifier; the phase margin must be greater than the phase shift to produce instability. The phase shift caused by this instability is -180°. The phase margin for the DG MOSFET amplifier in Figure 9 is -145°+180°=35°, and in Figure 10, it is -35°+180°=145°.

For two amplifiers shown in Figure 7 and Figure 8, typical phase delays are indicated as being around -35° for the first pole and -145° for the second pole. These poles occur at the phase of +180° and -180°, but these amplifier poles have been created to accommodate the N-channel DGMOSFET for the complete cycle of the input signal. Finally, the proposed distinct ρ-based DGMOSFET amplifier is fundamentally more stable than the conventional DG MOSFET amplifier.

4.3.3. Gain Analysis

Both amplifiers in the system shown in Figure 7 and Figure 8 are provided by a 10 V and 12 V to investigate the lower furthest reaches of the impact. It has been seen that the DG MOSFET device can protect its benefit for input signs of 1mV 2 kHz and 5mV 3 kHz in Figure 7 and Figure 8, individually. In any case, changes can be noticed for the 1mVpk signal at Vcc = 10 V, involving the DG MOSFET increase in Figure 7. This way, the device can increase strength for little signals with less voltage.

Noticing the increase allows the amplifier's capacity to be applied in a region of supply voltages, as shown in Figure 11 and Figure 14. From the observations, as shown in Figure 12 and Figure 15, the increases for the two amplifiers are protected for the supply voltage scope of 10 V to 12 V. For the DG MOSFET device, voltage gain (dB) increase is available for an information voltage of 5 mV, and a voltage of 12 V from 20 dB to 40 dB as shown in Figure 13 and Figure 16. From this, the DG MOSFET device can protect its usage at this supply voltage.

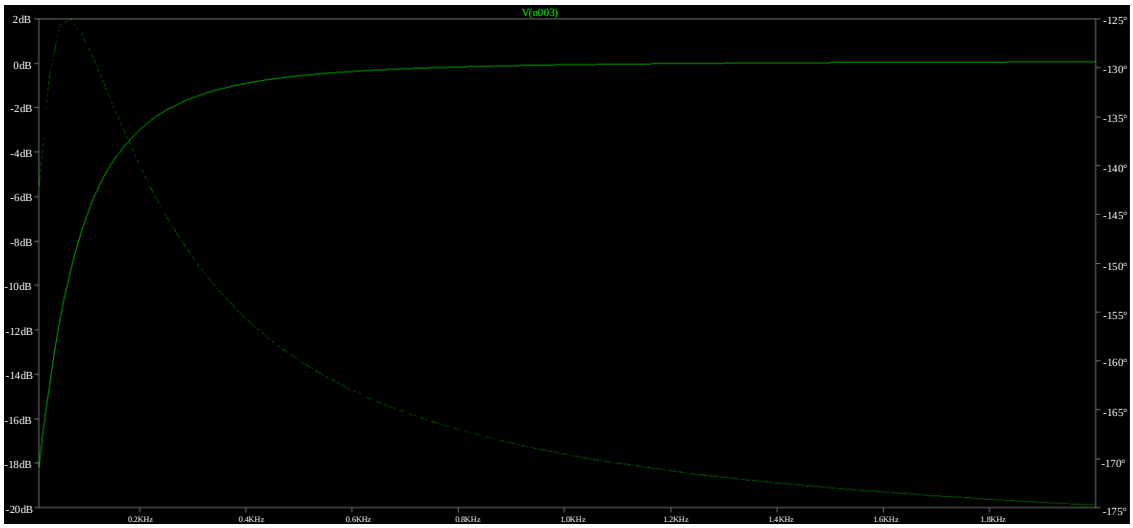


Fig. 9 For back gate design: Illustration of observed passband bandwidth of 2.18 KHz

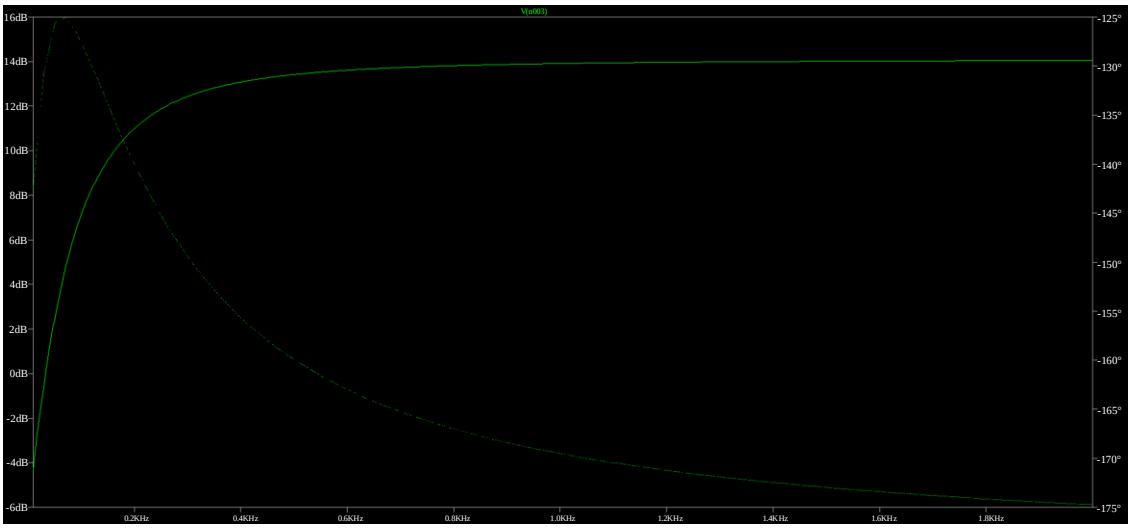


Fig. 10 For front gate design: Illustration of observed passband bandwidth of 2.18 KHz

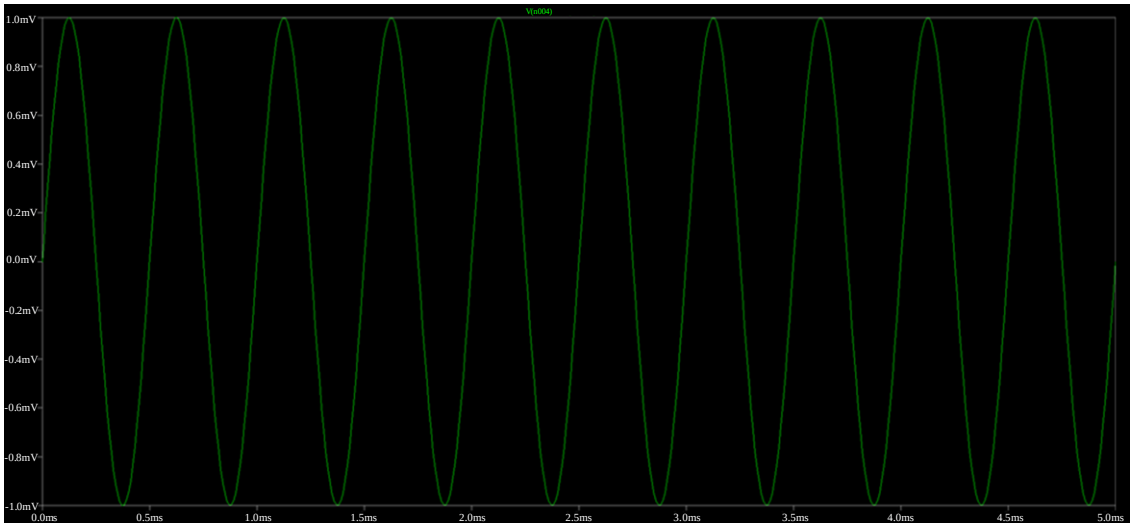


Fig. 11 Input waveform with 1mVpk at 2 kHz frequency with Vcc=10V

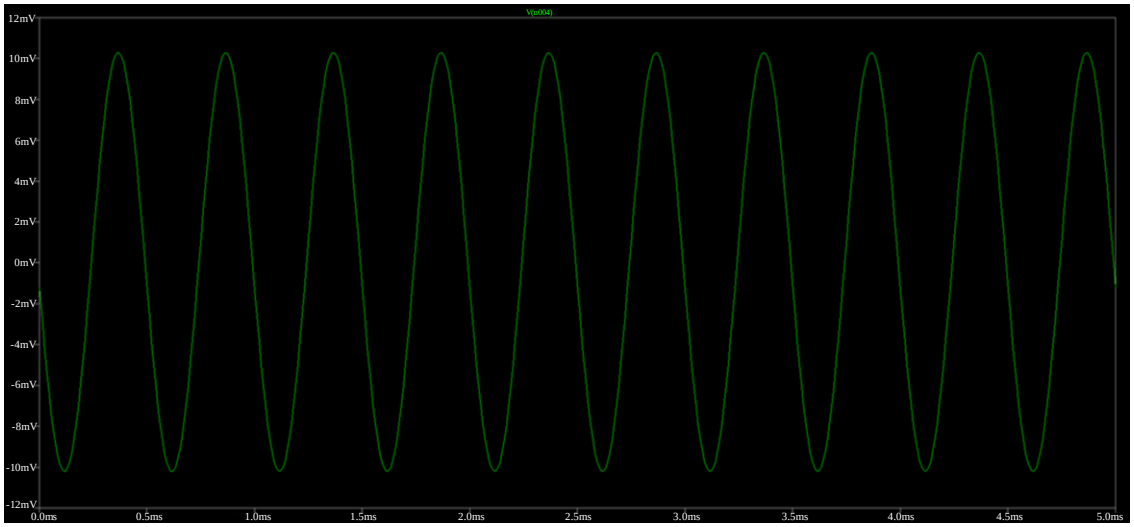


Fig. 12 Output waveform with 10mVpk at 2 kHz frequency with Vcc=10V

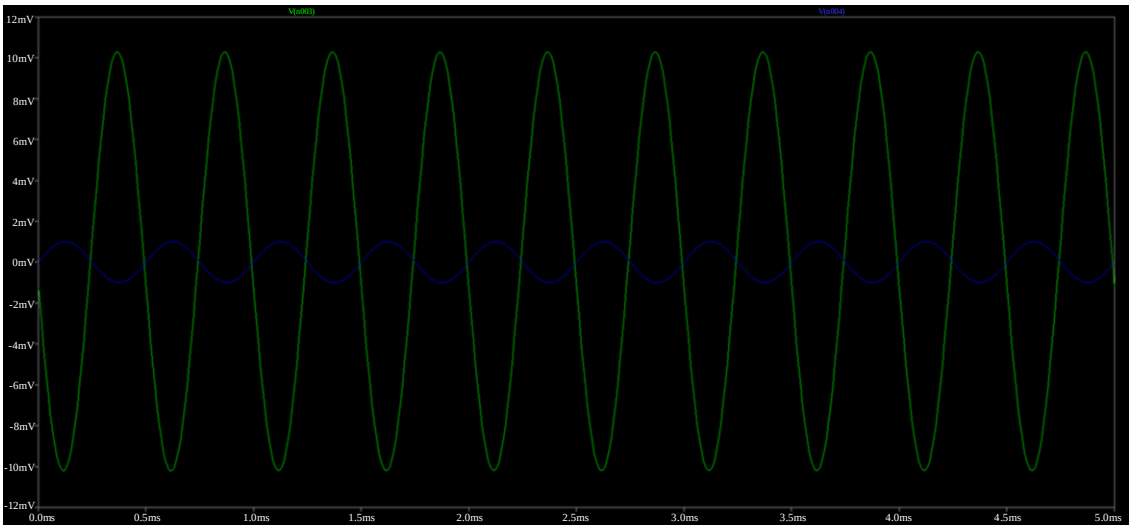


Fig. 13 Voltage gain (dB)= 20 dB for input waveform with 1mVpk and output waveform with 10mVpk at 2 kHz frequency

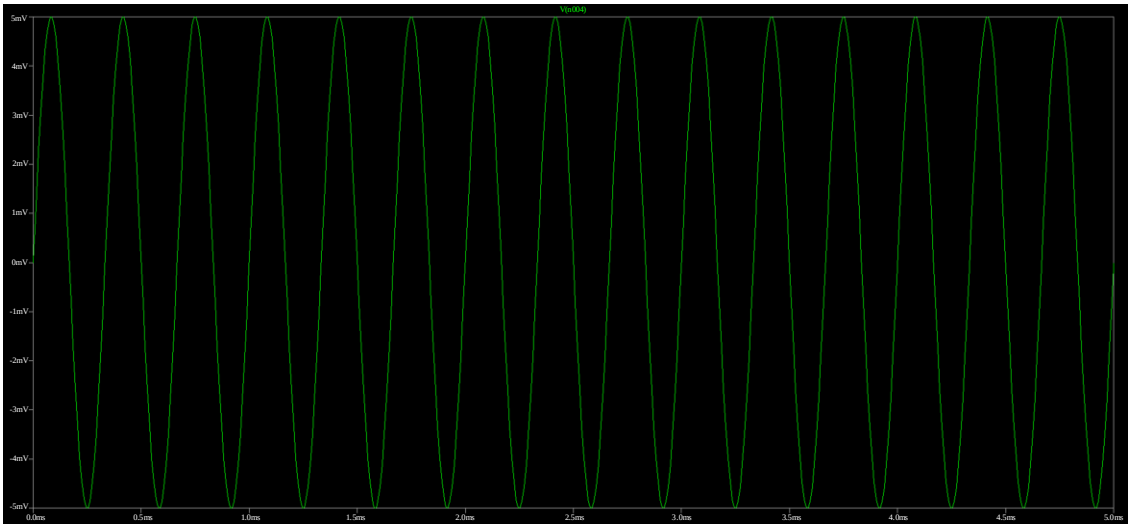


Fig. 14 Input waveform with 5mVpk at 3 kHz frequency with Vcc=12V

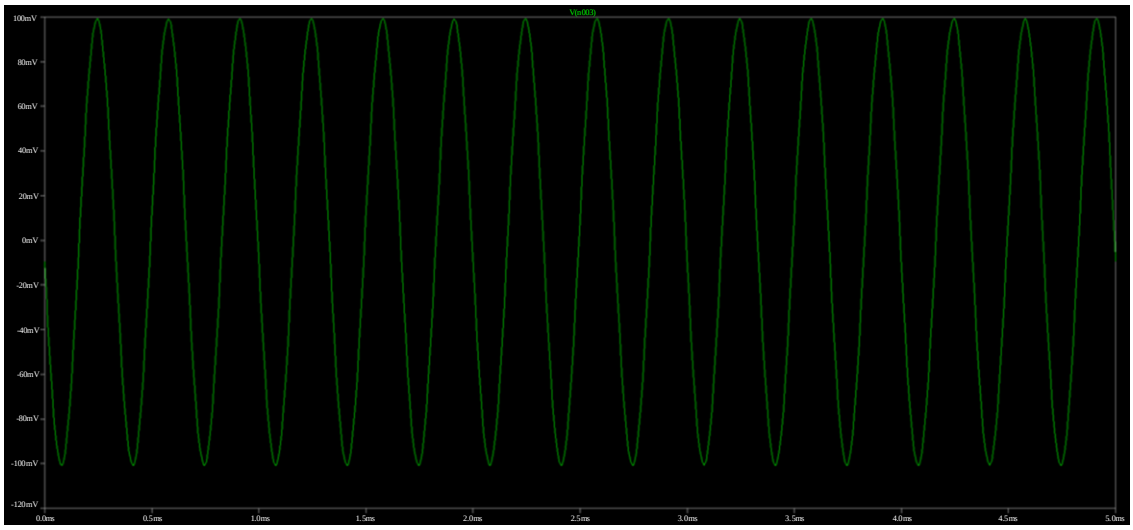


Fig. 15 Output waveform with 100mVpk at 3 kHz frequency with Vcc=12V

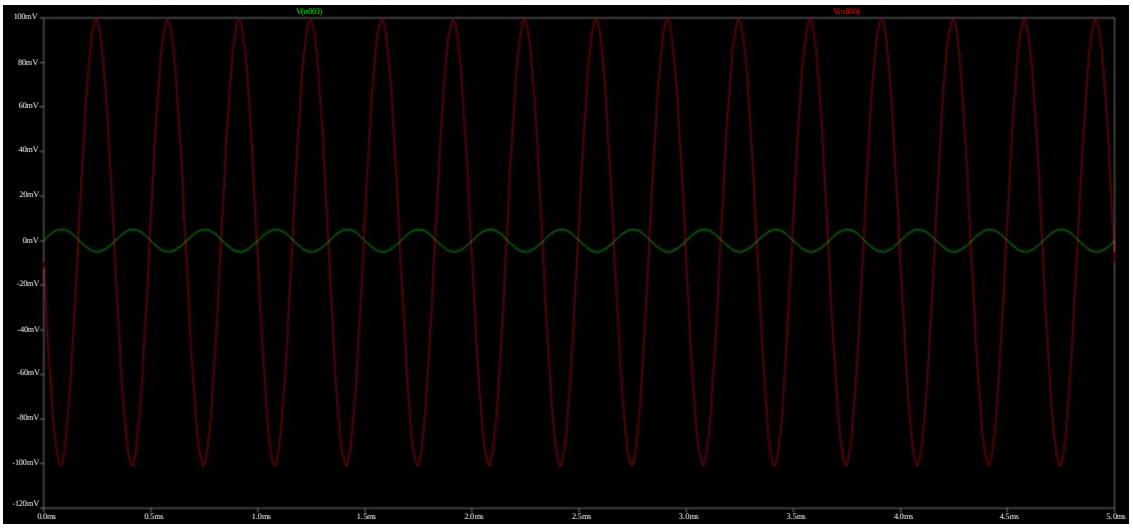


Fig. 16 Voltage gain (dB)= 40 dB for input waveform with 5mVpk and output waveform with 100mVpk at 2 kHz frequency

Table 10. Electrical characteristics for different channel thicknesses @ VGS=2.0V and @VDS=2.0V

Process	D Ccon (cm^{-3})	t_{Si} (nm)	I_{ON} (mA)	I_{OFF} (mA)	V_{tsat} (mV/decade)	SS_{sat} (mV/decade)	DIBL (mV/V)
Without distinct-ρ	2×10^{18}	20	3.9	$7.22 \times 10^{+3}$	0.24	61.98	20.31
Without distinct-ρ	3×10^{18}	5	2.5	$5.89 \times 10^{+1}$	0.19	54.22	22.34
With distinct-ρ	2×10^{18}	20	3.2	$2.78 \times 10^{+1}$	0.35	71.22	19.22
With distinct-ρ	3×10^{18}	5	2.2	2.1×10^{-2}	0.29	69.87	21.45

4.3.4. Output Impedance

Using the two amplifiers, 10 kΩ loads have been utilized to close the circuit circle. This should be visible as open-circle voltage Vopen=100 mVpk and short-circle voltage 70 mVpk. As recently referenced, an amplifier that can be designed with better impedance is a more advantageous device. From the design of both amplifier models of DG, designers have noticed indistinguishable result impedance.

4.4. A 90 nm TCAM Using 6T Bit Cell: An Application of Proposed Distinct ρ-Based DGMOSFET

A reconfigurable CAM circuit based on an ordinary, 6T SRAM bit cell that further develops as much as possible is proposed in this paper. Configurability includes permits device design modes among BCAM, TCAM, and SRAM. Along these, an SRAM is configured as TCAM to speed up equal match-like applications. SRAM mode is as yet utilized as expected with word line addresses, words put away in columns, and information in each line. The proposed memory is configurable for proper power utilization in the design. Utilizing a 6T DGMOSFET TCAM cell, as 64x64 TCAM consumes 1.6 fJ/bit/search shown in Table 10. Changes in the design of the proposed 6T DGMOSFET TCAM cell-memory configurations are made. The proposed 6T DGMOSFET TCAM cell memory provides TCAM in process mode contrasted with a TCAM for the region and proper power utilization in the design improvement over a regular TCAM. Likewise, the changes in the proposed design improved by 25% more than a regular TCAM because of the circuit improvements.

4.4.1. TCAM Mode Operation

TCAM mode is the same as BCAM based on the design of the CAM cell. In the TCAM design, 0, don't care, and 1 condition is addressed, which requires two devices for each cell. Therefore, two appliances must be utilized for each word, as illustrated in Figure 17, and consequently, the amount of cycle duration becomes half.

To address the TCAM cell bit values, '01' is used for combination design to use essentially 00 and 11 differently. During the TCAM operation read, the main contrasts with the BCAM comparison mode are the '01' and '10', as each word traverses two devices, as observed in Figure 18. In mode '01', two devices of the four-device produce lengths of '01' and '10' segments comprising a word length to perform AND operation as-together.

A bit segment-'11' won't provide the detected-bit-line or bit-line-bar because it has bit segment-'1' in the two-devices. Thus, these segments offer both-0-and-1 of the query information.

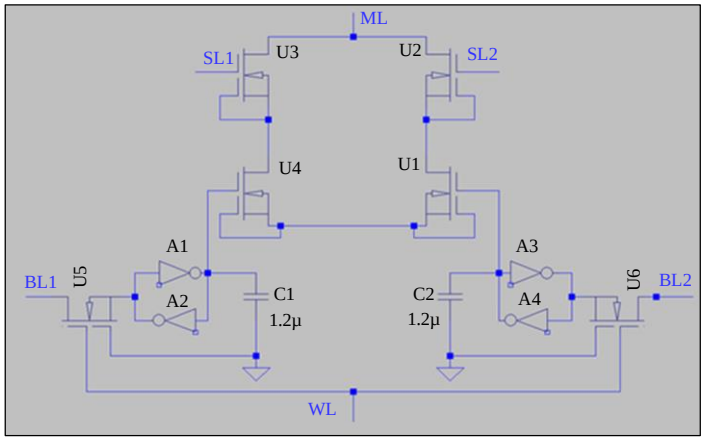


Fig. 17 Proposed TCAM using 6T bit cell

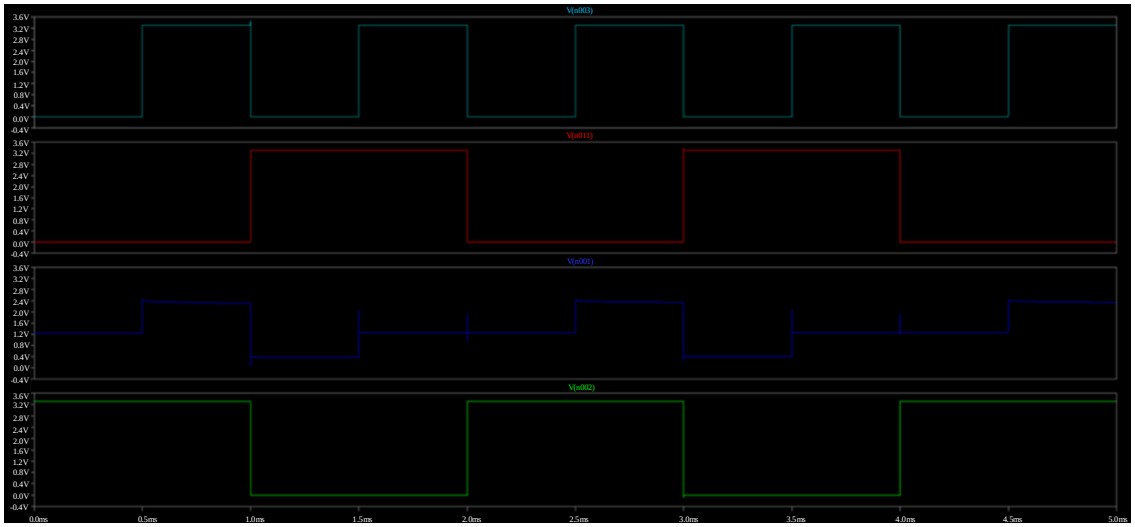


Fig. 18 Composed-'11' TCAM writes operation

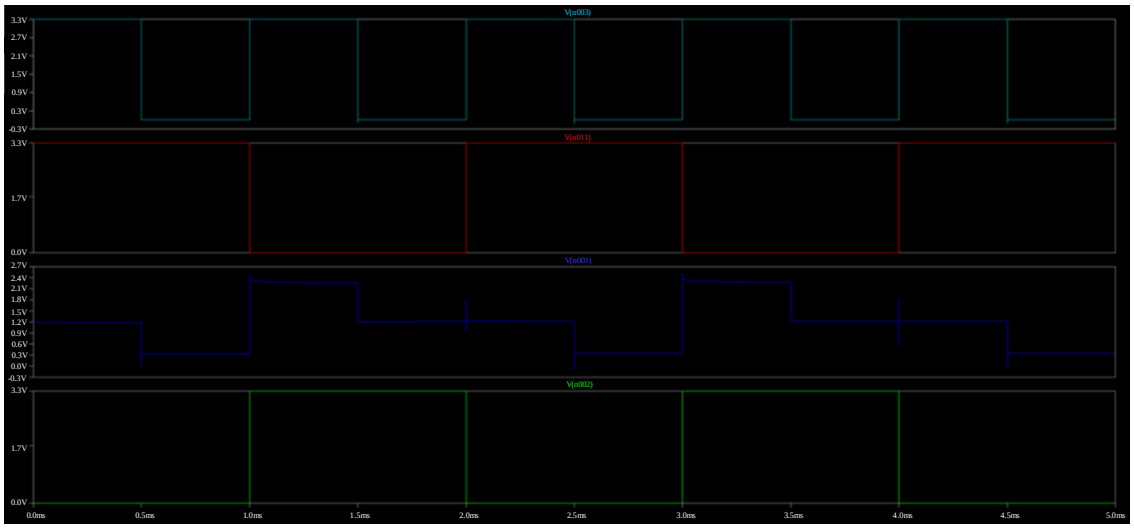


Fig. 19 Composed-'00' TCAM writes operation

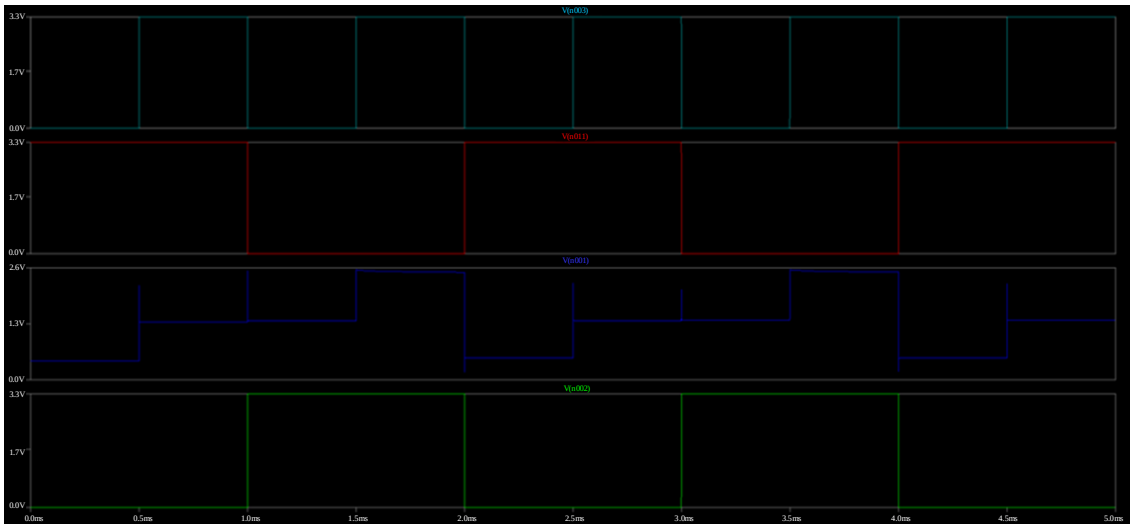


Fig. 20 Composed-'10' TCAM write operation

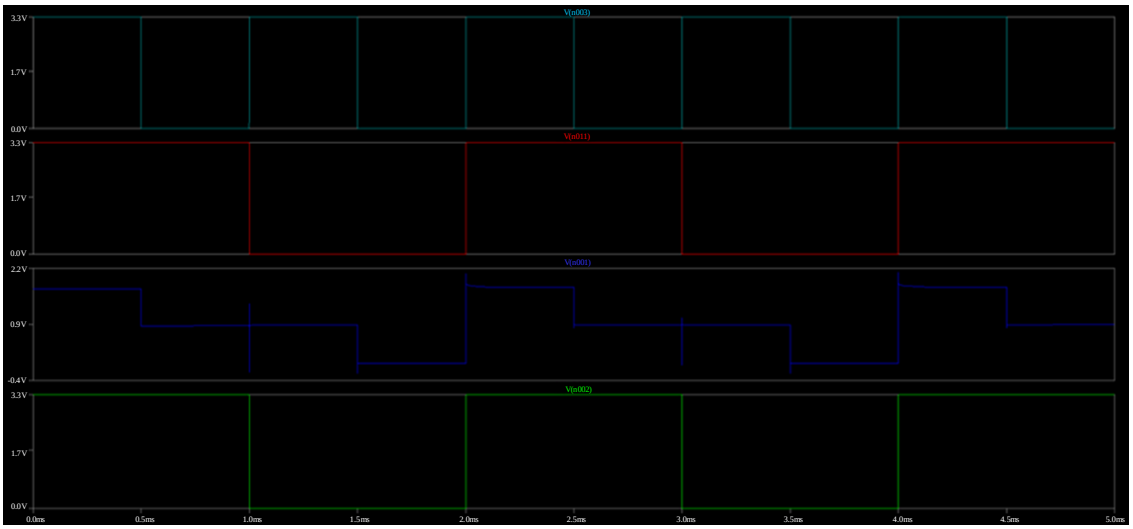


Fig. 21 Composed-'01' TCAM writes operation

As shown in the model in Figure 19, the top-devices circuit-design highlighted in matrix form is analyzed; having subsequent word-two-devices matches '1110'. With the top devices-circuit-design having better circuit performance, the subsequent word-two-devices would have similar-matchstring '0001'.

The design of TCAM with BCAM similarity needs four cycles. The first-two-cycles are composed-'11' and composed-'00'. The third cycle store-bit-'01' provides the word-devices-lines of columns considered for circuit design. The word-devices-lines cells are considered with composed-'01', with the proper bias-voltage for device-bit-lines, as illustrated in Figure 20. And in Figure 21, the fourth cycle is to the designed and proposed TCAM, which provides match and non-match waveforms. X-cell-bit and X-cell-bit+1 are having composed-'11', and Y-cell-bit and Y-cell-bit+1 are having composed-'00'. During match operation, the match-bit segments word as rows, Z-cell-bit having composed-'0' and Z-cell-bit+1 have composed-'1' as shown in a match and nonmatch waveforms. Since data availability is more uncommon in numerous CAM applications than searhkach, the extra cycles present less above.

Table 10 compares the electrical characteristics of the device proposed with various channel thickness tSi(nm): 5 and 20 nm with the values of VGS=2.0V and VDS=2.0V. Device parameters compared for our method analysis are DCcon, tSi, Vtsat, SSsat, and DIBL. Table 10 shows that for DCcon = 3 x 1018 cm-3, tSi=5 nm, the methods without distinct ρ-model give IOFF = 5.89 x 10-1 mA, which is high compared to method with distinct ρ-model with a better ION reduction. In this analysis, DCcon = 3 x 1018 cm-3 and DCcon = 2 x 1018 cm-3 are considered with tSi=5 nm and 20 nm to compare with the device parameters to verify the proposed distinct ρ-model can reduce SCEs. Here, DCcon is channel doping concentration, tSi is silicon thickness, Vtsat is the saturated threshold voltage, SSsat is saturated Sub-threshold Slope, and DIBL is Drain Induced Barrier Lowering.

The numerical simulation of the device proposed at a 90nm technology node is carried out using the TCAD tool. The proposed device's performance can be further enhanced by introducing high-k dielectric gate materials. Comparative technology CAD device simulation parameter results obtained in this work are shown in Table 11. The parameters of the device proposed by DGMOSFET are summarized and compared with other DGMOSFET designs of the proposed work, and the design analysis results are illustrated in Table 11. The device design parameters of the proposed distinct ρbased DGMOSFET device TCAM cell are compared with similar work published device models in Table 12. With 4T4M, the TCAM cell is proposed to have a minimum number of devices in the cell design, with only four transistors.

From Table 12, the use of a distinct ρ-based DGMOSFET device in the TCAM memory cell compared to previous TCAM cells makes the device energy efficient as the leakage current is reduced by limiting the electrostatic control over the channel through scaling the ρ-element-charge component. Also, the distinct ρ-based DGMOSFET device TCAM memory cell makes the device less search delay as the proposed binary-memory switch reduces the timing violations by reducing the number of cell-device components.

Table 11. Proposed DGMOSFET device comparison with similar DGMOSFET design works of literature survey

MOSFET Device	Parameter		
	Channel Length (Lg)	ON-State Current / OFF-State Current (ION/IOFF)	Subthreshold Swing SS (mV/dec)
Quad Gate SB-MOSFET [18]	17nm	3.3×10^{11}	60.65
Conventional SB-MOSFET	17nm	1.1×10^{6}	75.81
JL-DM-GSDG-MOSFET [19]	50nm	7.75×10^{4}	80.74
Conventional JL-DM-DG-MOSFET	50nm	3.80×10^{6}	70.32
Conventional DG JLT with SiO_2	32nm	3.86×10^{6}	66.49
Conventional DG JLT with Multi oxide	32nm	9.4×10^{7}	63.24
Conventional DG JLT with HfO_2	32nm	5.25×10^{9}	61.12
Proposed DGMOSFET	30nm	471.7930	106.9
Proposed DGMOSFET	40nm	1.384x103	90.9

Table 12. Performance comparison of the device proposed TCAM cell and prior works

Parameters	Hayashi I. et al., [20]	Zheng L. et al., [21]	Proposed Work
Technology (nm)	65	180	90
V_{DD} (V)	1	1.8	1
CAM/TCAM Cell device	TCAM	TCAM	TCAM
Cell Structure (T / M / T and M)	16T	5T2M	4T4M
Cell-Type (B / T): Memory	Ternary	Ternary	Ternary
Work-Length (bit)	72	128	128
Search-Delay (ns)	1.9	2	1.5
Search-Energy (fj/bit/search)	1.98	0.99	1.6

5. Conclusion

A novel static-based architecture is illustrated using a binary-memory switch for non-volatile data storage for the proposed distinct ρ-based DGMOSFET device TCAM. The possibility of storing the content-data bits in one TCAM cell for analysis reduced the search delay through available timing violations. A further reduction in search energy is achieved as the distinct ρ-based DGMOSFET-TCAM through four transistors and four memristors. An improved content-data search and data-write operation technique are presented.

A suitable match line is considered for enhancing content-data search time. With two different system clocks, the working of illustrated work is evaluated. The distinct ρ-elements in the proposed TCAM cell through distinct ρ-based DGMOSFET device were analyzed using the TCAD tool.

Simulation results show a better content-data search speed and low search delay of the cell design with DIBL (mV/V) of 168.9 and 126.0 for channel length (Lg) of 30 nm and 40 nm, respectively. The functional parameters of TCAM are simulated through Monte Carlo simulation. The comparative analysis with 128-bit has shown improved results. The distinct ρ-based DGMOSFET device may be extended for multi-core TCAM cell design with an increase in word length for every 64-bit cell array segment.

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