SSRG International Journal of Electrical and Electronics Engineering
ISSN: 2348-8379 / https://doi.org/10.14445/23488379/IJEEE-V10I2P116

Volume 10 Issue 2, 172-179, February 2023

Original Article

Implementation of M-Type Carrier-based PWM Method for 13-Level Multilevel Inverter

R. Sindhuja[1], S. Padma[2]

[1,2]*Department of Electrical Engineering, Faculty of Engineering and Technology, Annamalai University, Tamil Nadu, India.*

[1]*Corresponding Author: sindhuja.gct@gmail.com*

Received: 09 January 2023 Revised: 10 February 2023 Accepted: 20 February 2023 Published: 28 February 2023

Abstract *- In order to construct the levels for staircase waveforms, this study introduces a module for reconfiguring asymmetrical multilevel inverters that use DC link capacitors. The multilayer converter's configuration reduces the count of DC sources. Lower DC sources, on the other hand, permit the creation of 13 levels. The suggested multilayer inverter module generates 13 levels from two erratic dc sources (2VDC and 1VDC). 14 semiconductor switches and two charged capacitors are also included. The capacitors self-charge without the use of an additional circuit. Because there are fewer components, it is beneficial to employ them in a variety of applications. Additionally, it can be coupled in a modular cascade, creating a structure with additional voltage levels at greater voltages. The suggested module generates negative voltage levels naturally and without employing a unique circuit (such as an H-bridge circuit). To provide a superior sinusoidal output voltage, M-type carried-based switching modulation approach is used. The main novelty of this article is implementing a new M-type carrier-based PWM technique applied in the recently introduced 13-level MLI. The simulation and testing findings demonstrate good performance, and Simulink /MATLAB are used to run simulations.*

Keywords *- Cascaded H Bridge, Multilevel inverter, 13-Level, Power quality, Pulse width modulation, Total harmonic distortion*

1. Introduction

The In an effort to lessen reliance on conventional fuels and cut CO2 emissions, Renewable Non-conventional sources like photovoltaic (PV) and wind generation have undergone extremely rapid improvement, especially in the previous ten years. Multilevel voltage source inverters (MVSI) are demonstrating great promise and competitiveness as power converters in various industrial applications, such as electric drives, uninterruptible power supplies (UPS), and active power filters where quality standards are high. These applications include the grid integration of renewable resources. The employment of conventional inverters was prominent in the industry. Multilevel inverters (MLIs) have been providing top-notch voltage source converters to bridge the system that generates DC power to AC power systems.

1.1. Literature Review

MLIs come in a wide range of designs, and they are one of the fascinating circuits in the field of power electronics. Recently, the variety of topologies has extended them to a wide variety of applications in the power system [1-3]. Leading converters in PV systems, active power filters, HVDC for the transmission line, drive systems, power grid and electric vehicles; MLIs outperform two-level inverters in applications that demand medium- to high-power [4-5]. Due to their numerous output levels, MLIs feature low harmonic components and good output voltage resolution. The ability to link in a cascade gives them little load on switches, modularity, and scalability. Massive capacitors, unbalanced dc links, and severe switch stress are additional NPC and FC downsides. [6-7] Smaller component counts are hence the focus of research and are utilized to develop CHB topologies. The total standing voltage (TSV), intrinsic creation of negative levels, number of levels, number of dc sources, number of semiconductors, and others all share characteristics with these topologies, [8], [9] etc. To add further levels, the module can be joined in series.

On the other hand, if all levels are positive, then a second circuit is required to produce negative levels. In [29], the sinusoidal waveform in staircase format (positive and negative half-cycles) is introduced with an H-bridge to the series modules. The semiconductors used in H-bridge circuitry, which bring negative voltage levels, can handle higher switching stress. Typically, MLIs connect various semiconductor switches in different ways to synthesise a number of tiny voltage steps that come together to create a staircase output waveform. One of the key problems with MLI configuration is using cheaper components to provide

larger output voltage levels. The best way to solve this problem is to use unequal dc links. Asymmetric multilevel inverters with uneven dc links feature an innovative configuration that cuts the number of devices while enhancing output voltage levels. Power electronics semiconductors use dc linkages to add or subtract to build modules.

On the other hand, the voltage stress on switching devices in asymmetric multilevel inverters should be considered due to the multiple different DC supplies. TSV is the total voltage stress that appears across each switch in the off state. Crossing switches for dc links with opposing polarity were added to create more levels and divide the demand for switches [11]. In [12] and [13], extended H-bridges with various numbers of DC linkages are presented. These topologies have higher levels, which put more strain on the switches and the need for faster semiconductors. In [14], a different type of MLI is proposed in the form of hybrid-type topologies. Because of the achievement of more levels from available four DC sources, [15], [16] presented modules with low semiconductors with intrinsic negative levels.

MLI evolution cultivates to reduce components, particularly DC supplies, which have recently been replaced with passive circuit elements like capacitors. A suitable topology can provide a sinusoidal voltage source using mixed capacitors and dc sources. However, additional output levels can be produced by using the same DC sources. [17,19,30] Redesigned the configuration with a few capacitors to store energy and eliminate a few dc sources.

The widespread use of carrier-based PWM is a result of its straightforward design. Typically, carrier waves have a triangle or saw-tooth shape. Triangular and saw-tooth carriers are employed in the most widely used modulation method. M-Type carrier shapes are presented in this research, and their effectiveness is evaluated compared to that of triangular carriers. The M-type carriers are named because they are made up of alternating up and down-facing parabolas connected in series. The main driver for producing the distinctive M-type carrier waves was the impact of the carrier signals' effects on the whole PWM technique. In the past, [20,31] created half-parabolic carrier waveforms along with integrated active capacitors for voltage balancing into the half-parabolic carrier to leverage for capacitor voltage balancing with redundant stage. The full parabolic carrier was provided in [22-26] and used as an example to show how it improves the overall calibre of the output waveforms. M-type carrier waves are introduced in this study as a result of a couple of the fore-mentioned breakthroughs. [27-28] The modulation strategy improves the quality of the output waveforms and produces high rms voltage and low harmonic voltage compared to traditional PWM methods.

This paper describes a semiconductor arrangement with two unequal DC sources and capacitors used as DC links that achieve higher voltage levels, thereby improving implementation cost and power quality. With just two uneven DC sources of 1VDC and 2VDC, it can produce 13 different voltage levels. On the other hand, an asymmetric multilevel module is proposed to produce 6 positive and negative levels each and a zero level (total of 13 levels) without any extra circuit to generate negative voltage. The proposed module contains 14 power switches and 2 capacitors. The module is easily cascaded in series to obtain higher output voltages. Section II depicts the proposed multilevel inverter, module description, switching patterns, self-charging and discharging capacitors without any extra circuitry and a table of comparison with similar structures. The M-type PWM approach is used in this article, and Section III provides more details. The suggested work is simulated in Section IV, along with comparisons to alternative PWM techniques. Section V concludes the work.

2. Investigation on Proposed 13 Level MLI

A suitable power converter design can produce more output voltage levels from two different DC sources. Capacitors can be used to establish additional DC links to obtain higher levels than expected. The path in which capacitors get charged is provided in this type of configuration in addition to the output level paths. Two dc sources with varying voltages of 1VDC and 2VDC are present. There are more voltage levels and fewer harmonic components when different DC Power voltage sources are used for asymmetric MLI. It might be better to use capacitors to add two more DC links. It offers a total of four DC links. The suggested module is seen in Fig. 1 with a configuration that consists of 14 switches, of which 8 are unidirectional, and 3 are bidirectional, 14 diodes, two distinct DC sources, and two capacitors. This setup produces one zero, six positive, and six negative levels.

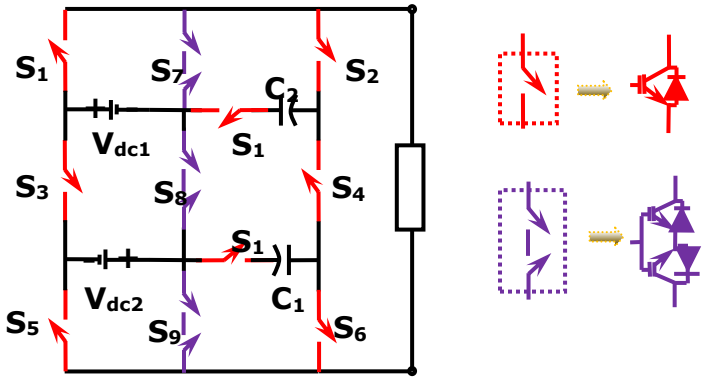


Fig. 1 Topology of 13 level MLI

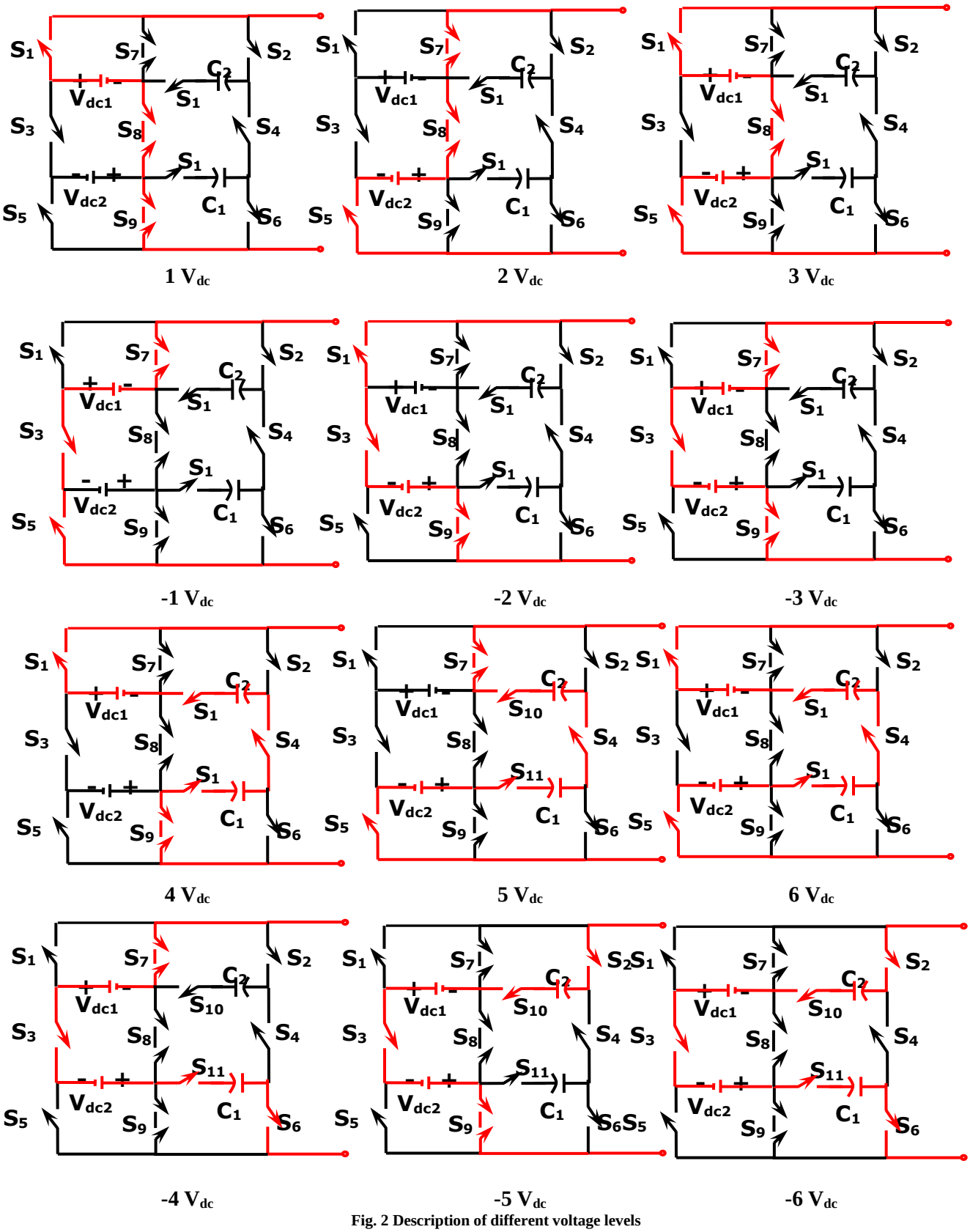


Fig. 2 Description of different voltage levels

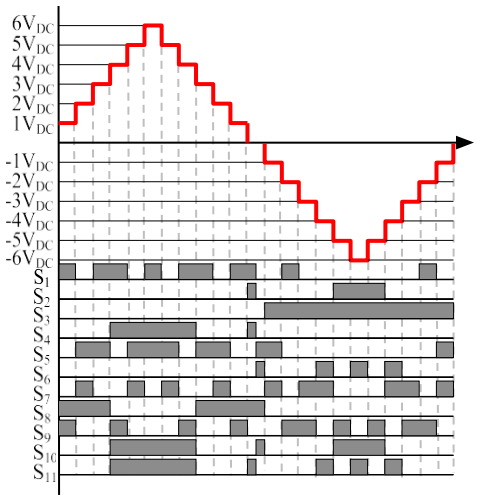


Fig. 3 Switching pattern for 11 Switches

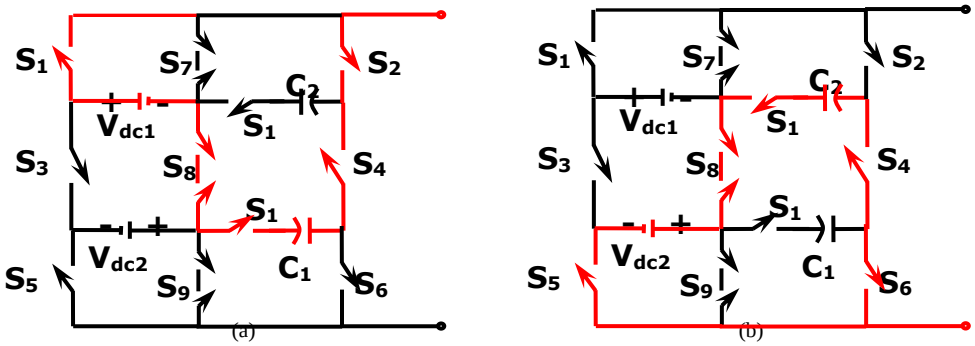


Fig. 4 Capacitor charging switching path (a) (b)

Table 1. Switching sequence for 11 switches

Levels	V_{out}	State of Switches										
		S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8	S 9	S 10	S 11
Positive Level	6 V_{dc}	1	0	0	1	1	0	0	0	0	1	1
	5 V_{dc}	0	0	0	1	1	0	1	0	0	1	1
	4 V_{dc}	1	0	0	1	0	0	0	0	1	1	1
	3 V_{dc}	1	0	0	0	1	0	0	1	0	0	0
	2 V_{dc}	0	0	0	0	1	0	1	1	0	0	0
	1 V_{dc}	1	0	0	0	0	0	0	1	1	1	0
	0 V_{dc}	1	1	0	0	0	0	0	1	0	0	1
Negative Level	-1V_{dc}	0	0	1	0	1	0	1	0	0	0	0
	-2V_{dc}	1	0	1	0	0	0	0	0	1	1	0
	-3V_{dc}	0	0	1	0	0	0	1	0	1	1	0
	-4V_{dc}	0	0	1	0	0	1	1	0	0	0	1
	-5V_{dc}	0	1	1	0	0	0	0	0	1	1	0
	-6V_{dc}	0	1	1	0	0	1	0	0	0	0	1

The major idea behind this configuration is to establish various routes from various sides in order to connect other DC links in order to achieve negative levels and eliminate the H-bridge. It is seen that the power source with 2VDC charges the C2 capacitor without the need for an additional circuit, whereas the DC supply with 1VDC charges the C1 capacitor. The switching structures of the output levels in the proposed design are presented in Fig. 2 and Table I. The module's design and the switching routes' selection ensured no positive poles would be conducted in the diode on its anode side. Additionally, Fig. 3 demonstrates that the no switches need to be turned on to create a close loop for DC links. In order to prevent short-circuiting in the module, even when switches are disabled, diode polarity and switches are used.

Table I shows the switch modes for each level. There are also redundant paths from other dc links for some levels. To avoid a short circuit between both sources, switches (S1 and S7), (S3 and S8), and (S5 and S9) cannot be switched on/off simultaneously. A low frequency is used to turn on switches S2, S3, S4, and S8, as shown in Fig. 2, reducing switching losses. The remaining switches will function at a reasonable switching frequency as well. Figure 3 depicts the proposed inverter's schematic voltage at the output with the related signal sequence in one fundamental voltage cycle.

Another configuration capability is the capacitors getting charged without using an extra circuit. The module is constructed with pathways for DC links to get charged. At level zero, state capacitors have been charged. The charging path for capacitors is shown in Fig. 4, with a 1VDC DC

source charging C1 as shown in Fig. 4(a) and a 2VDC DC source charging C2 as in Fig. 4(b). It is evident from Fig. 2 that capacitor charging can take place at a zero level. Additionally, capacitors will charge after every half-cycle. The application will determine how many capacitors are needed to maintain charging for at least one half-cycle.

3. Modulation Techniques

The literature has suggested a number of modulation techniques for direct the operation of MLI circuits. This portion discusses recently produced M-type carrier-based PWM. The suggested modulation technique belongs to the level-shifted modulation techniques category (LS-PWM). Phase disposition (PD), alternative phase opposite disposition (APOD) and opposite phase disposition (POD) are the three traditional categories for level-shifted modulation techniques (APOD). All three of the categories are applicable to the presented MLI structure. To reduce the sideband harmonics present in traditional PWM techniques, the modulating wave frequency must eventually be lesser than the modulating wave frequency. This part demonstrates the creation of modified carrier signals, known as M-type carriers.

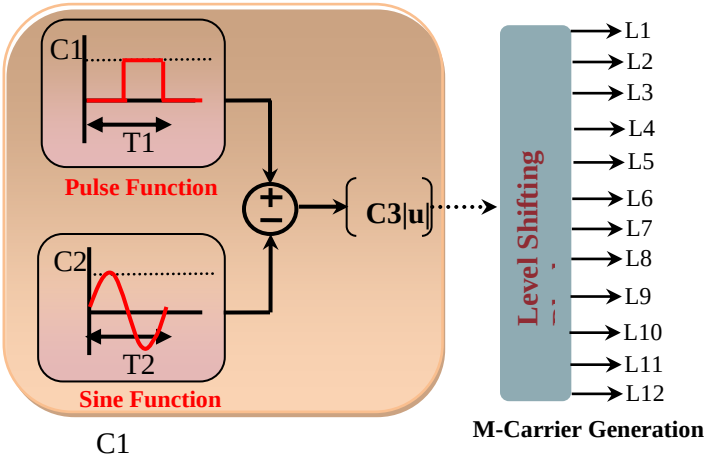
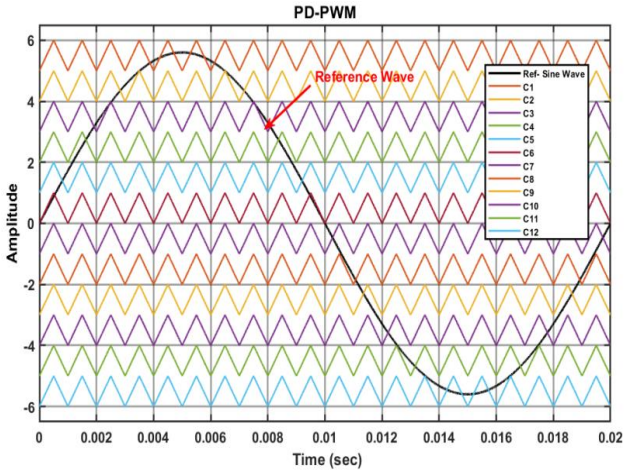


Fig. 5 Block diagram for M-type carrier wave generation

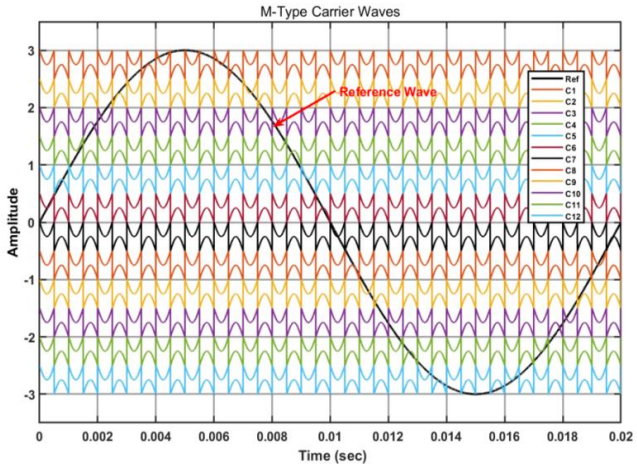
Table 2. Simulation parameters

S. No.	Parameter	Value
1.	V1 : V2	1: 2 V_{dc}
2.	V_{dc}	100 V
3.	Fundamental Frequency	50Hz
4.	Switching Frequency	2 kHz
5.	Resistive Load	100 Ω
6.	Inductive Load	40 mH
7.	Capacitors (C1: C2= 1:2) C1	100 µF

Fundamentally parabolic in nature, the M-type carrier waves are produced by various combinations of them. The techniques significantly govern the semiconductor's maximum value, average value and ripple readings under various types of pulse width modulation (PWM). A new carrier wave of M-type is suggested to oversee and eliminate the harmonic content present in the output voltage at lower switching frequency values and boost overall production. The creation of M-type carrier signals using sinusoidal and pulse functions is shown in Fig. 5. By keeping the frequency ratios of the sinusoidal function f2 and pulse function f1 at 1:1 (f1 = f2), the M-type wave can be produced. The same generator can create different wave types by changing the frequency ratio between the two functions. The values of the coefficients C3, C2, and C1 are assessed to be 0.5, 0.5, & 0.5, accordingly, in the M-type signal generator depicted in Fig. 5. The level-shifted PWM is made up of a sinusoidal wave taken as reference signal with fundamental frequency designated as Vref and twelve carrier signals known as M-type carriers labeled as L1 to L12 in increasing order.



(a)



(b)

Fig. 6 Carrier waveforms (a) Triangular type (b) M-Type

The inverter is controlled using the level-shifted PWM approach. PWM pulses, which can be compared to carrier signals and reference signals with underlying frequency, are formed as a result of the constraint of the signal amplitude

produced in the prior step, which establishes the size/amplitude of a specific voltage level. The PWM pulses for the 13-layer synthesis of desired amplitude are then added to get the indented switching function. As seen in Fig. 6, the sinusoidal wave, which has a fundamental frequency of 50Hz, acts as the reference wave for both level-shifted PWM scenarios (M-type and triangular-type carrier). In both instances, each level-shifted carrier has a magnitude of 0.5. The carrier wave has a frequency of 2000 Hz. 12 vertically shifted carrier waves with an amplitude of 0.5 are generated.

4. Results and Comparison

The simulation was done in the MATLAB Simulink environment for steady-state performance. Table 2 displays the parameters used for the simulation. All modulation techniques use the same DC source of 100 volts. Loads of RL nature having the value of Resistance 100Ω and Inductance of 40mH were utilized under operation. Capacitors with 200F and 400F were used to assess the impact of various PWM carriers on the converter's performance.

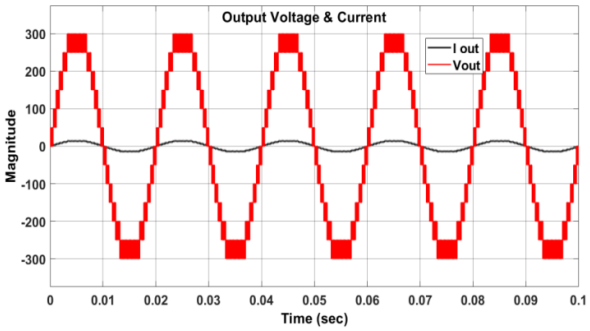


Fig. 7 Output Voltage and Current waveforms

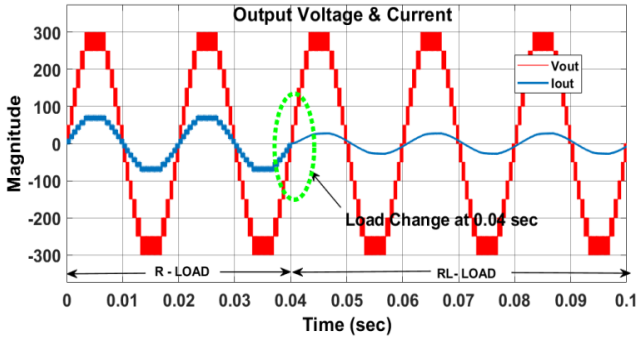


Fig. 8 Output voltage and current waveforms for dynamic load variation

A switching frequency of 2 kHz was selected. PWM carrier waves of both types were generated and applied to a 13L-MLI. Voltage and current waveforms from both carriers' waveforms were analysed for harmonic content. The 13-level voltage appeared across the load terminal, and the wave shape of current through the load when the triangle carrier is utilised is depicted in Fig. 7. The percentage of harmonic distortion that appeared in the voltage waveform is 15.23%. The % THD in the output current waveform is 1.57 percent. The voltage and current wave patterns across load when the suggested M-form carrier is applied are shown in Fig. 7. The output current and voltage respective THDs for the related harmonic spectrum are 0.89 percent and 10.07 percent.

When the load varies from the resistive load of 80Ω to the RL load of 100+j40Ω, wave shaping occurs. The harmonics present in the waveform get reduced, as represented in fig.8. The output current and voltage waveform as the carrier waves' modulation index varies is depicted in Fig. 9. The output levels fall linearly together with the modulation index. The waveform clearly shows that the levels decreased from 13L to 7L MLI from 0.04 sec as the modulation index varied from 0.97 to 0.49. The THD percentage for both carriers when the modulation index Ma = 1 is represented in Fig. 10. The lowest current and voltage THD is found in the suggested M-type carrier, at 0.89 percent and 10.07 percent, respectively. Additionally, the fundamental output voltage is around 298.2 V with a frequency of 50 Hz. The % of harmonic content at the multiple switching frequency is extremely high because the switching frequency is set to 2 kHz. The spectrum analysis of harmonics also demonstrates that higher-order frequencies have a higher THD %.

The variation in the harmonics present across the load for each carrier put in is shown in Fig.10(a). The voltage THD values corresponding to applied carriers employed in the lower modulation index range show a distinct difference. When the modulation index becomes closer to 1, the THD for voltage waveform under both types of carriers under discussion is found to be lesser. In the whole range from ma = 0.2 to ma = 1.0, the voltage THD in M-type carrier waves is found to be lesser than that of triangular carriers.

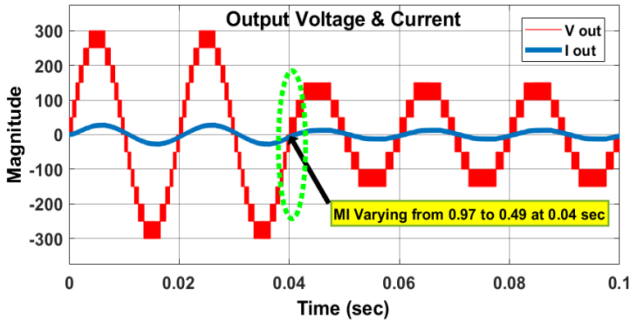
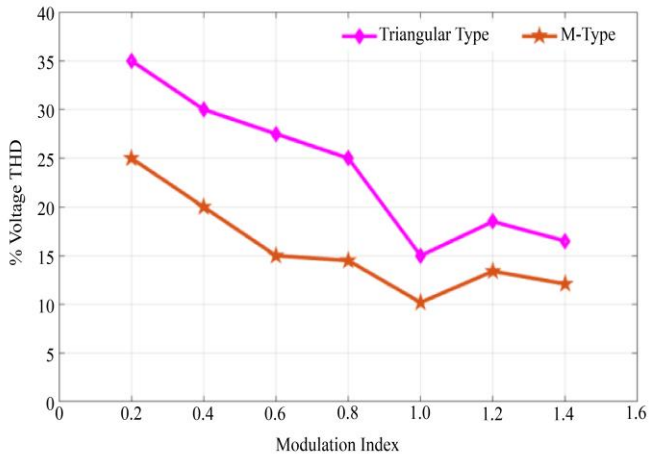
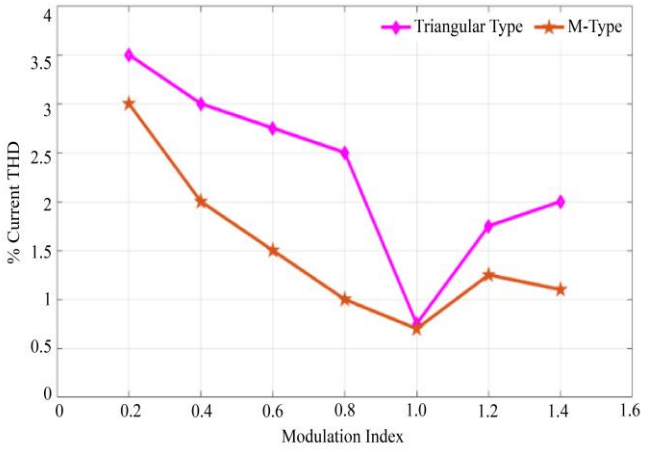


Fig. 9 Output voltage and current waveforms for variation in modulation Index



(a)



(b)

Fig. 10 THD % as modulation Index varies (a) Voltage THD (b) Current THD

Fig.10.b depicts the harmonics present in the current through the load considered under various PWM techniques, both using triangular and M-type carriers as modulation indices ranging from ma = 0.4 to ma = 1.4. A 50Hz frequency is kept constant. 100 ohms and 40 mH are the applied loads. The M-type carrier's current THD sharply decreases from 0.4 to 1.0 before abruptly rising from 1.0 to 1.4 and continuing to rise with a steep gradient. The current THD for M-Type carrier waves ranges from ma = 0.4 to 0.8 and is significantly lower than for Triangular carriers. The modulation index modification has zero effect on the value of the harmonics present. When ma = 1, the present THD values virtually equalize each other.

5. Conclusion

The A recently released 13L-MLI was used to test the suggested M-type PWM approach, and the inverters' performance metrics were compared to those of the traditional triangle PWM. The findings demonstrate that when the modulation index (ma) magnitude is 0 and 1.2, the proposed M-type carrier has the maximum efficiency and lowest voltage THD. A single module of an asymmetrical MLI that produces 13 levels from two DC sources was provided in this article. The model setup uses two additional DC links via capacitors (as virtual dc supply) to add extra levels to the staircase waveform. Compared to other structures, the construction only needs two dc sources, two capacitors, and fourteen semiconductors. It might be utilised in various applications that utilise two dissimilar DC sources (with a ratio of 1:2). Additionally, it is effortlessly expandable by arranging it in a cascade fashion to obtain higher voltage levels with less strain imposed on the devices with fewer components. Numerous unique applications, like a solar field with numerous DC sources, can take advantage of this capacity. DC sources can also have a range of voltage amplitudes. Asymmetrical multilevel converters allow some dc resources to be combined to provide acquired AC output, but conventional approaches suffer from larger losses, greater complexity, and worse efficiency and power output. It reduces, among other things, the number of different inverters, parts, and losses. Another benefit is that even without any additional circuitry, it can produce positive and negative halves of the output. The module has been tested, and it performs well. Voltage and Current THD percent are spotted to be 10.07 percent and 0.89 percent, respectively, which meet harmonics standards (IEEE519).

References

[1] K. Suresh, and E. Parimalasundar, "A Modified Multi Level Inverter with Inverted SPWM Control," *In IEEE Canadian Journal of Electrical and Computer Engineering*, vol. 45, no. 2, pp. 99-104, 2022. [CrossRef]

[2] S. Islam et al., "A Switched Capacitor-Based 13-Level Inverter with Reduced Switch Count," *In IEEE Transactions on Industry Applications*, vol. 58, no. 6, pp. 7373-7383, 2022. [CrossRef]

[3] Shahbaz Ahmad Khan et al., "M-Type and Cd-Type Carrier Based PWM Methods and Bat Algorithm-Based SHE and SHM for Compact Nine-Level Switched Capacitor Inverter," *In IEEE Access*, vol. 9, pp. 87731-87748, 2021. [CrossRef]

[4] Benjamin Kroposki et al., ‘‘Achieving a 100% Renewable Grid: Operating Electric Power Systems with Extremely High Levels of Variable Renewable Energy,” *IEEE Power Energy Magazine*, vol. 15, no. 2, pp. 61–73, 2017. [CrossRef]

[5] K. Suresh et al., “Encapsulated 3ø Converter for Power Loss Minimization in a Grid-Connected System,” *Automatika*, vol. 64, no. 1, pp. 189-197, 2023.2022. [CrossRef]

[6] Ke Jia, “Influence of Inverter-Interfaced Renewable Energy Generators on Directional Relay and an Improved Scheme,” *IEEE Transactions on Power Electronics*, vol. 34, no. 12, pp. 11843–11855, 2019. [CrossRef]

[7] Haitham Abu-Rub et al., "Medium-Voltage Multilevel Converters—State of the Art, Challenges, and Requirements In Industrial Applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581–2596, 2010. [CrossRef]
[8] K. Suresh, and E. Parimalasundar, "A Novel Dual-Leg Dc-Dc Converter for Wide Range Dc-Ac Conversion," *Automatika*, vol. 63, no. 3, pp. 572-579, 2022. [CrossRef]
[9] J. Venkataramanaiah, Y. Suresh, and A. K. Panda, "A Review on Symmetric, Asymmetric, Hybrid and Single Dc Sources Based Multilevel Inverter Topologies," *Renewable and Sustainable Energy Reviews*, vol. 76, pp. 788–812, 2017. [CrossRef]
[10] Ebrahim Babaei, Mohammad Farhadi Kangarlu, and Mehran Sabahi, "Extended Multilevel Converters: An Attempt to Reduce the Number of Independent Dc Voltage Sources in Cascaded Multilevel Converters," *IET Power Electronics*, vol. 7, no. 1, pp. 157–166, 2014. [CrossRef]
[11] Rushikesh S.Shahakar, and Kawita D. Thakur, "Comparative Analysis and Switching Requirements of 1ø Grid Connected Non-Isolated Inverters," *International Journal of Engineering Trends and Technology*, vol. 70, no. 3, pp. 319-326, 2022. [CrossRef]
[12] Ebrahim Babaei, Sara Laali, and Somayeh Alilu, "Cascaded Multilevel Inverter with Series Connection of Novel H-Bridge Basic Units," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 12, pp. 6664–6671, 2014. [CrossRef]
[13] Parimalasundar Ezhilvannan, and Suresh Krishnan, "An Efficient Asymmetric Direct Current (Dc) Source Configured Switched Capacitor Multi-Level Inverter," *European Journal of Automated Systems*, vol. 53, no. 6, pp. 853-859, 2020. [CrossRef]
[14] Emad Samadaei et al., "An Envelope Type (E-Type) Module: Asymmetric Multilevel Inverters with Reduced Components," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7148–7156, 2016. [CrossRef]
[15] Hani Vahedi, and Kamal Al-Haddad, "Real Time Implementation of A Seven Level Packed U-Cell Inverter with A Low-Switching-Frequency Voltage Regulator," *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5967–5973, 2016. [CrossRef]
[16] Vishal Anand, and Varsha Singh, "A 13 Level Switched-Capacitor Multilevel Inverter with Single Dc Source," *In IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 2, pp. 1575-1586, 2022. [CrossRef]
[17] N. Sandeep,"A 13-Level Switched-Capacitor-Based Boosting Inverter," *In IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 3, pp. 998-1002, 2021. [CrossRef]
[18] Asala. S. Al-Dmour et al., "Staircase Modulation Using GWO Technique for CHB-MLI with Symmetrical and Asymmetrical Mode," *International Journal of Engineering Trends and Technology*, vol. 69, no. 8, pp. 71-80, 2021. [CrossRef]
[19] E. Parimalasundar et al., "A Performance Investigations of Modular Multilevel Inverter with Reduced Switch Count," *2022 International Conference on Intelligent Innovations in Engineering and Technology*, pp. 83-87, 2022. [CrossRef]
[20] R. Siva Sai et al., "Explorative Analysis of Various Properties in Transformer Oil Based Nanofluids and Vegetable Oils for a Transformer," *Journal of Green Engineering (JGE)*, vol.10, no.6, pp. 2776-2796, 2020.
[21] Anem Apparo, and G. Chandra Sekhar, "A Grid Connected HRES Using Seven Level Inverter - A Hybrid Mfo-Rbfnn Technique," *International Journal of Engineering Trends and Technology*, no. 68, no. 7, pp. 56-68. 2020. [CrossRef]
[22] Kavali Janardhan et al., "Performance Investigation of Solar Photovoltaic System for Mobile Communication Tower Power Feeding Application," *International Journal of Electrical and Electronics Research*, vol. 10, no. 4, pp. 921-925, [CrossRef]
[23] B. Hemanth Kumar et al., "Control of Modified Switched Reluctance Motor for EV Applications," *2022 Trends In Electrical, Electronics, Computer Engineering Conference* (*TEECCON*), pp. 123-127, 2022. [CrossRef]
[24] B. Hemanth Kumar, "A New Series-Parallel Switched Capacitor Configuration of a Dc–Dc Converter for Variable Voltage Applications," *In Electric Vehicles: Springer*, pp. 247-270, 2021.
[25] E. Parimalasundar, "Fault Diagnosis in a Five- Level Multilevel Inverter Using an Artificial Neural Network Approach," *Electrical Engineering & Electromechanics*, no. 1, pp. 31-39, 2023. [CrossRef]
[26] K. Suresh, and E. Parimalasundar, "IPWM Based IBMSC Dc-Ac Converter Using Solar Power for Wide Voltage Conversion System," *IEEE Canadian Journal of Electrical and Computer Engineering*, vol. 45, no. 4, pp. 394-400, 2022. [CrossRef]
[27] Sindhuja R et al., "Comparison between Symmetrical and Asymmetrical 13 Level Mli with Minimal Switches," *2022 International Conference on Automation, Computing and Renewable Systems*, pp. 187-191, 2022. [CrossRef]
[28] Yannam Ravi Sankar, K. Chandra Sekhar, "Hybrid Energy System for Smart Dc Microgrid Using Optimized Pi-Based Cuk Integrated Boost Dc-Dc Converter," *SSRG International Journal of Electrical and Electronics Engineering*, vol. 10, no. 1, pp. 1-14, 2023. [CrossRef]
[29] M. F. Kangarlu, and E. Babaei, "Cross-Switched Multilevel Inverter: An Innovative Topology," IET Power Electronics, vol. 6, no. 4, pp. 642–651, 2013. [CrossRef]
[30] K. Suresh, and E. Parimalasundar, "Design and Implementation of Universal Converter," *IEEE Canadian Journal of Electrical and Computer Engineering*, vol. 45, no. 3, pp. 272-278, 2022. [CrossRef]
[31] Sindhuja R et al., "A Reconfigurable Multilevel Inverters with Minimal Switches for Battery Charging and Renewable Energy Applications," *2022 6th International Conference on Electronics, Communication and Aerospace Technology*, pp. 422-427, 2022. [CrossRef]