SSRG International Journal of Electrical and Electronics Engineering
ISSN: 2348-8379/ https://doi.org/10.14445/23488379/IJEEE-V10I8P103

Volume 10 Issue 8, 23-36, August 2023

Original Article

A New Multilevel Inverter Topology for Symmetrical and Asymmetrical Configuration

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Received: 03 June 2023 Revised: 07 July 2023 Accepted: 05 August 2023 Published: 31 August 2023

Abstract - *Inverters with innovative modular symmetrical and asymmetrical topologies were introduced in this study. Either an isolated DC source, an additive or subtractive combination with other DC sources is used to produce the multilevel output. This study presents a novel approach (an alternate quinary sequence) for selecting magnitude input dc voltage sources. Phase Opposition Disposition (POD) pulse width modulation approach is used for pulse generation to the suggested topology. Regarding cost function, switch count and DC source count, the suggested topology performs better than a few current topologies. Switching states were derived to develop 5-Level, 9-Level, and 49-Level suggested topology. The proposed topology's validity is verified by simulation, and the prototype was developed for nine-level output voltage.*

Keywords - *Modeling of switching pulses, POD technique, Symmetrical and asymmetrical multilevel inverter, Selection of DC sources.*

1. Introduction

Environmental degradation and depletion of fossil fuels led to Renewable Energy Sources (RES). There are many RES solar, wind, biomass, and hydro. The future's most crucial energy generation option is Distributed Generation (DG), formed with RES. Photovoltaic (PV) is the primary means of producing electricity from RES. The growth of Distributed Generation (DG) systems increases the interest in Multilevel Inverters (MLI). In MLI desired output voltage is achieved with a different arrangement of semiconductor switches from several levels of input DC voltages to get a stepped waveform with less dv/dt and low harmonic distortions. With increased levels, the output wave is smooth-stepped. The increased levels complicate the circuit design and controlling process. DC voltage sources to which the switches are connected incur a voltage burden on the switches of MLI. Conventional MLIs are

1. Neutral point clamped MLI [1]
2. Flying capacitor MLI [2]
3. Cascaded H-bridge MLI [2, 3]

However, in multilevel inverters, no specific topology is recommended to be advantageous in all cases. The choice depends mainly on the application. Therefore, the optimal selection is necessary on a case-to-case basis. It paves the way for researchers to evolve newer topologies, switching techniques, and controlling strategies of inverters. Two types of classification in multilevel inverters based on DC voltage sources are symmetrical and asymmetrical configuration [4]. Many inverter topologies evolve with less switch count and different control techniques [5, 6]. The MLI in [7] has multipart with similar functionalities and specifications.

An H-bridge was added for the proposed topology for generating zero and negative levels. In [8] proposed, a 13-level generated structure consisting of two capacitors, two DC sources, and a proper arrangement of semiconductor switches was presented; the benefit of this construction is that no extra circuit is required for capacitor charging. In [9], a topology was proposed, and the favourable characteristics for cross-switched and T-type MLI have been carried over into the proposed topology. Due to this hybridization, the HT-type MLI can produce greater voltage levels using fewer components and less overall voltage stress.

In [10], a new topology is reported and, in extension, was realized with novelty being the DC source is cascaded to increase output voltage levels with less standing voltage on switches. A new topology [11] proposed does not require an H-bridge for negative output voltage generation for Asymmetrical configuration. In [12], the symmetrical configuration is discussed with DC sources and is connected alternatively in opposite polarities along switches to get the required output voltage levels. A novel topology with

bidirectional switches is proposed [13] with asymmetric DC sources. In [14], a Single DC source is used. The number of capacitors is connected in a circuit, so the capacitors will charge stage by stage to get the output voltage.

In [15], a new technique was proposed to keep power production ratios for each DC source at their predicted levels. In [16], a half-bridge was combined with cascaded H-bridges to improve output voltage levels. Output voltage almost doubles compared to conventional cascaded H-bridge.

In [17], a new topology was introduced for generating levels, and H-bridge is connected for polarity generation. In [18], a new topology was introduced with minimum switches. It has superior performance compared with many topologies.

In [19], a new topology to synthesize the sinusoidal output voltage was proposed, where each elementary part is a combination of H and half bridges to isolate the equally dc voltage sources and bidirectional auxiliary circuits. A topology [23] proposed a back-to-back connection of switches in a T-shape called a Square T (ST type) module. Generating higher voltage output levels, the modules can be readily joined to one another in a cascade connection.

In [25], the unique voltage source and single impedance network used in the suggested inverter allow for voltage increase. As a potential divider, a series of interconnected capacitors is employed across the input. By utilizing a self-voltage balance circuit, an equal voltage is kept across all capacitors without the use of a feedback circuit.

A new asymmetrical MLI topology is proposed with a reduced switch count. A fault-tolerant multilevel inverter for improved power quality and reduced switch base has been proposed in [26], the switching angles for improving power quality are obtained from the TLBO algorithm, and it is examined for levels 3, 5, 7, 9, and 11. It has been found that as levels rise, THD decreases, and the M-MLI configuration performs flawlessly even under problematic circumstances. The presented basic topology with the extension of cascaded and nested loop structures in [27] obtains more levels with less switch count. Mathematical modelling to generate switching pulses based on Phase Opposition Disposition Sinusoidal Pulse Width Modulation technique is derived to several levels.

The main contribution of this paper is

1. MLI topology with minimum switches was proposed.
2. An algorithm to select values for DC voltage sources was proposed.
3. Regarding cost function, switch count and DC source count, concerning the number of levels, a relative comparison is made.

The arrangement of the paper is as follows: In section II, a new topology is proposed and shown. In section III, a novel algorithm is proposed for choosing the value of DC. Section IV presents a Phase opposition disposition technique to generate switch modulation signals. The calculations regarding blocking voltages on switches are in section V. Suggested topology is compared with some topologies in Section VI. Section VII, Simulation and hardware results, were presented. Finally, Section VIII gives a conclusion.

2. Proposed Topology

The proposed topology is illustrated in Figure 1. Each module comprises an elementary unit with two DC voltage sources, four unidirectional switches (S11, S'11, S'12 and S1A), and one bidirectional switch (S12). The unidirectional and bidirectional switches are insulated gate bipolar transistors (IGBT). The elementary unit generates level, and an H-bridge with four unidirectional switches (SA, SB, SC and SD), generates polarity in the output voltage. In the elementary unit, power switches S11, S'11 and, S1A, S'12 should not turn on to eliminate short circuit paths over DC sources Vdc1 and Vdc2, respectively. Table 1 depicts switching states for the proposed MLI. The use of switches in the suggested topology is determined by the algorithm used and the output voltage level required. Each polar level has the same amount of conducting switches and is self-balanced. As demonstrated in Figure 2, output voltage levels were raised by connecting 'n' no.of elementary units in series.

The desired switch count for this arrangement is given by

$$N_S = 4 + 6n \tag{1}$$

n=1,2,3.....no.of cascaded elementary units.

The number of DC sources required are

$$N_{DC} = 2n \tag{2}$$

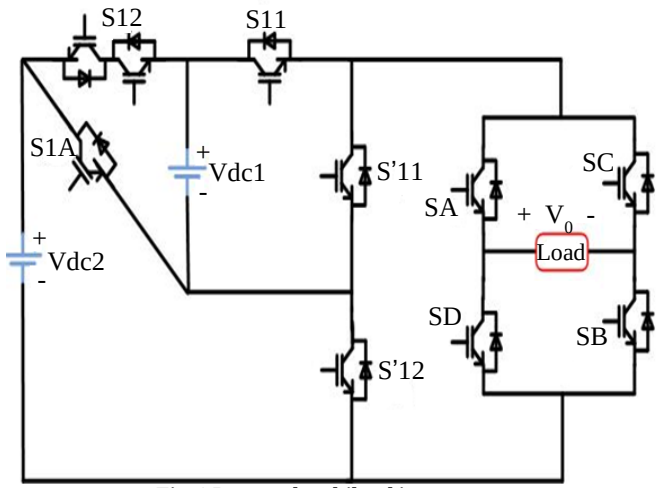

Fig. 1 Proposed multilevel inverter

Table 1. Switching states for proposed topology

Output Voltage (Vo)	+Vo/-Vo Switching States
0	S'_{11},S'_{12},S_A,S_B (or) S_A, S_C (or) S_B, S_D (or) S'_{11},S'_{12},S_C,S_D
+/- Vdc1	S_{11},S_A,S_B, S'_{12} / S_{11},S_C,S_D,S'_{12}
+/- Vdc2	S_{1A}, S'_{11},S_A,S_B (or) S_{12},S_{11},S_A,S_B / S_{1A}, S'_{11},S_C,S_D (or) S_{12},S_{11},S_C,S_D
+/-(Vdc2-Vcd1)	S_{12},S'_{11},S_A,S_B / S_{12},S'_{11},S_C,S_D
+/-(Vdc2+Vcd1)	S_{1A},S_{11},S_A,S_B / S_{1A},S_{11},S_C,S_D

3. Magnitudes of DC Sources Determination Algorithm

Various approaches for determining magnitude at DC sources for both asymmetrical and symmetrical topologies are explored in this section. In a symmetrical design, all DC sources have the same value, but in an asymmetrical configuration, all DC sources have different values. Output voltage levels in asymmetrical design can be enhanced using the same number of DC sources and switches as in symmetrical configuration [20].

3.1. Symmetrical Configuration

DC source values in symmetrical configuration are selected based on an unary algorithm.

Unary algorithm: (ratio of DC sources 1:1:1….)

DC source values magnitude is determined as

$$V_{dci} = V_{dc}\ ;\ i = 1,2,3 \dots k \tag{3}$$

'k' represents the DC sources count. The output voltage maximum value from the suggested topology with the unary algorithm is

$$V_{omax} = \sum_{i=1}^{k} V_{dc\,i} = k \times V_{dc}\ ; k = 2,4,6 \tag{4}$$

Levels count in the output voltage is

$$N_L = 2 \times \left(\frac{V_{omax}}{V_{dc}}\right) + 1 = (2 + k) + 1 \tag{5}$$

For the proposed topology with one elementary unit. Output voltage switching states are depicted in Table 2. The output voltage 0, +/-(1Vdc) has redundant states. Multiple switching states may exist for these two voltage levels at the output.

3.2. Asymmetrical Configuration

The magnitude of DC sources for the proposed topology can also be selected based on existing Asymmetrical algorithms, which are represented as case 1 and case 2.

Case 1: Natural sequence algorithm: (ratio of DC sources is 1:2:3:4...)

DC source voltage magnitudes are determined as

$$V_{dci} = i \times V_{dc}; i = 1,2,3 \dots . k \tag{6}$$

The maximum output voltage from the circuit with a natural sequence algorithm is

$$V_{omax} = \sum_{i=1}^{k} V_{dci} = \left(\frac{k \times (k+1)}{2}\right) \times V_{dc} \tag{7}$$

Levels count in output voltage is

$$N_L = 2 \times \left(\frac{V_{omax}}{V_{dc}}\right) + 1 = k \times (k+1) + 1 \tag{8}$$

In an Asymmetrical configuration, if DC source values are in natural sequence with two elementary units shown in Figure 2. It generates 21 levels in the output voltage.

Case 2: Binary sequence algorithm:(ratio of DC sources 1:2:4:8...).

Magnitude for DC voltage source values was determined as

$$V_{dci} = 2^{(i-1)} \times V_{dc}; i = 1,2,3 \dots . k \tag{9}$$

Maximum output voltage from the circuit with binary sequence algorithm as

$$V_{omax} = \sum_{i=1}^{k} V_{dci} = \left(2^k - 1\right) \times V_{dc} \tag{10}$$

Levels count in output voltage is

$$N_L = 2 \times \left(\frac{V_{omax}}{V_{dc}}\right) + 1 = 2^{(k+1)} - 1 \tag{11}$$

If DC source values are in binary sequence with two elementary units for asymmetrical configuration, 31 levels will appear in the output voltage.

Case 3: Alternative Quinary Sequence:(ratio of DC sources is 1:3:5:15:25:75:125)

This paper proposes a novel Alternative Quinary Sequence algorithm to determine the magnitude of DC sources. Magnitude of DC source values is determined as

$$V_{dcj} = 5^{(i-1)} \times V_{dc}, j = 1,3,5 \ldots \& \, i = 1,2,3 \ldots \quad (12)$$

$$V_{dcj} = 3 \times 5^{(i-1)} \times V_{dc}, \; j = 1,3,5 \ldots \& \; i = 1,2,3 \ldots \quad (13)$$

Maximum output voltage from the proposed topology with natural sequence algorithm as

$$V_{omax} = \sum_{i=1}^{k} V_{dci} = \left(5^{\left(\frac{k}{2}\right)} - 1\right) \times V_{dc} \quad (14)$$

Levels count in the output voltage is

$$N_L = 2 \times \left(\frac{V_{omax}}{V_{dc}}\right) + 1 = \left(2 \times 5^{\left(\frac{k}{2}\right)} - 1\right) \quad (15)$$

Figure 1 shows the circuit that can generate 9-levels with the proposed algorithm (Alternative Quinary Sequence). Table 3 depicts the switching states to get output voltage as 9-level. With suggested algorithm for the circuit shown in Figure 2 gives a 49-level output voltage.

Table 4 shows the switching states of the 49-level output voltage. The proposed Alternative quinary sequence gives the highest output voltage levels than existing unitary, natural and binary sequences. Compared to the natural sequence, the proposed algorithm enhances the number of levels in output voltage to 28 levels.

In contrast, the proposed algorithm enhances output voltage to 18 levels compared to the binary sequence. More elementary units have to be cascaded to increase the output voltage, as shown in Figure 2.

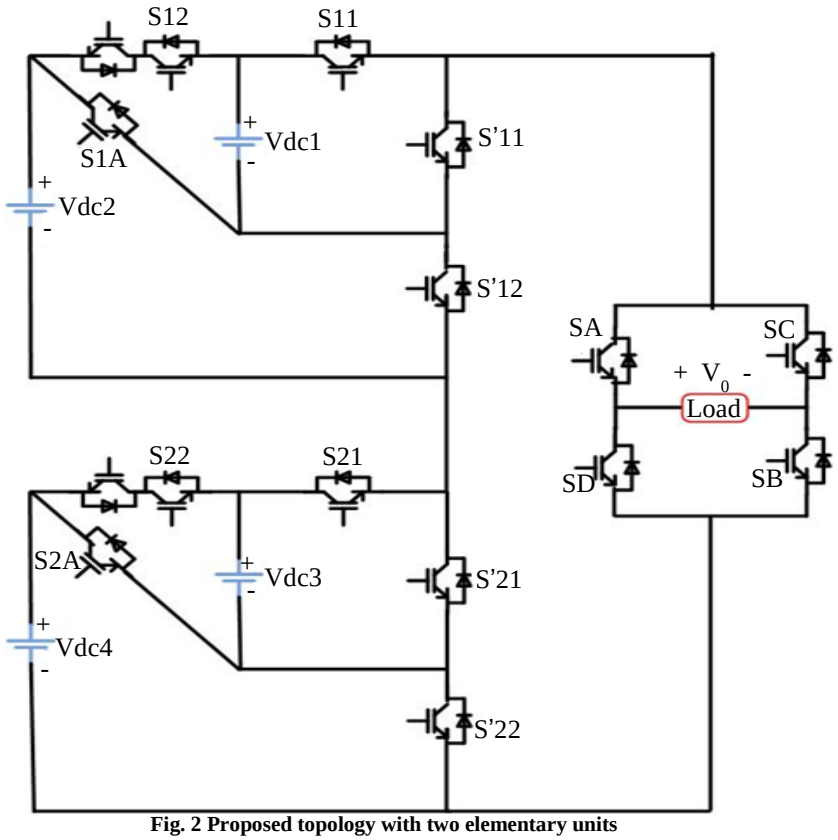

Fig. 2 Proposed topology with two elementary units

4. Modulation Techniques

The modulation techniques used to regulate the inverter are primarily responsible for the harmonic reduction in MLI. For the carrier arrangements, a sinusoidal pulse width modulation approach based on the POD strategy is used to create gating signals for the proposed topology. All carriers above zero reference using POD have the same frequency and peak-to-peak amplitude and are 180^0 out of phase for carriers below zero reference. Creating pulses to N-level inverter requires (N-1) carriers and are equally spread above and below the reference to generate pulses as depicted in Figure 3. For the (N-1)/2 carrier signals to generate positive

pulses a_1, a_2,...., $a_{(N-1)/2}$, they should be compared with reference sine wave positive half cycle. Negative pulses a_{-1}, a_{-2},..., $a_{-(N-1)/2}$ are obtained by comparing the remaining (N-1)/2 carrier signals below reference along the negative half cycle of reference (sine) wave.

For the suggested topology shown in Figure 1, corresponding switching pulses are as follows [21, 26].

$$S_{11p} = a_1 - a_2 + a_3 - a_5 \quad (16)$$

$$S_{12p} = a_2 - a_4 \quad (17)$$

$$S'_{11p} = a_2 - a_3 \quad (18)$$

$$S'_{12p} = a_1 - a_2 \quad (19)$$

$$S_{1Ap} = a_4 \quad (20)$$

$$S_A = S_B = a_1 \quad (21)$$

$$S_C = S_D = a_{-1} \quad (22)$$

The eq's (16) to (20) are the elementary topology switches that generate levels. The eq's (21) and (22) are the H-bridge switches to generate polarity in output voltage.

Mathematical modeling of switches for a 49-level inverter in Figure 2 is derived as follows [26].

$$S_{11p} = \sum_{n=1}^{\infty}\left(a_{1+(n-1)\times 5} - a_{2+(n-1)\times 5}\right) + \left(a_{3+(n-1)\times 5} - a_{5+(n-1)\times 5}\right) \quad (23)$$

$$S_{12p} = \sum_{n=1}^{\infty}\left(a_{2+(n-1)\times 5} - a_{4+(n-1)\times 5}\right) \quad (24)$$

$$S_{21p} = \sum_{n=1}^{\infty}\left(a_{5+(n-1)\times 25} - a_{5+(n-1)\times 25}\right) + \left(a_{15+(n-1)\times 25} a_{25+(n-1)\times 25}\right) \quad (25)$$

$$S_{22p} = \sum_{n=1}^{\infty}\left(\left(a_{10+(n-1)\times 25} - a_{10+(n-1)\times 25}\right)\right) \quad (26)$$

$$S'_{11p} = \sum_{n=1}^{\infty}\left(a_{2+(n-1)\times 5} - a_{3+(n-1)\times 5}\right) + \left(a_{5+(n-1)\times 5} - a_{6+(n-1)\times 5}\right) \quad (27)$$

$$S'_{12p} = \sum_{n=1}^{\infty}\left(a_{1+(n-1)\times 5} - a_{2+(n-1)\times 5}\right) \quad (28)$$

$$S'_{21p} = \sum_{n=1}^{\infty}\left(a_{1+(n-1)\times 25} - a_{2+(n-1)\times 25}\right) + \left(a_{10+(n-1)\times 25} - a_{25+(n-1)\times 25}\right) \quad (29)$$

$$S'_{22p} = \sum_{n=1}^{\infty}\left(a_{1+(n-1)\times 25} - a_{10+(n-1)\times 25}\right) \quad (30)$$

$$S_{1Ap} = \sum_{n=1}^{\infty}\left(a_{4+(n-1)\times 5} - a_{5+(n-1)\times 5}\right) \quad (31)$$

$$S_{2Ap} = \sum_{n=1}^{\infty}\left(a_{20+(n-1)\times 25} - a_{25+(n-1)\times 25}\right) \quad (32)$$

$$S_A = S_B = a_1 \quad (33)$$

The eq's (23) to (32) represent positive pulses for the switches. They are represented with 'p' in the suffix for clear indication. Negative pulses for the switches can be obtained by using eq(34)

$$S_{11n} = S_{11p} \times a_{-1} \quad (34)$$

$$S_C = S_D = a_{-1} \quad (35)$$

The switching pulse is obtained from eq (35) for SC and SD switches. The negative pulses for the switches are obtained by considering the condition in eq (36).

$$a_m \times a_{-1} = a_{-m} \quad (36)$$

Combination of Positive and Negative pulses for switches yields gating pulses to each switch, as shown in eq (37).

$$S_{11} = S_{11p} + S_{11n} \quad (37)$$

Similarly, the gating pulses were obtained for all the switches except SA, SB, SC and SD, as shown in eq (37). For S_A, S_B, S_C and S_D gating pulses are shown in eq's (33) & (35), respectively.

Table 2. 5-Level output voltage symmetrical configuration switching states

Output Voltage (Vo)	+Vo/-Vo Switching States
0	S'_{11},S'_{12},S_A,S_B (or)S'_{12},S_{1A},S_{12},S_{11} ,S_A,S_B(or) S_A, S_C (or) S_B, S_D (or) S'_{11},S'_{12},S_C,S_D
+/- 1Vdc	S_{11},S_A,S_B, S'_{12} (or) S_{11}, S_{12} , S_A,S_B (or) S_{1A},S'_{11},S_A,S_B/ S_{11},S_C,S_D,S'_{12} (or) S_{11}, S_{12} , S_C,S_D (or) S_{1A},S'_{11},S_C,S_D
+/- 2Vdc	S_{1A},S_{11},S_A,S_B / S_{1A},S_{11},S_C,S_D

Table 3. 9-Level output voltage of proposed algorithm switching states

Output Voltage(Vo)	+Vo/-Vo Switching States
0	S'_{11},S'_{12},S_A,S_B (or) $S'_{12},S_{1A},S_{12},S_{11},S_A,S_B$ (or) S_A, S_C (or) S_B, S_D (or) S'_{11},S'_{12},S_C,S_D
+/- 1Vdc	S_{11},S_A,S_B, S'_{12} / S_{11},S_C,S_D,S'_{12}
+/- 2Vdc	S_{12},S'_{11},S_A,S_B / S_{12},S'_{11},S_C,S_D
+/- 3Vdc	S_{1A}, S'_{11},S_A,S_B (or) S_{12},S_{11},S_A,S_B / S_{1A}, S'_{11},S_C,S_D (or) S_{12},S_{11},S_C,S_D
+/- 4Vdc	S_{1A},S_{11},S_A,S_B / S_{1A},S_{11},S_C,S_D

Table 4. 49-Level output voltage of proposed algorithm switching state

Output Voltage(Vo)	+Vo/-Vo Voltage switching states
0	S'_{11},S'_{12},S_A,S_B (or) S_A, S_B (or) S_C, S_D (or) S'_{11},S'_{12},S_C,S_D
+/-(1Vdc)	S_{11},S_A,S_B, S'_{12} / S_{11},S_C,S_D,S'_{12}
+/-(2Vdc)	S_{12},S'_{11},S_A,S_B / S_{12},S'_{11},S_C,S_D
+/-(3Vdc)	S_{1A}, S'_{11},S_A,S_B (or) S_{12},S_{11},S_A,S_B / S_{1A}, S'_{11},S_C,S_D (or) S_{12},S_{11},S_C,S_D
+/-(4Vdc)	S_{1A},S_{11},S_A,S_B / S_{1A},S_{11},S_C,S_D
+/-(5Vdc)	$S_{21},S'_{12},S'_{11},S_A,S_B,S'_{22}$ / $S_{21},S'_{12},S'_{11},S_C,S_D,S'_{22}$
+/-(6Vdc)	$S_{21},S'_{12},S_{11},S_A,S_B,S'_{22}$ / $S_{21},S'_{12},S_{11},S_C,S_D,S'_{22}$
+/-(7Vdc)	$S_{21},S_{12},S'_{11},S_A,S_B,S'_{22}$ / $S_{21},S_{12},S'_{11},S_C,S_D,S'_{22}$
+/-(8Vdc)	$S_{21},S_{12},S_{11},S_A,S_B,S'_{22}$ (or) $S_{21},S_{1A},S'_{11},S_A,S_B,S'_{22}$ / $S_{21},S_{12},S_{11},S_C,S_D,S'_{22}$ (or) $S_{21},S_{1A},S'_{11},S_C,S_D,S'_{22}$
+/-(9Vdc)	$S_{21},S_{1A},S_{11},S_A,S_B,S'_{22}$ / $S_{21},S_{1A},S_{11},S_C,S_D,S'_{22}$
+/-(10Vdc)	$S_{22},S'_{21},S'_{12},S'_{11},S_A,S_B,S'_{22}$ / $S_{22},S'_{21},S'_{12},S'_{11},S_C,S_D,S'_{22}$
+/-(11Vdc)	$S_{22},S'_{21},S'_{12},S_{11},S_A,S_B,S'_{22}$ / $S_{22},S'_{21},S'_{12},S_{11},S_C,S_D,S'_{22}$
+/-(12Vdc)	$S_{22},S'_{21},S_{12},S'_{11},S_A,S_B,S'_{22}$ / $S_{22},S'_{21},S_{12},S'_{11},S_C,S_D,S'_{22}$
+/-(13Vdc)	$S_{22},S'_{21},S_{12},S_{11},S_A,S_B,S'_{22}$ (or) $S_{22},S'_{21},S_{1A},S'_{11},S_A,S_B,S'_{22}$ / $S_{22},S'_{21},S_{12},S'_{11},S_C,S_D,S'_{22}$ (or) $S_{22},S'_{21},S_{1A},S'_{11},S_A,S_B,S'_{22}$
+/-(14Vdc)	$S_{22},S'_{21},S_{1A},S_{11},S_A,S_B,S'_{22}$/ $S_{22},S'_{21},S_{1A},S_{11},S_C,S_D,S'_{22}$
+/-(15Vdc)	$S_{22},S_{21},S'_{12},S'_{11},S_A,S_B,S'_{22}$ (or) $S_{2A},S'_{21},S'_{12},S'_{11},S_A,S_B,S'_{22}$ / $S_{22},S_{21},S'_{12},S'_{11},S_C,S_D,S'_{22}$ (or) $S_{2A},S'_{21},S'_{12},S'_{11},S_C,S_D,S'_{22}$
+/-(16Vdc)	$S_{22},S_{21},S'_{12},S_{11},S_A,S_B,S'_{22}$ (or) $S_{2A},S'_{21},S'_{12},S_{11},S_A,S_B,S'_{22}$ / $S_{22},S_{21},S'_{12},S_{11},S_C,S_D,S'_{22}$ (or) $S_{2A},S'_{21},S'_{12},S_{11},S_C,S_D,S'_{22}$
+/-(17Vdc)	$S_{22},S_{21},S_{12},S'_{11},S_A,S_B,S'_{22}$ (or) $S_{2A},S'_{21},S_{12},S'_{11},S_A,S_B,S'_{22}$ / $S_{22},S_{21},S_{12},S'_{11},S_C,S_D,S'_{22}$ (or) $S_{2A},S'_{21},S_{12},S'_{11},S_C,S_D,S'_{22}$
+/-(18Vdc)	$S_{22},S_{21},S_{12},S_{11},S_A,S_B,S'_{22}$ (or) $S_{2A},S'_{21},S_{1A},S'_{11},S_A,S_B,S'_{22}$ / $S_{22},S_{21},S_{12},S_{11},S_C,S_D,S'_{22}$ (or) $S_{2A},S'_{21},S_{1A},S'_{11},S_C,S_D,S'_{22}$
+/-(19Vdc)	$S_{22},S_{21},S_{1A},S_{11},S_A,S_B,S'_{22}$ (or) $S_{2A},S'_{21},S_{1A},S_{11},S_A,S_B,S'_{22}$ /$S_{22},S_{21},S_{1A},S_{11},S_C,S_D,S'_{22}$ (or) $S_{2A},S'_{21},S_{1A},S_{11},S_C,S_D,S'_{22}$
+/-(20Vdc)	$S_{2A},S_{21},S'_{12},S'_{11},S_A,S_B,S'_2$/ $S_{2A},S_{21},S'_{12},S'_{11},S_C,S_D,S'_{22}$
+/-(21Vdc)	$S_{2A},S_{21},S'_{12},S_{11},S_A,S_B,S'_{22}$ / $S_{2A},S_{21},S'_{12},S_{11},S_C,S_D,S'_{22}$
+/-(22Vdc)	$S_{2A},S_{21},S_{12},S'_{11},S_A,S_B,S'_{22}$ / $S_{2A},S_{21},S_{12},S'_{11},S_C,S_D,S'_{22}$
+/-(23Vdc)	$S_{2A},S_{21},S_{12},S_{11},S_A,S_B,S'_{22}$ / $S_{2A},S_{21},S_{12},S_{11},S_C,S_D,S'_{22}$
+/-(24Vdc)	$S_{2A},S_{21},S_{1A},S_{11},S_A,S_B,S'_{22}$ / $S_{2A},S_{21},S_{12},S_{11},S_C,S_D,S'_{22}$

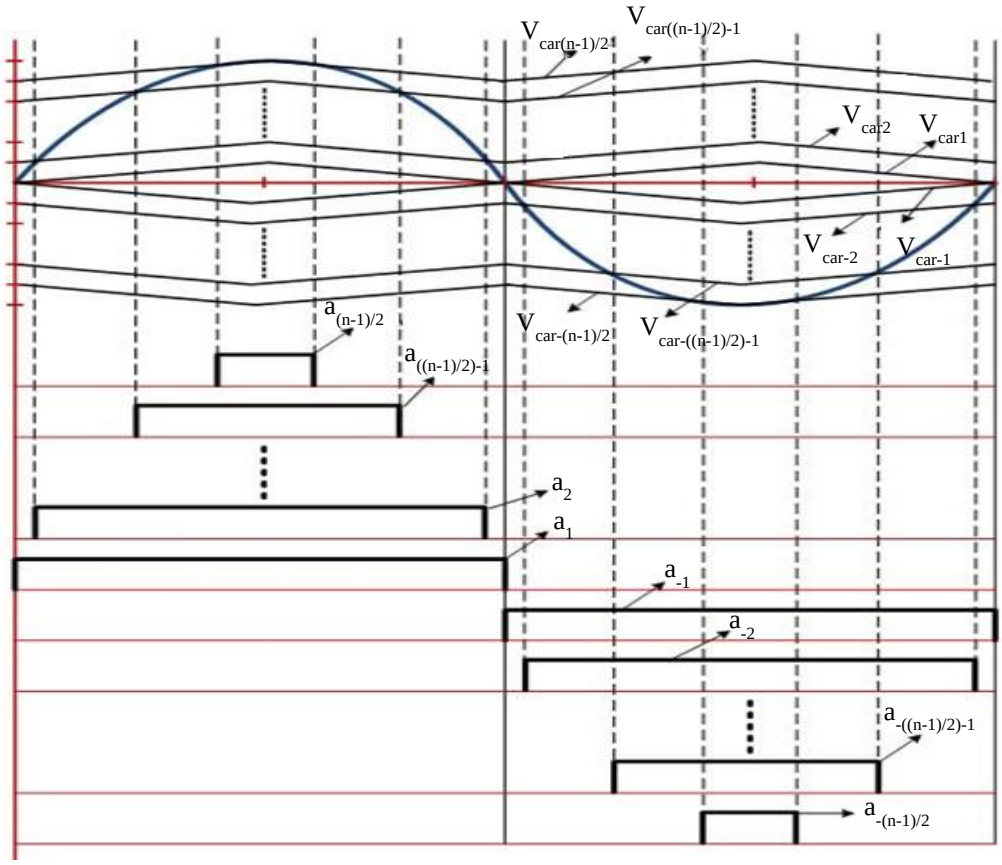

Fig. 3 Pulse generation using sinusoidal pulse width phase opposition disposition (SPWMPOD) technique

5. Calculation of Blocking Voltages on the Switches

Blocking voltages on the switches are the main factor in deciding the switch's rating. It also influences inverter cost [17]. The different switching states of the switches lead to different blocking voltages across them, depending on the DC voltage source value. According to Figure 1, blocking switch voltages are obtained as follows.

$$VS_{n1} = VS'_{n1} = Vdc_1 \tag{38}$$

$$VS_{n2} = VS'_{n1} = V_{dc1} \tag{39}$$

$$VS'_{n2} = VS_{nA} = V_{dc2} \tag{40}$$

$$\mathrm{VS_A} = \mathrm{VS_B} = \mathrm{VS_C} = \mathrm{VS_D} = \mathrm{V_{omax}} \tag{41}$$

Vomax is the maximum generated amplitude of output voltage by the inverter. In the suggested topology total blocking voltage across all switches, $V_{block,}$ is given as

$$V_{block} = \sum_{n=1}^{\infty}(VS_{n1} + VS_{n2} + VS'_{n1} + VS_{nA}) + (VS_A + VS_B + VS_C + VS_D) \tag{42}$$

6. Comparisons

The main aim of multilevel inverters is to raise the levels count in the output voltage with less cost[24]. The cost can be reduced by reducing the devices and DC sources count. The quantity of needed driver circuits is reduced as the count of switches is reduced, reducing the inverter's connection complexity. In this section, a comparison of suggested topology was made with some existing topologies [10][17][19][23] in terms of levels count vs DC sources count, levels count vs switches count, and levels count vs cost function.

Figure 4 and Figure 5 represent levels count vs sources count and levels count vs switches count, respectively. Table 5 shows the relations considered to plot graphs. The proposed topology considered an Alternative Quinary sequence algorithm (case 3 in Asymmetrical configuration) to compare with existing topologies.

From Figure 4, the suggested topology shows the best performance in terms of DC sources comparison with some existing topologies to generate a particular output level. In Figure 5, the suggested topology shows that it requires fewer switches count than the other presented topologies to generate particular output levels.

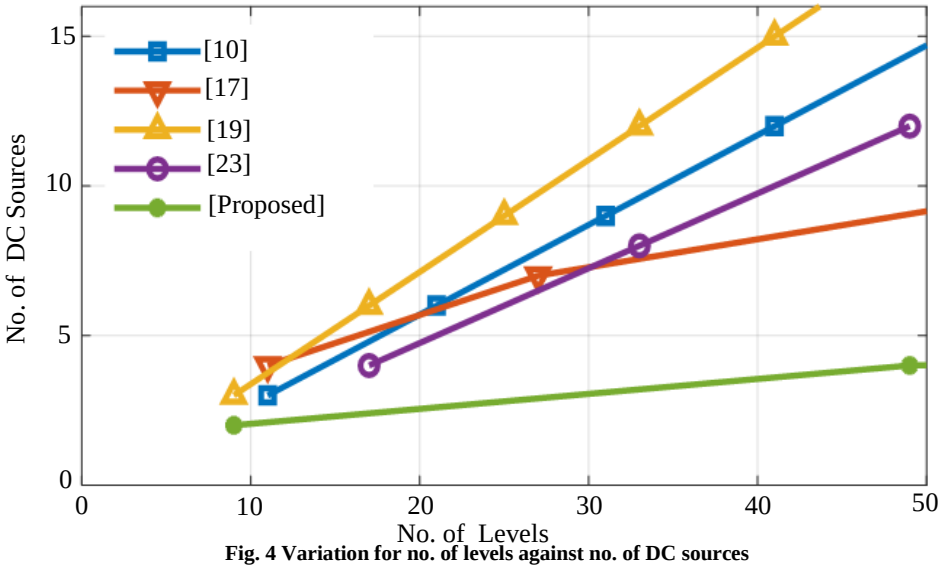

Fig. 4 Variation for no. of levels against no. of DC sources

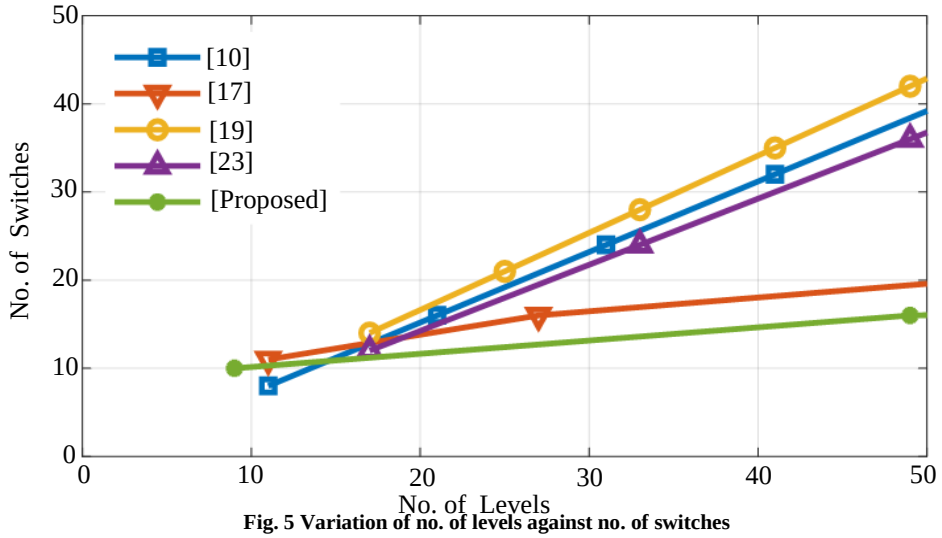

Fig. 5 Variation of no. of levels against no. of switches

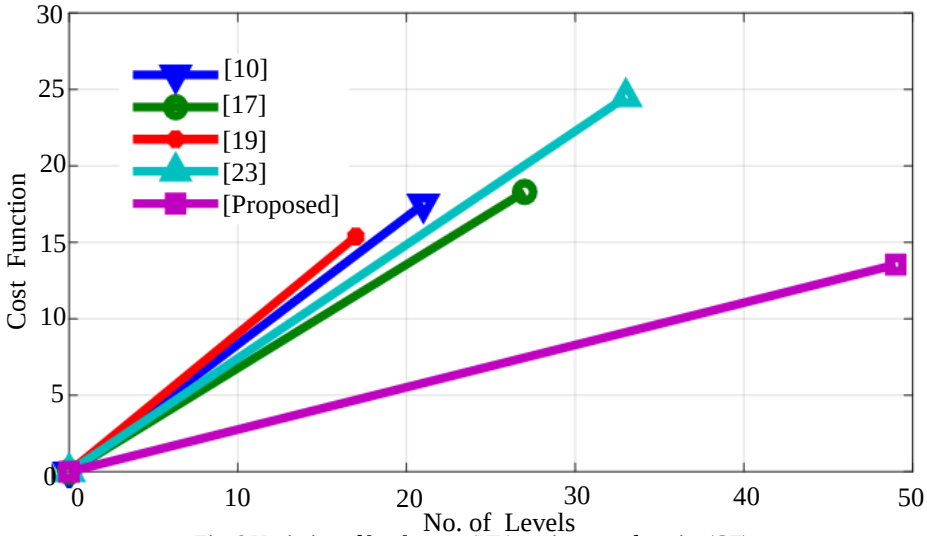

Fig. 6 Variation of level count (NL) against cost function(CF)

The overall cost estimation is given by cost function (CF). It can be defined as follows [22]

$$CF = N_{IGBT's} + \alpha V_{Block}^{P..U} = N_{IGBT's} + \alpha \left(\frac{V_{Block}}{V_{omax}}\right) \quad (43)$$

In eq (43), 'α' is a significant (weight) factor for the blocked voltage of switches against the count of IGBTs. The value of blocked voltages will be crucial if the 'α' value is more than one; if 'α' is lower than one, the count of IGBTs and their cost is crucial in selecting the suitable switching devices.

The cost function against the levels count in Figure 6 indicates that the suggested topology has less cost than the few presented topologies in literature when α= 0.5 and k=1. 'α' is chosen as 0.5 to prioritise the number of IGBTs in finding the cost function. From the above comparisons, the proposed topology requires less switch and DC source count; cost function decreased, and installation space is less to create specific output voltage levels.

7. Results

In this section, results are verified in MATLAB/SIMULINK software. Simulation results are validated through experimental setup. The parameters used for simulation and hardware for Figure 1 are R=40 ohms, L=55 mH.

7.1. Simulation Results

By considering a symmetrical unitary configuration for one elementary unit, as depicted in Figure 1 of the proposed system, 5-levels appear in the output voltage with the positive half having two levels negative half having two levels and 1 zero level as illustrated in Figure 7. The DC voltage source values are chosen as Vdc1 = Vdc2 = 10 Volt. Each level is 10 volts, and the maximum amplitude of the output voltage is 20 Volts.

By considering an Alternative quinary sequence with one elementary unit, 9-levels appear in the output voltage, with the positive half having four levels, the negative half having four levels, and 1 zero level as illustrated in Figure 8. The DC source values are selected as Vdc1 =10 Volt, Vdc2=30 Volt.

Each level is 10 volts with the peak value of output voltage as 40 volts. Comparing Figure 7 and Figure 8 for the same topology because of an Asymmetrical DC source, the output levels are more in Figure 8.

Cascading two elementary units, as illustrated in Figure 2, an Alternative quinary sequence algorithm is chosen to decide the values of the DC voltage source. In the simulation, DC voltage values are chosen as Vdc1=10V, Vdc2=30V, Vdc3=50V and Vdc4=150V. The output voltage Peak amplitude is 240 V, and 49 levels will appear in output voltage as illustrated in Figure 9, with a positive half cycle having 24 levels, a negative half cycle having 24 levels and 1 zero level.

The current waveform at the load is shown in Figure 10. The inductive nature of load causes phase delay in load current. Output voltage's harmonic spectrum is smaller than the 5% percent constraint set by IEEE519 standards, illustrated in Figure 11.

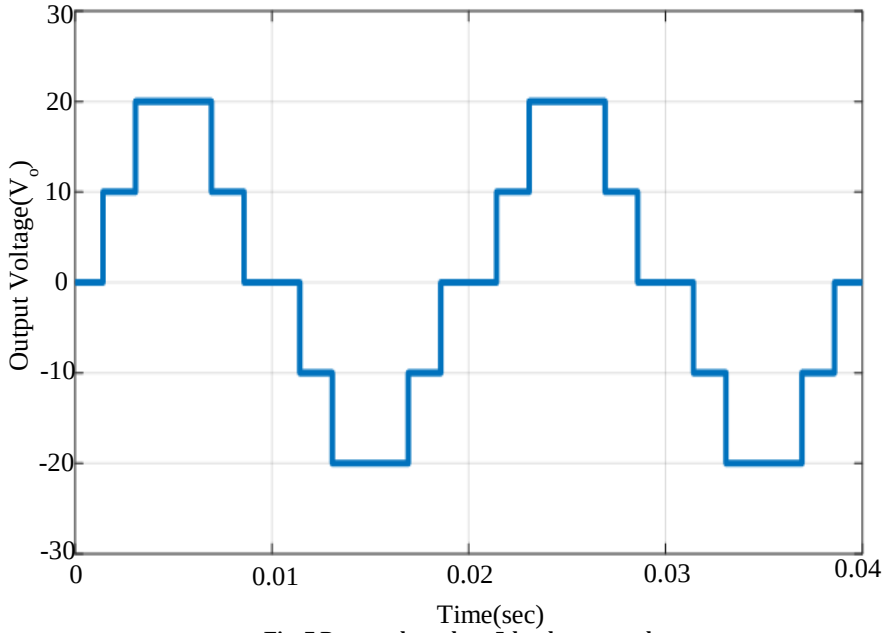

Fig. 7 Proposed topology 5-level output voltage

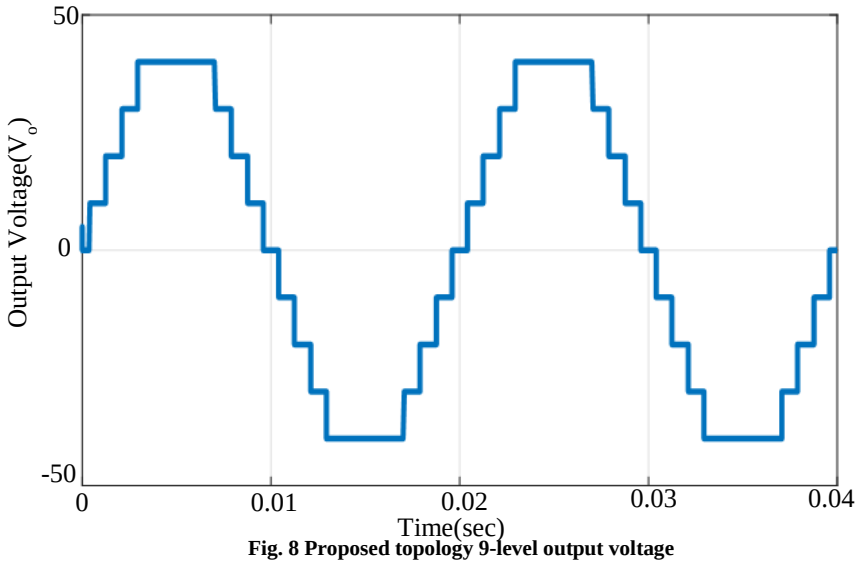

Fig. 8 Proposed topology 9-level output voltage

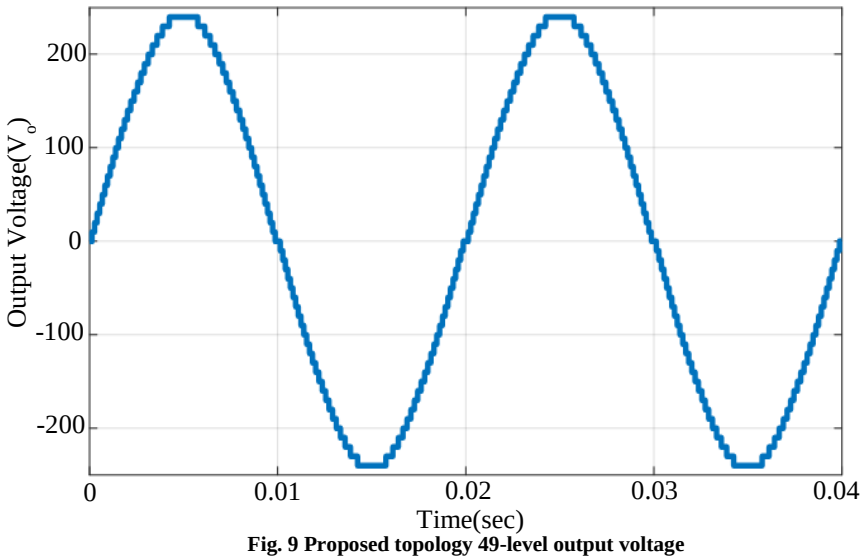

Fig. 9 Proposed topology 49-level output voltage

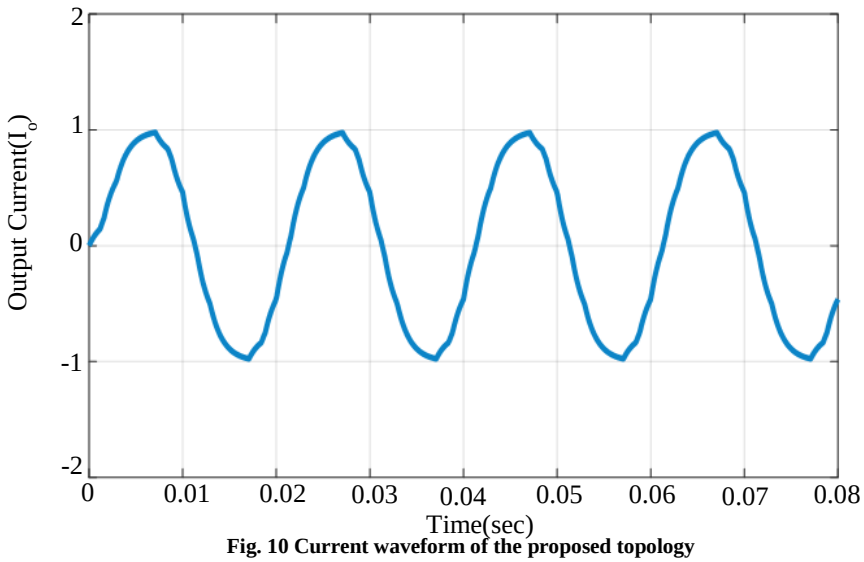

Fig. 10 Current waveform of the proposed topology

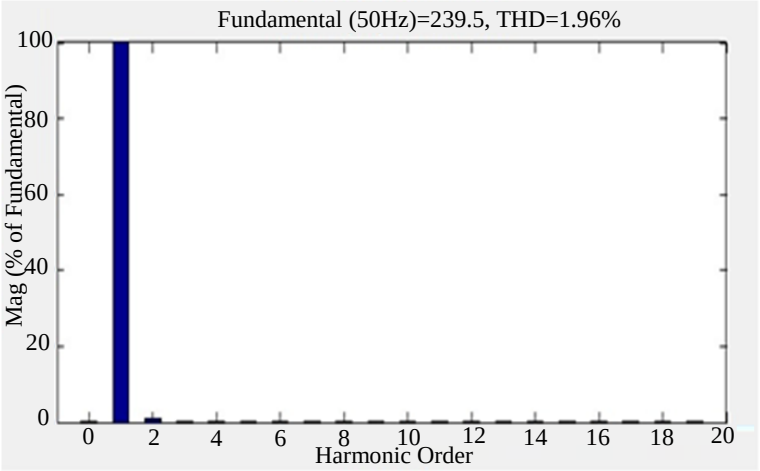

Fig. 11 FFT analysis of 49-level inverter output voltage spectrum

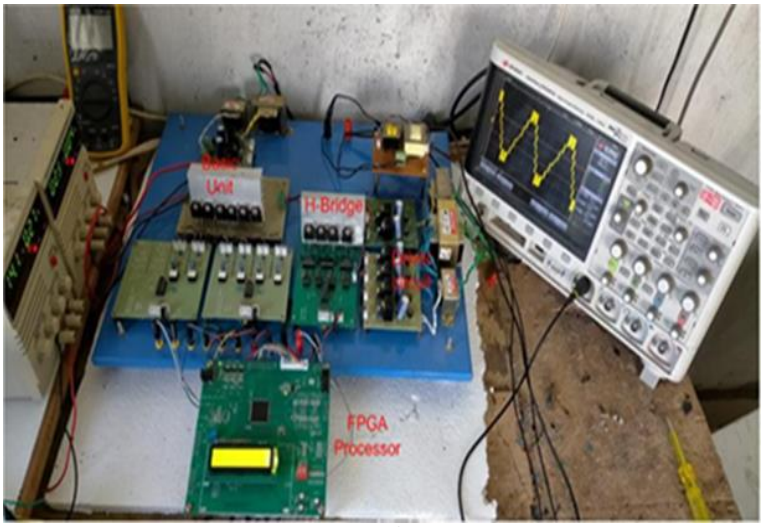

Fig. 12 Prototype of 9-level inverter

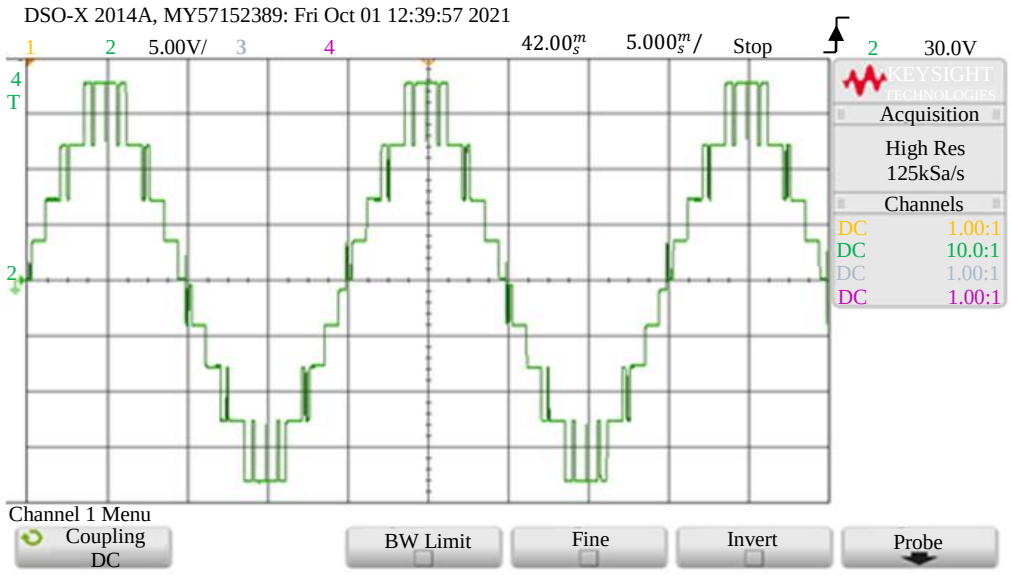

Fig. 13 Experimental voltage of 9-level inverter

7.2. Experimental Results

Figure 12 shows the experimental setup of the suggested topology to generate the 9-level output voltage. This setup was designed based on Figure 1. The experimental setup comprises power electronics switches for the elementary unit and H-bridge, gate drive circuit (TLB250) and FPGA processor. The IGBTs used in the prototype of the elementary circuit and H-bridge are (FGA25N1200).

FPGA processor SPARTAN 6 XILINX generates switching pulses to IGBTs. One proposed unit consists of four unidirectional IGBT S_{11}, S_{1A}, S'_{11}, S'_{12}, one bidirectional switch S_{12} for the elementary unit and four unidirectional IGBT'S SA, SB, SC, SD for the H-bridge. For the proposed quinary sequence algorithm, DC voltage source values are chosen as V_1 and V_2 are 5 V and 15 V, respectively.

It can create a 9-Level output voltage (positive half cycle having four levels, negative half cycle having four levels and Zero level) with an output voltage peak amplitude is 18V, illustrated in Figure 13 and Figure 14 is an output current waveform lagging concerning output voltage, experimental output current and voltage values are in good agreement along simulation results.

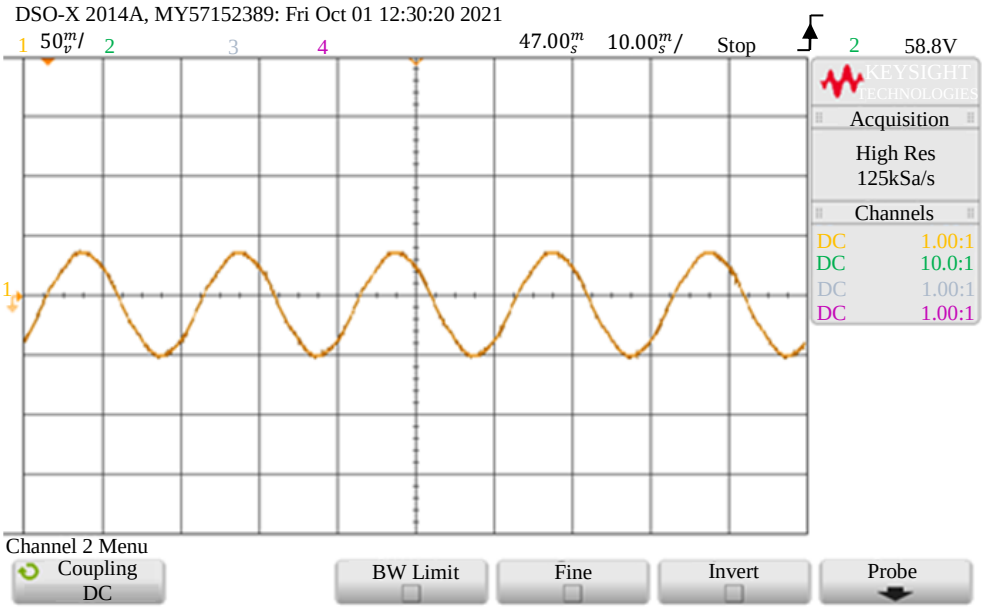

Fig. 14 Experimental current waveform

Table 5. Relations used to compare topologies

Topology	Magnitude of DC sources	N_{Level}	$N_{Switches}$	$N_{DCsources}$
[10]	$V_{a1,n}=V_{dc}$ $V_{a2,n}=Vb_{1,n}=Vb_{2,n}=Vb_{3,n}=2V_{dc}$ 'n' is number of sources	(10n+1)	8n	3n
[17]	$V_{1,j}=0.5V_{2,j}=V_{3,j}=2^{j-1}V_{dc}$ For j=1,2,----n	2^{n+3}-5	5n+6	3n+1
[19]	$V_S=V_{dc}$, $DC_i=DC_{i+1}=V_{DC}/2$ For i=1,2…	(8n/3)+1	7n/3	3n
[23]	$V_{U1}=1V_{DC}$,$V_{L1}=3V_{DC}$ V_{U2}=total number of levels in previous unit. $V_{L2}=51V_{DC}$	16n+1	12n	4n
[Proposed]	$V_{dci}=5^{(i-1)}V_{dc}$ For odd values of 'i' $V_{dci}=3*5^{(i-1)}V_{dc}$ For even values of 'i'	$2*5^n$-1	4+6n	2n

8. Conclusion

This paper proposes a new topology and an Alternative Quinary sequence algorithm to determine the magnitude of DC sources. The proposed algorithm with the proposed topology gives the best results compared to a few existing topologies regarding switches count; DC sources count concerning levels count. The cost function of the suggested topology is also low compared to a few existing topologies in the literature. Simulation results have been presented for the suggested topology in symmetrical configuration with a 5-level in output voltage, asymmetrical configuration with a 9-Level in output voltage with one elementary unit and asymmetrical configuration with a 49-level in the output voltage by cascading two elementary units.

Finally, the prototype was developed to validate simulation results and performance of topology in generating 9-level output voltage.

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