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Original Article

A Single Source Switched Capacitor Seven-Level Boost Inverter for Solar PV Applications

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Abstract *- Multilevel Inverters (MLIs) are cascade inverters that may take several or a single DC input and produce a single AC output of the desired Frequency (F) and voltage, making them ideal for medium power applications. MLIs are better than 2L inverters in many aspects; however, implementing MLIs is becoming more difficult due to the increasing amount of switches and their configurations. For high-gain DC-AC converters, Switched Capacitor (SC) driven MLIs often demonstrate the compromise between switch count and voltage rating. A Single-Source Switched Capacitor Seven-Level Boost Inverter (S^3C7LBI) is presented in this research. Since the S^3C7LBI can offer intrinsic capacitor voltage balancing, triple voltage gain, and seven output levels without requiring sensors or other auxiliary operations, it is appropriate for renewable energy applications. The proposed S^3C7L boost inverter design requires only one DC power source, eleven electronic switches, and two capacitors. Utilizing the sinusoidal PWM control approach, the functioning of the S^3C7LB inverter is examined. The usefulness of the S^3C7LBI architecture is validated by the simulation results for dynamic modulation index values, and different load conditions are presented. Additionally, hardware findings confirm that the S^3C7LBI architecture is feasible.*

Keywords *- Boost voltage, Harmonic distortion, Multilevel Inverter, Switched Capacitor, DC-AC inverter.*

1. Introduction

Increasing the switching frequency in a simple two-level inverter reduces the output voltage's harmonics, resulting in increased switching losses and voltage stresses due to reduced output voltage's step count. The drawbacks of the two-level inverter pique interest in Multilayer Inverters (MLIs). MLI was introduced in 1991, & its progress has been rapid.

MLIs are widely used in several industries today, especially for high-power and intermediate-voltage applications. MLIs produce a staircase waveform that closely resembles a sinusoidal signal and has less harmonic distortion by using more DC supply and switches. Over conventional two-level inverters, MLIs provide several advantages, including a greater primary output voltage, reduced switching loss and common mode voltage, decreased EMI, and decreased THD [1]. Because of these advantages, MLIs apply to various applications, including HVDC, FACTS, electric vehicles, and solar power systems [2]. The most common MLI topologies are the CHB inverter, Flying Capacitor (FC), and NPC inverter. FC utilizes capacitors in a ladder structure, while NPC uses diodes.

NPC and FC need more power components to achieve greater inverter levels and suffer from voltage imbalance. In the CHB topology, H-bridge modules are allied in series, and the modular architecture is established by requiring each cell to possess its own DC supply [3].

This CHB architecture is advantageous for both single-phase and three-phase power conversion. CHB MLIs are suited for PV applications and are one of the three core MLI topologies. The primary block diagram of the grid-tied solar PV system is shown in Figure 1. MLI is essential in utilizing renewable resources for various applications [4]. Alternatively, all MLI research and development is limited to SC Multilevel Inverters (SCMLIs). Inherent balancing of

capacitor voltages and small size are the critical advantages of SCMLI over standard MLIs [5-11]. Within high-F AC microgrids, [12] suggests a quasi-resonant SC multilevel inverter.

A resonant inductor raises the charging current of switched capacitors. Despite being straightforward, this topology cannot be made better. In [13], a streamlined three-phase MLI is suggested. Four boosting switching capacitors are used in the individual phase of an inverter to provide different output levels. On the other hand, many capacitors and diodes are used.

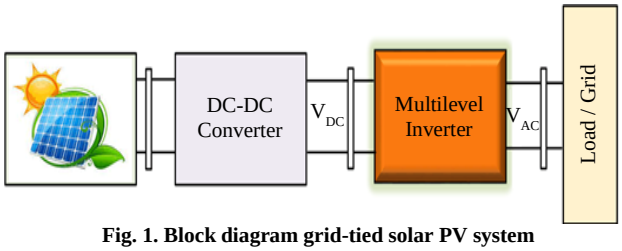


Fig. 1. Block diagram grid-tied solar PV system

The adaptable multilevel inverter and the 7L inverter both employ a T-type tie and the SC method. The self-balance and symmetry of the T-type structure are investigated. The literature has other instances of seven-stage SC inverters.

The H-bridge structure of [14] is the basis for the MLI topology in [15], contrary to the active NPC inverter designs. MLIs utilize either floating or switching capacitors. The voltage of FCs is kept back at 50% of the source voltage, attributable to the SC's voltage-maintaining capabilities.

Moreover, the literature presents the multilevel output and self-balancing core modules for MLI. Their intended use is in cascaded single-phase systems [16]. Every basic module uses a switching capacitor and has a comparable twin boost factor [17]. The 3L unit's maximum output via fewer components is just half of the input in [18]. At a voltage of 120V, the 7L, three-capacitor inverter (may be seen functioning in cascade) has a gain of 1.5. Because there are two asymmetrical DC sources in the 13-level module in [19], the two SCs are charged at different voltages. The planned use of these simple modules in cascading connections enables significant output levels.

Based on results from comparison for reference and voltages of capacitors and output current direction, redundant operating modes are selected for FC and CHB-based hybrid topologies [20]. Voltage balance may, therefore, be obtained via sensors. The extra balancing techniques necessary in the preceding MLIs add more components and complexity to govern. As a result, MLIs that avoid the difficulty of voltage balancing have gained popularity. The switched-capacitor approach combines a T-type construction in the 7L inverter [21] and the modular MLI [22]. The T-type structure's inherent balance with symmetric operation is used. The topology in [23, 24] provides further seven-level switched-capacitor inverters. The topology in [25] is based on an H-bridge structure, whereas that in [26] is based on an active NPC. The SCMLI proposed in [25] addresses this issue by including full-bridge cells. Each cell's voltage stress cannot go beyond the amplitude of the dc source.

Furthermore, involving the negative terminals of the DC source and output reduces leakage current. The topology in [27] has more diodes and capacitors and a low gain and high-cost factor for obtaining seven output levels. By adding more SC cells, the SCMLI in [28] can increase their production level. All the while, they are maintaining the ability to maintain equilibrium. Although it generates seven levels, the topology suggested in [29] has a problem with voltage stress distribution. Many different modulation techniques for controlling different MLI kinds have been presented in the literature [30-34].

This article presents the new Single-Source Switched Capacitor Seven-Level Boost Inverter (S^3C7LBI) architecture, addressing the abovementioned issue. S^3C7LBI uses a single source and nine power switches to provide seven output levels. Three times the input voltage is the maximum output voltage. The natural equilibrium of the SC voltages may occur even in the absence of sensors. These advantages demonstrate that the S^3C7LBI that is being described is a good fit for applications that need medium-low voltage/power levels, such as REG integration.

2. Single Source Switched Capacitor Seven Level Boost Inverter (S^37LBI) Topology

Figure 2 depicts the proposed Single-Source Switched Capacitor Seven-Level Boost Inverter (S^3C7LBI) topology. The proposed S^3C7LBI has just 02 switching capacitors and 11 power switches. The voltages of SCs may be balanced on input voltage without the need for sensors or other tools. The proposed S^3C7L BI max output voltage achieves three times the magnitude of V_{in}. Because of this, the S^3C7LBI being shown has a gain of 3. Seven levels are generated as 0, $\pm V_{DC}$, $\pm 2V_{DC}$ and $\pm 3V_{DC}$.

Table 1 demonstrates the switching logic of the proposed S^3C7LBI topology where 1 represents the switch is ON & 0 represents the switch is OFF. In Table 1, the red colour in the switching logic represents those switching states responsible for charging the two capacitors, which helps balance the capacitors' voltages to the voltage level of V_{DC}. Figure 3 (a)-(g) shows the suggested S^3C7LBI operating states at different phase output voltage levels ($+3V_{DC}$ to $-3V_{DC}$). At certain voltage levels, the cascade-connected capacitors C_1 and C_2 act as Switching Capacitors (SC) in parallel with the V_{DC} supply.

Consequently, the whole voltage of its C_1 is charged to V_{DC}; on the other hand, it discharges at output levels of $2V_{DC}$, $3V_{DC}$, and $-3V_{DC}$, while C_2 discharges at output levels of $3V_{DC}$, $-2V_{DC}$, and $-3V_{DC}$. Due to their symmetric discharge, V_{DC} may balance the voltages for C_1 and C_2. To produce a gain of three times the input voltage V_{DC}, C_1 and C_2 are coupled in a cascaded manner with a V_{DC} supply at $3V_{DC}$ and $-3V_{DC}$ to create the maximum output voltage.

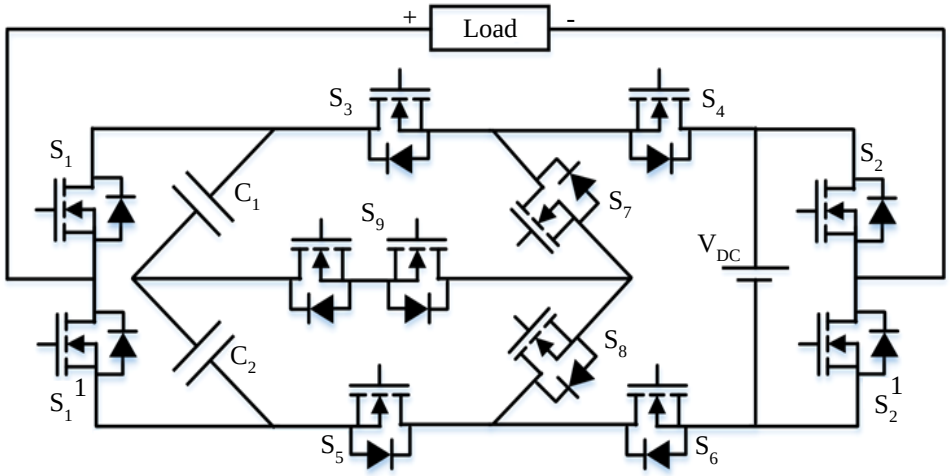
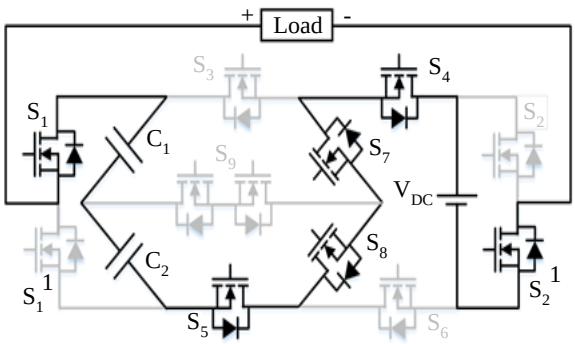


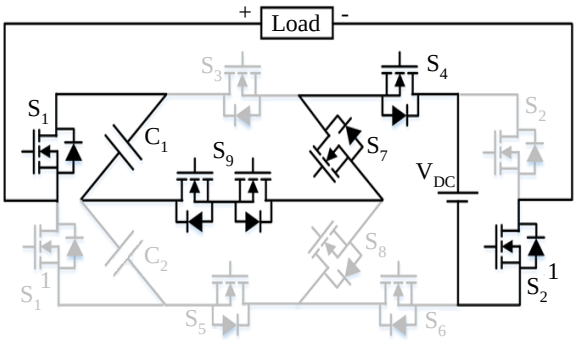
Fig. 2 Proposed S³C7LBI topology

Table 1. Switching states of proposed S³C7LBI topology

State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
$+3V_{DC}$	1	0	0	1	1	0	1	1	0
$+2V_{DC}$	1	0	0	1	1	1	1	0	1
$+V_{DC}$	1	0	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
$-V_{DC}$	0	1	0	1	1	1	1	0	1
$-2V_{DC}$	0	1	1	1	0	1	0	1	1
$-3V_{DC}$	0	1	1	0	0	1	1	1	0



(a) $+3V_{DC}$



(b) $+2V_{DC}$

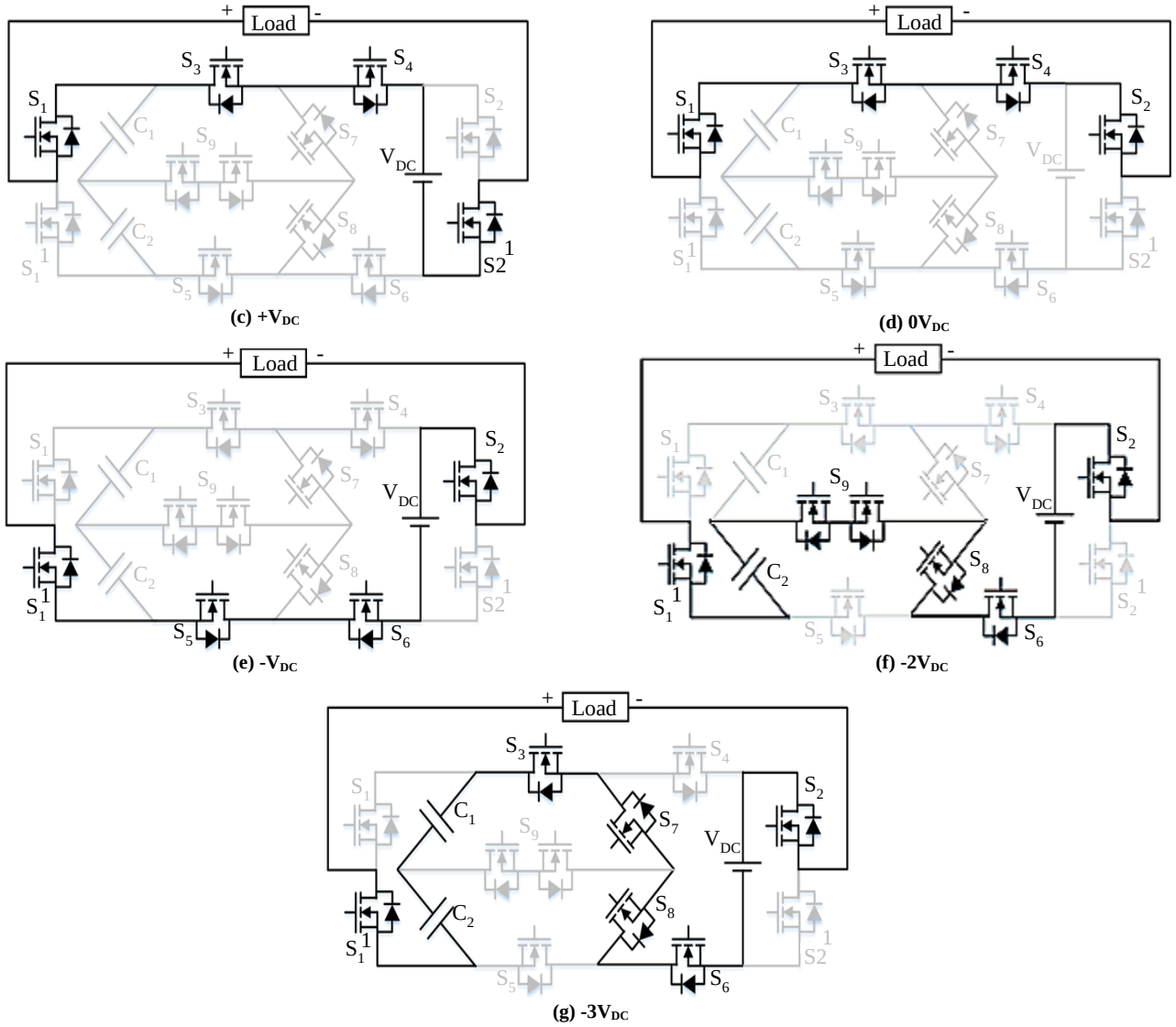


Fig. 3 Conduction paths of S³C7LBI for various voltage levels

3. Results and Discussions

3.1. Simulation Results

In this study, MATLAB simulation analysis has been performed to validate the provided S³C7LBI architecture. The S³C7L boost inverter uses the sinusoidal PWM scheme to create gate pulses for an inverter to power electronic devices. An in-phase carrier pattern, seen in Figure 4, is considered when using the SPWM approach to generate inverter pulses.

The following are considered for the simulation parameters: RL load, whose parameter values are well thought-out as L=110mH and R=100Ω, 100V DC source, and 1/3950Hz as switching frequency. Figure 5 shows the S³C7LBI phase voltage for a range of Modulation Index (MI) values, from 1.0 to 0.2, which validates the S³C7LBI architecture that is being proposed. The phase output voltage's number of voltage levels drops in tandem with a decrease in the value of M.

Additionally, Table 2 displays the phase output voltage levels concerning Modulation Index (MI) variation for the 7L inverter. Figures 6a and 6b show the phase voltage and current at an M value of 1.0 for two distinct load circumstances, R and RL.

Figure 7 depicts the load current waveform with a M value of 1.0. Figure 8 displays the frequency spectrum of the phase current and voltage at the unity modulation index.

Table 3 shows the phase voltage RMS and harmonic distortion for the dynamic values of M. These waveforms demonstrate that S³C7LBI can have closed-loop capability for solar photovoltaic applications.

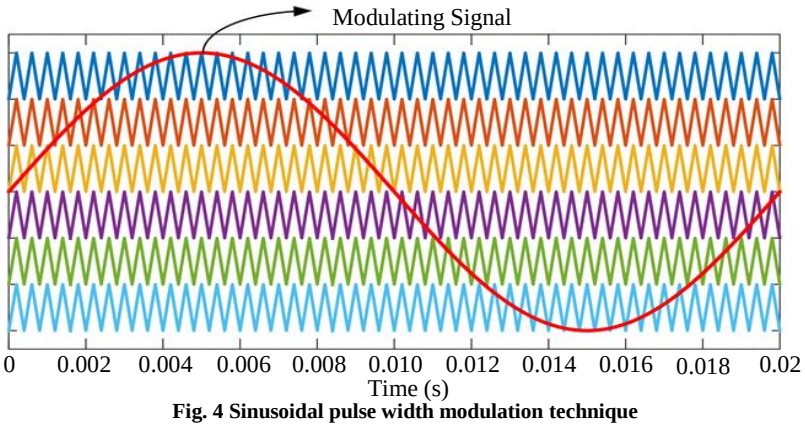
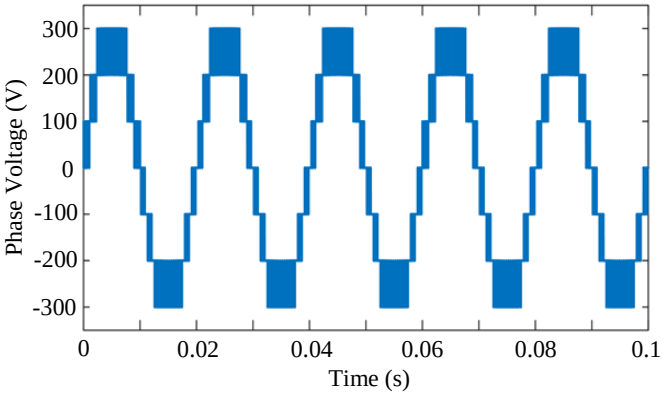
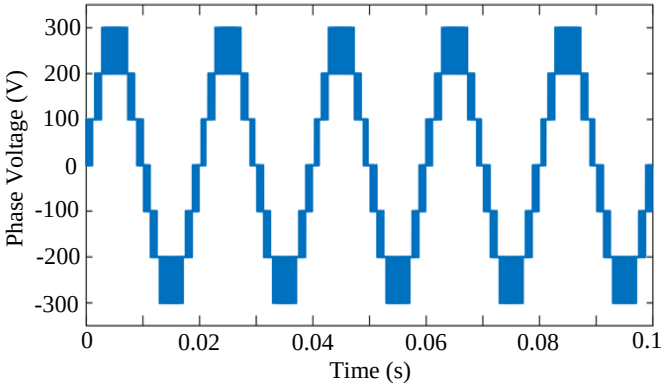


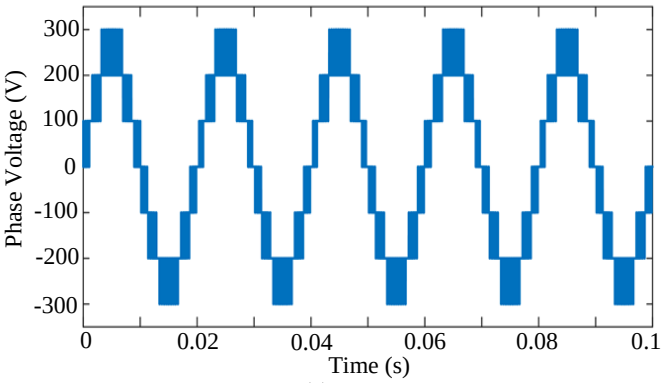
Fig. 4 Sinusoidal pulse width modulation technique



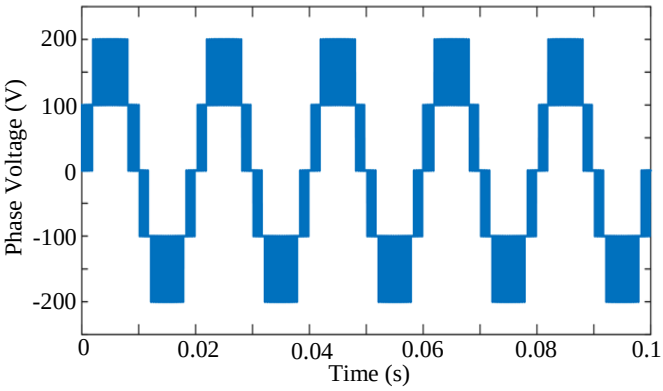
(a) M=1.0



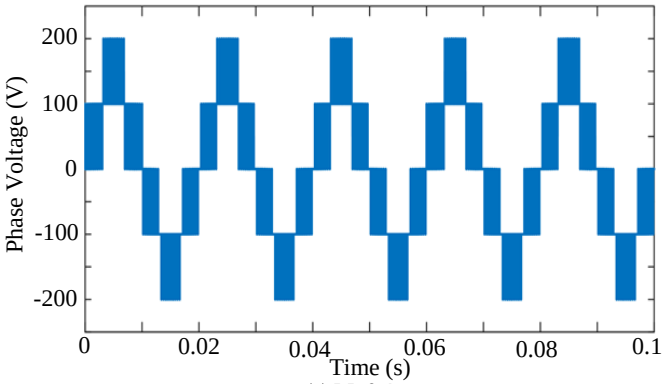
(b) M=0.9



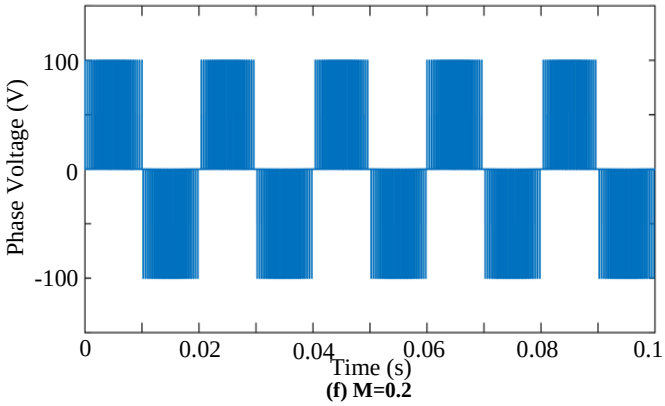
(c) M=0.8



(d) M=0.6

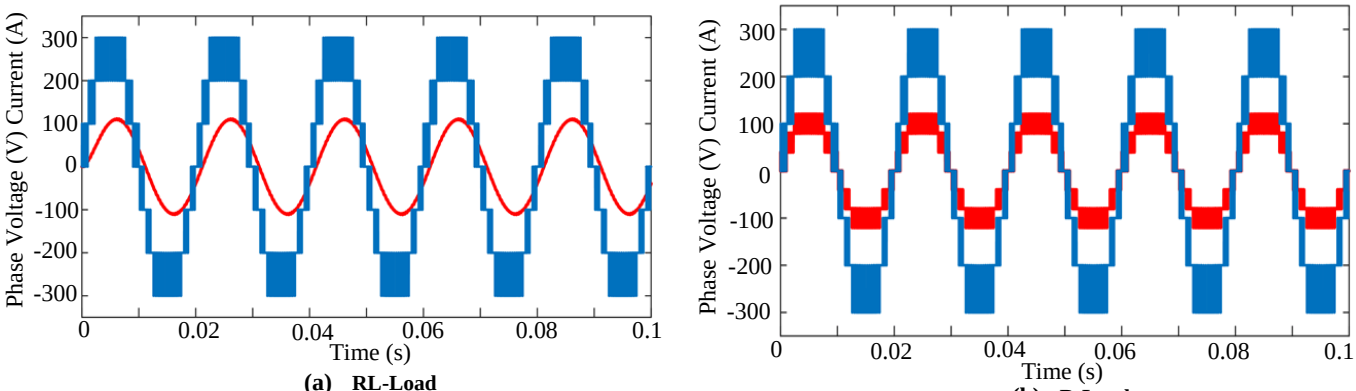


(e) M=0.4



(f) M=0.2

Fig. 5 S^3C7LBI output voltage waveform for dynamic values of M



(a) RL-Load **(b) R-Load**

Fig. 6 Phase current and voltage at M=1.0 for different load conditions

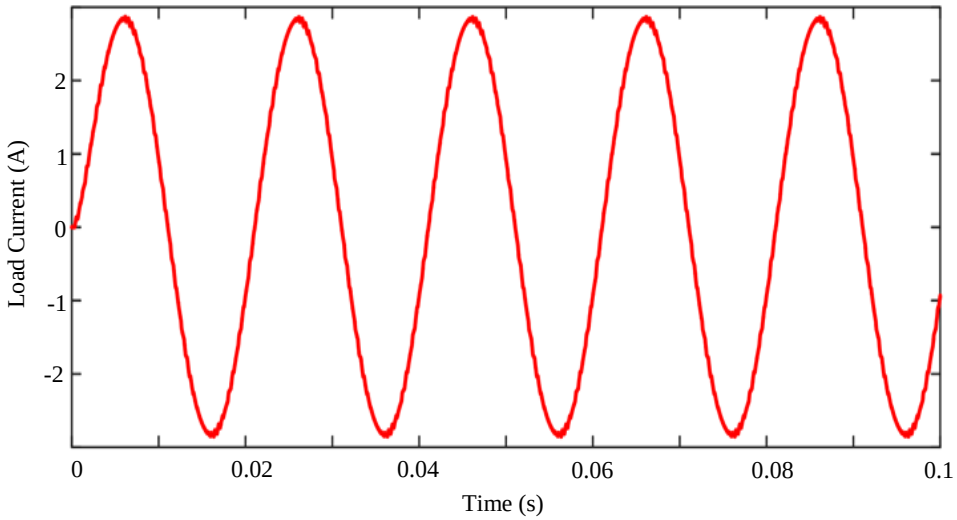
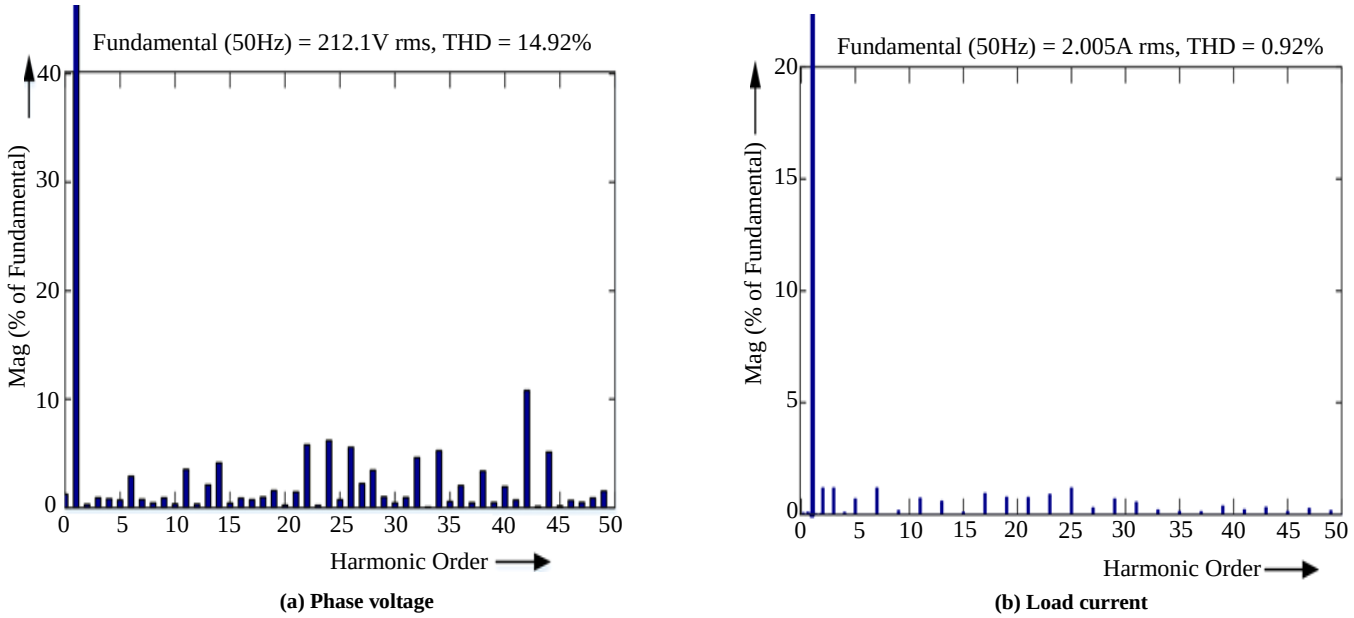


Fig. 7 Load current at M=1.0 for RL-load



(a) Phase voltage **(b) Load current**

Fig. 8 Frequency spectra at unity modulation index

Table 2. Voltage levels of inverter phase for dynamic values of M

Modulation Index	Phase Voltage Levels
1.0	7
0.9	7
0.8	7
0.6	5
0.4	5
1.2	3

Table 3. Inverter output phase voltage RMS and THD for dynamic values of M

Modulation Index	RMS Voltage	%THD
0.5	106	34.16
0.6	127.2	28.50
0.8	169.6	20.23
0.9	190.9	18.99
1.0	212.1	14.92

Table 4. Comparison of S^3C7L BI with the existing topologies

Topology	N_{sw}	N_{cap}	N_D	N_d	Gain	TSV_{pu}	Balancing Ability
12	12	3	0	12	0.5	6	Self
15	6	4	4	6	3	6	Self
14	8	4	2	7	1.5	6	Self
26	13	3	4	13	3	7.33	Self
28	14	2	2	14	3	5.33	Self
21	16	6	0	15	1.5	9.33	Self
19	8	3	0	7	0.75	5.33	Aux
29	7	3	2	7	0.73	6.33	Self
27	8	3	3	8	0.77	7.67	Aux
Proposed S^3C7LBI	11	2	0	10	3	5.33	Self

N_{sw}- No. of Switches, N_{Cap}-No. of Capacitors, N_D-No. of Diodes, N_d-No. of Gate Drivers, and TSV-Total Standing Voltage

3.2. Hardware Results

Experimental results have been reported as part of validating S^3C7LBI topology. The parameters of the modulation scheme and the load utilized in this study are precisely the same as those considered in the simulation. The power electronic switches' gate signals are made using the DSP TMS32F28335 toolkit. Figure 9 displays the practical seven-level inverter output phase voltage, and Figure 10 shows the load current at an M value of 1.0. Figure 11 shows at M=1.0 displays the frequency spectrum for the load current and voltage. The hardware results confirm the practicality of the presented S^3C7L boost inverter topology for real-time applications. Table 4 compares S^3C7LBI with the existing MLI topologies regarding component count, gate driver requirements, increasing ability, Total Standing Voltage (TSV) and inherent capacitor voltage balancing.

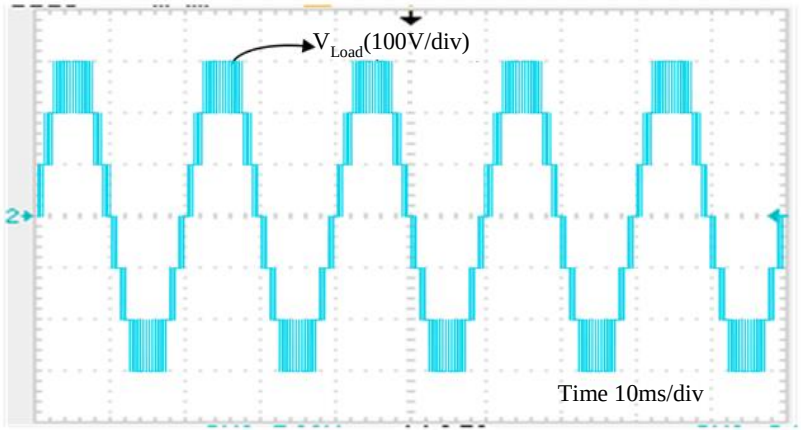


Fig. 9 Practical voltage waveform at M=1.0

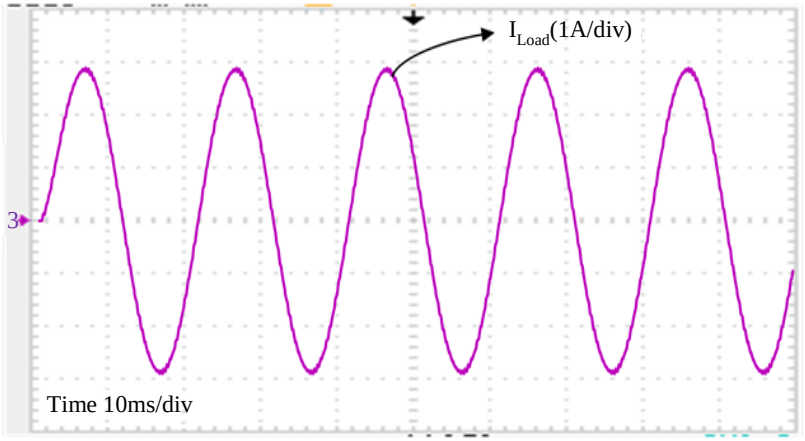
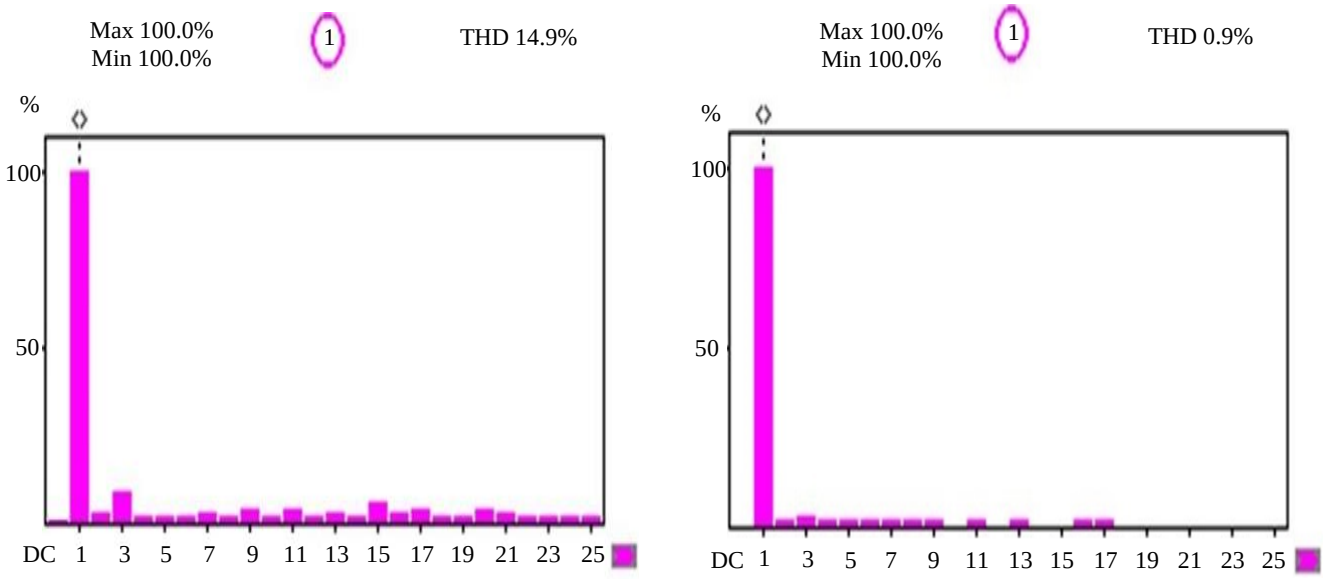


Fig. 10 Practical load current waveform at M=1.0



(a) Phase voltage **(b) Load current**

Fig. 11 Practical frequency spectra at unity modulation index

4. Conclusion

This paper presented a novel Single-Source Switching Capacitor Seven-Level Boost Inverter (S^3C7LBI) architecture for solar PV applications. It has a more straightforward control method and fewer components. With a three-times boost, it produces 7-levels. Furthermore, the two capacitors may attain equilibrium at V_{DC} without the need for any further sensors or control algorithms. There is inherent capacitor balance in the circuit. Due to its simplified control mechanism, the accompanying peripheral model and sensors have been significantly reduced. Its supporting aspects are the inherent balance, low number of power switches, high voltage gain value, and affordability of the S^3C7LBI. It has been thought that the operating S^3C7LBI architecture under dynamic situations is studied by using the sinusoidal PWM approach.

The MATLAB simulation results show the performance of the S^3C7LBI topology, and two distinct load circumstances are taken into account in the simulation to determine the viability of the suggested topology. Additionally, experimental findings have been provided to support the viability of the S^3C7LBI architecture that has been proposed. These results demonstrate that S^3C7LBI can have closed-loop capability for solar photovoltaic applications.

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