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Original Article

Conceptualization and Design of 8-Bit SRAM Using Quantum Dot Cellular Automata

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Abstract - *In the current landscape, nanotechnology stands as the foremost area of research, striving to shrink device sizes. Among the array of techniques within nanotechnology, Quantum-dot Cellular Automata (QCA) is heralded for its remarkable efficiency: boosting operating frequencies, minimal power consumption, and superior density. When it comes to designing circuits using Quantum dot Cellular Automata (QCA), the traditional method involves arranging these QCA cells in specific ways to achieve desired functions. Creating higher-level circuits is complex, and troubleshooting is even more challenging. However, this technology has the potential to execute all designs possible with CMOS technology. As per the existing works, the latch and flip-flop design is mainly considered only for storing data. An alternative to the traditional design is the hierarchical approach, which proposes an 8-bit memory element design in this paper. This paper proposes the inclusion of read and write signals in the memory register designed using QCA so that read/write signals can enable efficient access to the specific memory units. The proposed design occupies less area, QCA cells, and latency as well, thus leading to less circuit cost compared to existing works. Another precedence of this paper is the repeatability and regularity of the design, which aids in expanding the design size and can be applied to increase memory capacity as needed by making appropriate modifications to the designs. The results are simulated using the QCA Designer 2.0.3 tool for verification of obtained results. These designs can further be combined with other designs for application development.*

Keywords - *Clock zones, D Flip-Flop (DFF), Driver cells, Fixed cell, Normal cell, Polarized cells, SRAM.*

1. Introduction

Nanotechnology's significance lies in its various advantages, with device miniaturization standing out as a critical benefit. As per Moore's Law, device density doubles roughly every 18 months. However, in today's Integrated Circuit era, merely reducing device size is not sufficient for progress. Scaling down devices leads to significant secondary effects, posing notable challenges. Nanotechnology is emerging as a solution to tackle these hurdles.

Quantum-dot Cellular Automata (QCA) stands as a good alternative among existing CMOS silicon technologies [1]. It is a technology still in the research phase and has not been commercialized. QCA operates on a fundamental cell structure featuring two electrons positioned diagonally in a square cell [2].

This approach offers advantages of speed, power efficiency, device density, and operational frequency. QCA is considered to be one of the promising technologies among the other existing low-power technologies available [3]. The revolutionary QCA technology is founded upon a fundamental unit called the QCA cell, utilizing a pair of electrons as its core element [4]. To comprehend QCA circuits comprehensively, one must delve into the foundational aspects encompassing QCA cell structure, variants, alignments, layering, and interconnections.

Initial exploration into electron polarization within cell boundaries surfaced in Metal Island technology, birthing the magnetic QCA platform [5]. However, due to concerns surrounding reliability and efficacy, the magnetic QCA technology encountered setbacks. Consequently, the emergence of electrostatic QCA centred on electron manipulation has garnered attention as an innovative solution, offering the promise of circumventing the limitations imposed by CMOS technology.

The QCA cell, a basis of this technology, comprises four quantum dots positioned at the corners of a square, enclosed within a transparent material. Within these dots, a pair of electrons is strategically placed, diagonally opposite to each other. The configuration of these electrons is the digital bit stored within the cell, illustrated in Figure 1 [6].

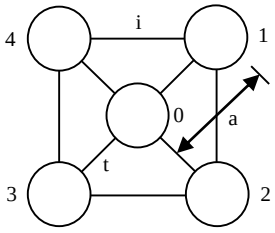


Fig. 1 QCA cell

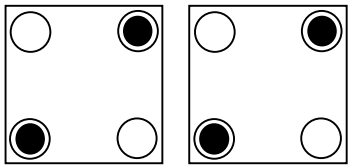


Fig. 2 Polarized QCA cells with (a) Logic 1, and (b) Logic 0.

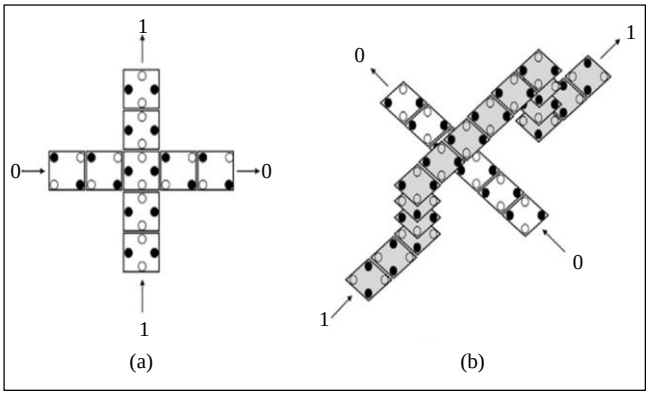


Fig. 3 Layered structure in QCA (a) Single layer, and (b) Multi-layer.

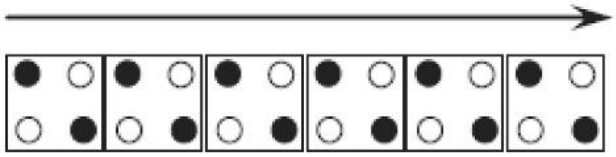


Fig. 4 QCA wire

Within QCA, two distinct types of cells exist: functional cells and driver cells. Driver cells serve as input ports, facilitating the transmission of values into the cell structure. Notably, these driver cells exert influence on adjacent functional cells by manipulating potential energies within the cell through Columbic interactions [7, 8]. This Columbic interaction, depicted as E_{ij} in equation-1, symbolizes the energetic interplay between the electrons within the cell.

$$Eij = \frac{1}{4\pi\pi e} X \frac{q1q2}{dij} \quad (1)$$

The interaction between electrons within adjacent cells is mathematically represented by q_i and q_j, denoting the electrons, and d_{ij}, signifying the distance between them. Whenever an electron changes its alignment, it reacts with the electron in adjacent cells and changes its position based on the force of attraction/repulsion. Quantum-dot Cellular Automata (QCA) offers two distinct arrangements: the Standard form, comprising cells placed adjacent to each other in a square layout, and the rotated form, where cells are rotated and aligned linearly in a rhombus pattern [8].

In both arrangements, information propagation occurs through the Columbic interaction among cells, as delineated in Figure 2 [9]. The functional cells within QCA systems can be further categorized into three classes: Normal, Fixed, and Output cells, as evident from the specified designs in the subsequent section. The adoption of QCA technology is advocated owing to the dense and compact arrangement of cells it facilitates. For wiring, QCA employs two primary layering techniques: Coplanar structures and multi-layered structures [10].

The multi-layered structure methodology ensures the segregation of signal crossings, aiding in the establishment of isolated pathways for networking and interconnecting modules within minimal space [11]. While the implementation of multi-layered crossings necessitates a precise calculation of cell numbers and layers, it has proven to be highly efficient in terms of space utilization. Figure 3 provides a visual representation of these two layering techniques [12].

A fundamental element within QCA is the wire, which is essential for facilitating cell interconnections. This wire structure is represented as a straightforward linear arrangement of cells, as depicted in Figure 4 [13]. The essential advantage of this linear cell arrangement lies in its absence of kink energy [14], enabling it to function as a wire [15] seamlessly.

This absence of kink energy ensures the smooth transmission of signals without encountering any disruptions or impediments along its path. Thus, this linear configuration serves as an effective means of establishing interconnections between cells within the QCA framework.

From the literature survey, we find that the development of QCA in circuit design has been somewhat sluggish since its inception. Researchers have extensively explored the design of digital circuits, like - adders [16, 17] and multipliers [18, 19], wherein adders are designed using majority voter gates, and in [20, 21], they are designed using strategic placement of QCA cells for logical functioning.

Design of multiplexers is also carried out similarly, using majority voter gates, in [22, 24], whereas [25, 26] gives a different designing strategy. The design of logic gates [9] has also achieved various successful outcomes. However, the progress in QCA circuit design has been relatively limited, reaching only up to the level of latches and flip-flops [27, 28],

especially D-Flip-Flop (DFF) [29, 30]. The memory elements have been designed previously but for single-bit memory storage [31, 32]. Memory elements are also enhanced for their circuit cost [33] and operating speed [34], but the realization has been restricted to a single-bit SRAM cell [35]. Research carried out in the QCA domain on designing SRAM modules has reached a level of designing single bit SRAM cells only [36].

It can be noted that the SRAM designed previously do not include Read/Write (R/W) signals. Since SRAM cells are considered to be memory elements, R/W signals are essential signals to be incorporated within the design. This paper introduces a new design strategy that is utilized for the creation of a D-Flip-Flop serving as a single-bit storage unit. Subsequently, this particular component, i.e., the single-bit storage unit, serves as a foundational element for designing memory registers. It is proposed to design SRAM units with the inclusion of R/W signals by utilizing these single-bit storage components. A methodical process is employed in the design of the D-Flip-Flop, using structured implementation, as explained in [29].

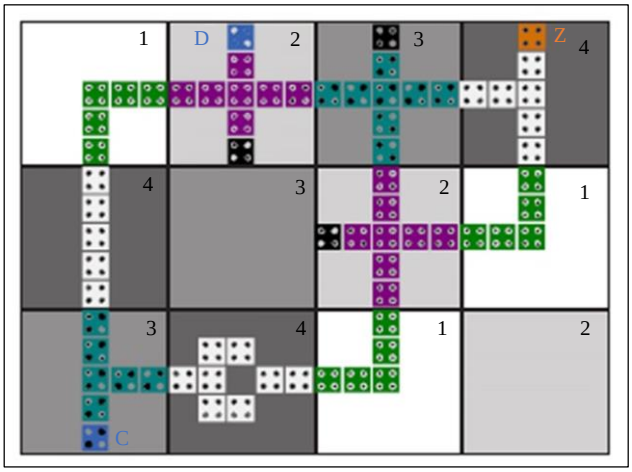
The design was first carried out on a single bit SRAM cell and then extended to 2-bit, 4-bit and 8-bit. The methodology implemented incorporates repeated and regular designs so that the memory element design can be extended further as and when required. These designs were optimized in order to reduce QCA cells and, hence, the occupied area.

The cascading functionality, i.e. designing one memory element and then repeating the design for the extension of the memory size, was validated by applying it to the shift-register design. After designing this optimized 1-bit SRAM cell, the design was expanded to 2-bit, 4-bit, and 8-bit SRAM.

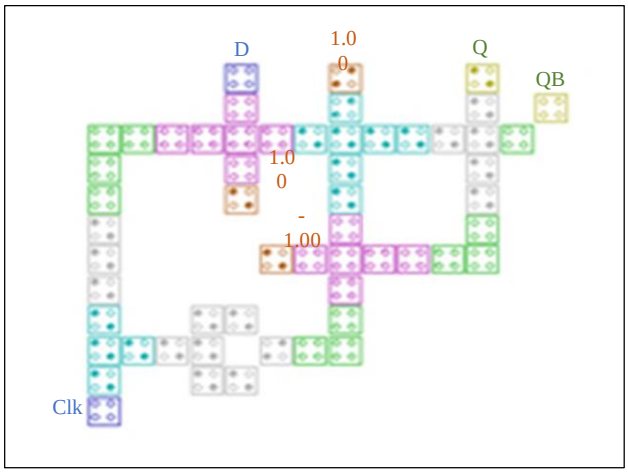
2. Materials and Methods

From [29], it is perceived that the design of DFF can be made efficiently by systematically arranging the logical function in a 5x5 QCA cell structure. This systematic arrangement of cells follows a universal, scalable, efficient clocking system.

As a process, this DFF is first tested and simulated for the correctness of the output, which is depicted in Figure 5(a) [29], Figure 5(b) and Figure 6. After satisfactory results of the flip-flop function are obtained, it is then modified as per the proposed design, having reduced cells. The design is then expanded to a bit of a flip-flop, connected to serve as a shift register. The initial 2-bit shift register undergoes a systematic expansion to accommodate a 4-bit configuration, necessitating comprehensive design alterations to facilitate this enhancement. Subsequently, this design is further scaled to operate seamlessly as an 8-bit shift register.



(a)



(b)

Fig. 5 D-Flip-Flop (a) Systematic structure [29], and (b) QCA implementation.

Despite these expansions, it is crucial to note that these registers, in their current state, do not fulfil the criteria to function as complete memory elements. These shift registers, along with their simulation results, are shown in Figures 7 and 8. The design and simulation of shift registers were performed to verify the regularity and repeatability of the design and the procedure of expansion of design size.

To elaborate, transitioning from a 2-bit to a 4-bit shift register and subsequently to an 8-bit variant entails a careful adjustment of the circuit's architecture, ensuring compatibility and coherence throughout the design evolution. However, while these advancements allow for increased data capacity and complexity, the registers, at this stage, lack the additional functionalities necessary to qualify as fully functional memory elements. This distinction is crucial as the registers solely serve the purpose of shifting data without incorporating the essential features required for comprehensive memory operation, such as data retention and recall capabilities.

The transformation of these shift registers into memory elements involves the integration of gating functions at the input terminals, serving as the fundamental mechanism for data storage. The corresponding QCA implementation, illustrating this operational shift and its subsequent enhancements, along with simulation results, are visually represented in Figure 9, and Figure 10. Through comprehensive simulation analysis, it becomes apparent that these redesigned circuits effectively emulate storage devices, thus justifying their categorization as memory elements. These designs are not only smaller in size but also possess read/write signals with the least latency.

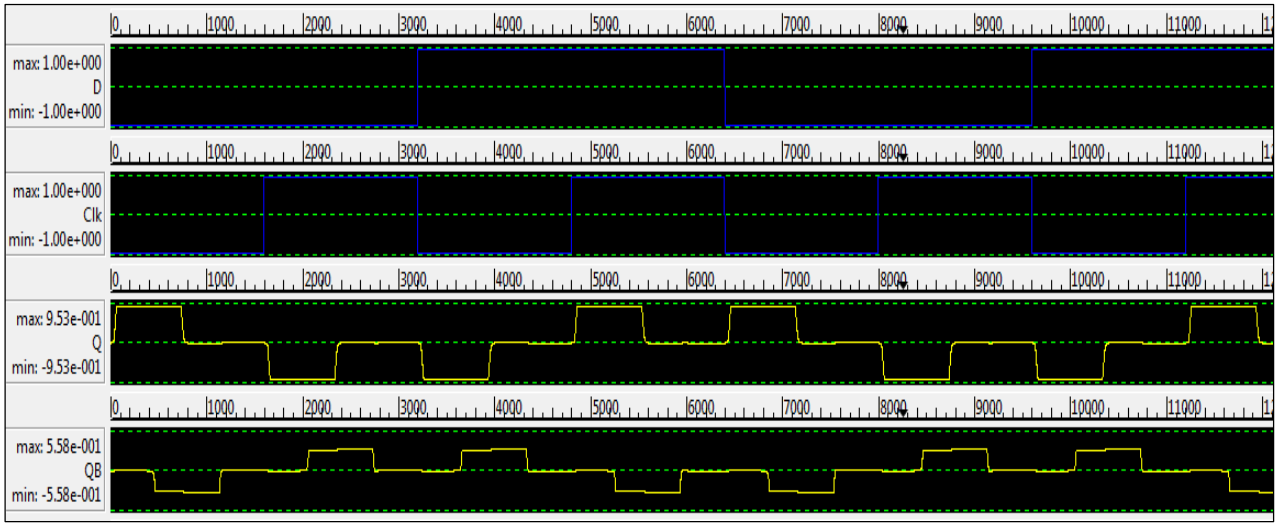
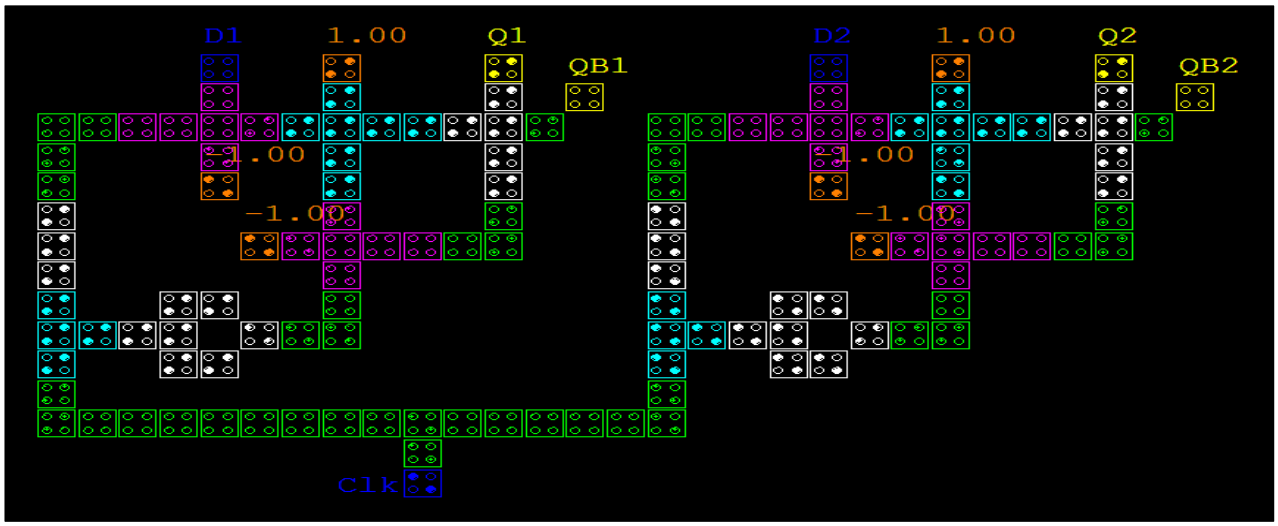
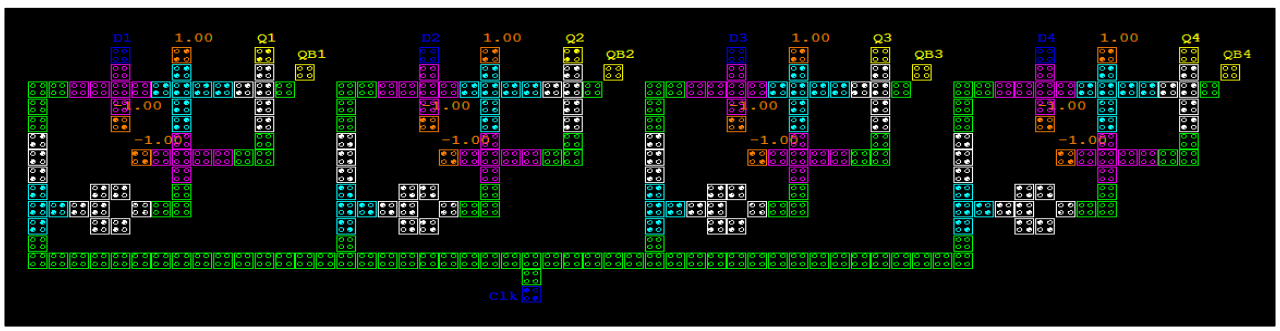


Fig. 6 D-Flip-Flop simulation results



(a)



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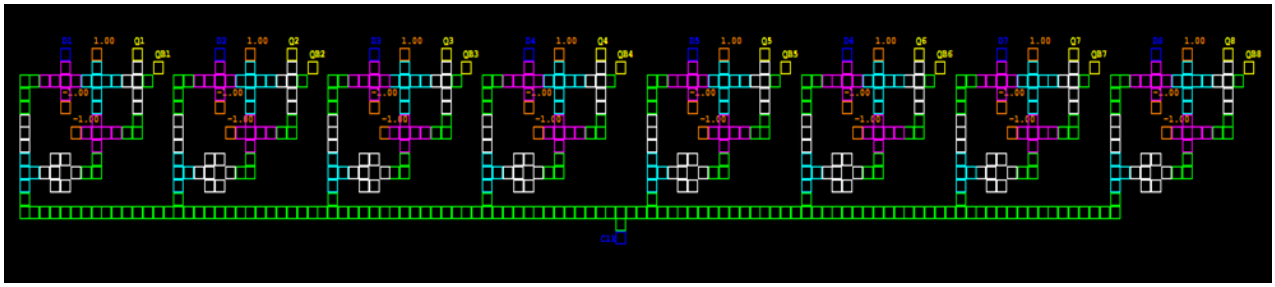
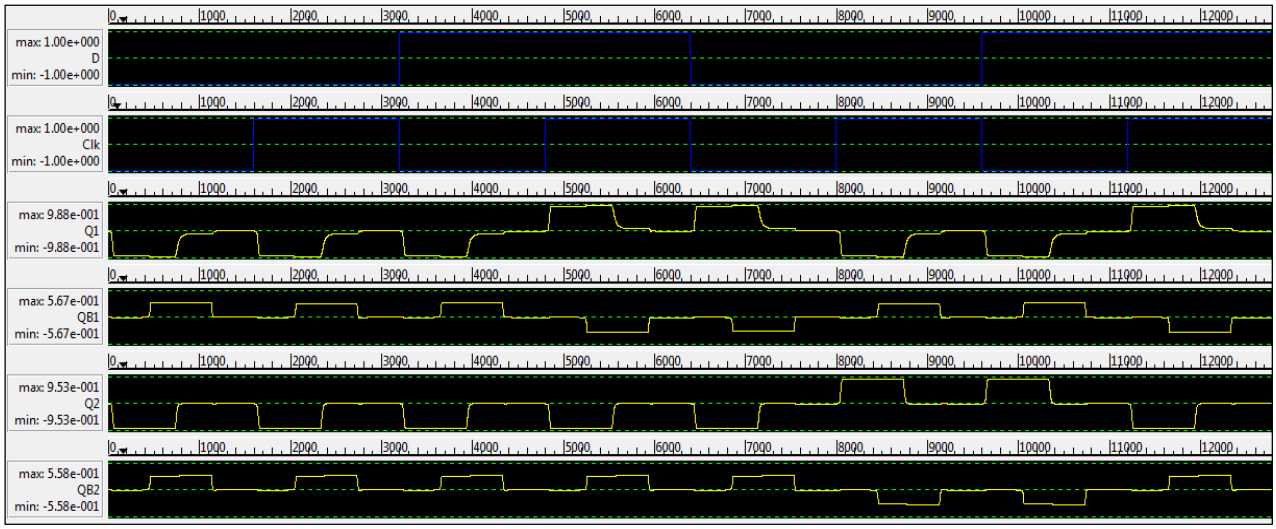
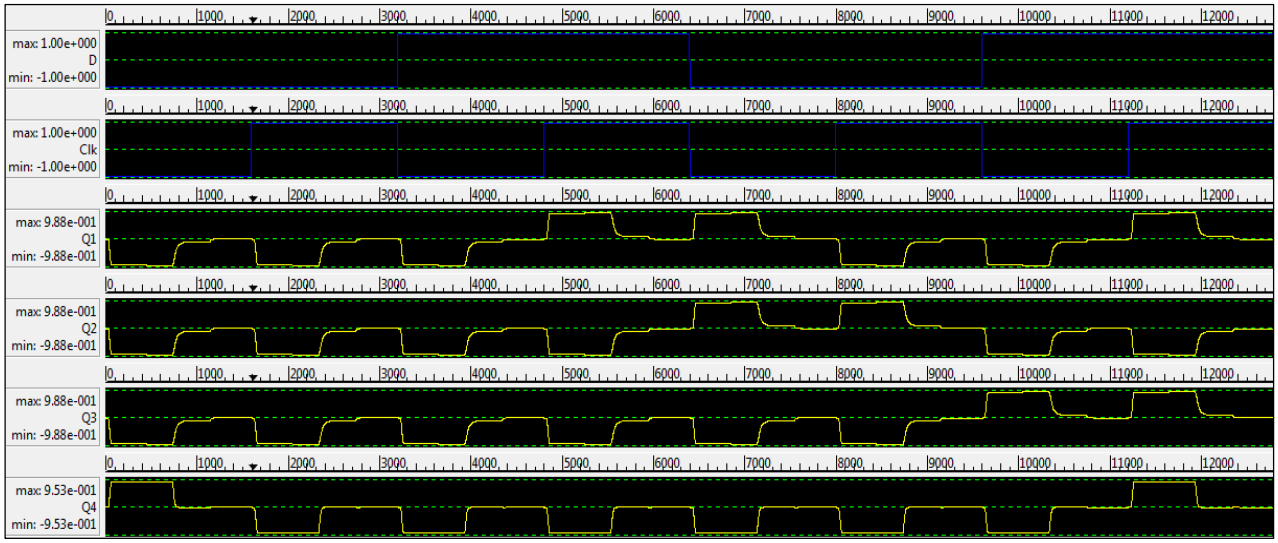


(c)

Fig. 7 Shift registers QCA implementation (a) 2-bit, (b) 4-bit, and (c) 8-bit.



(a)



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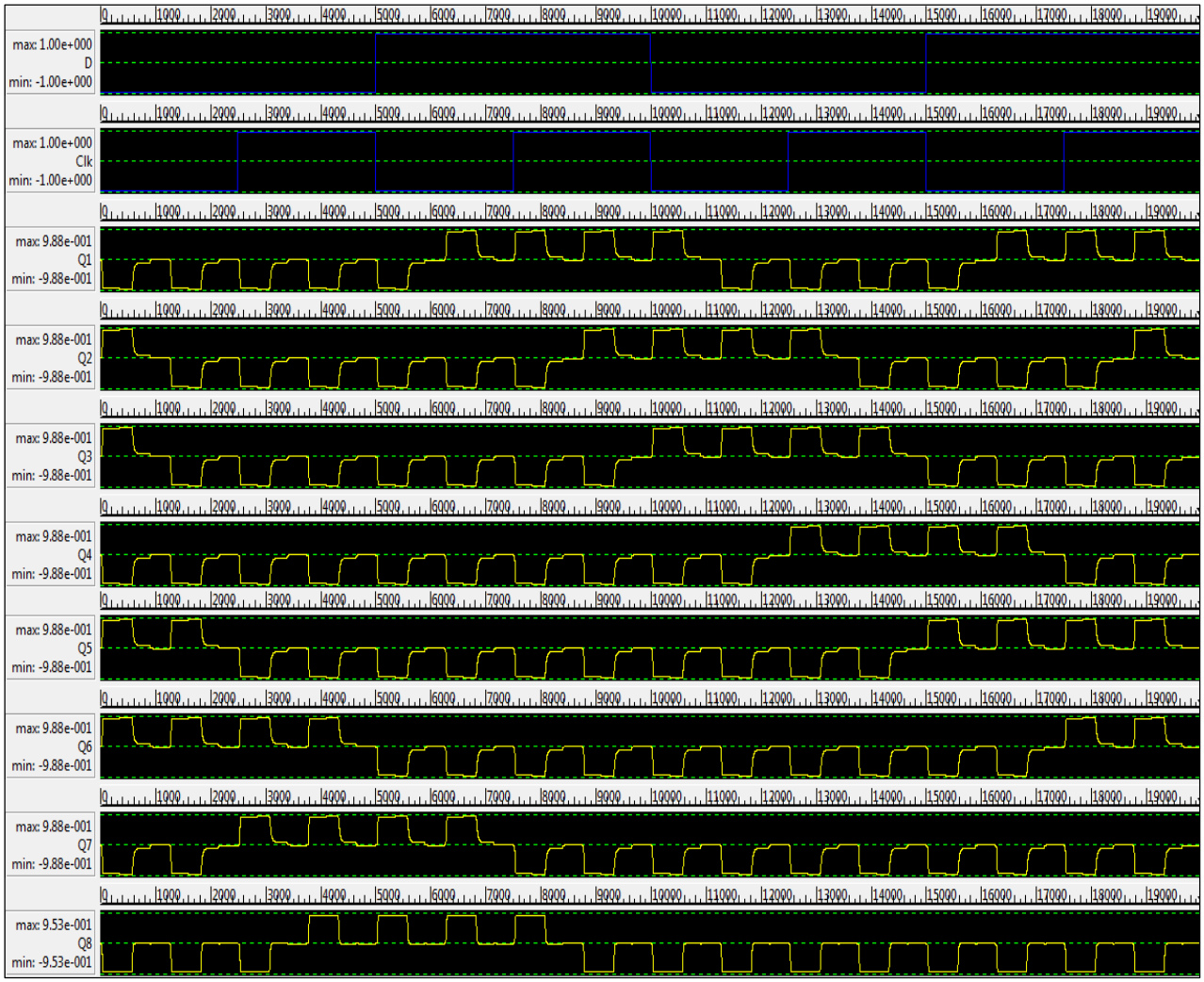
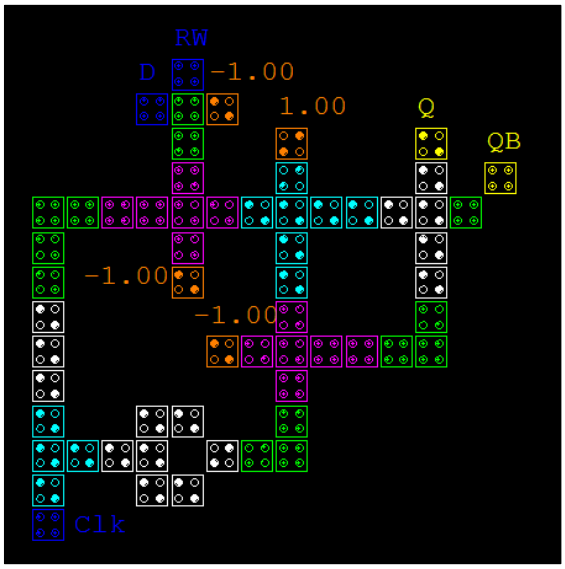
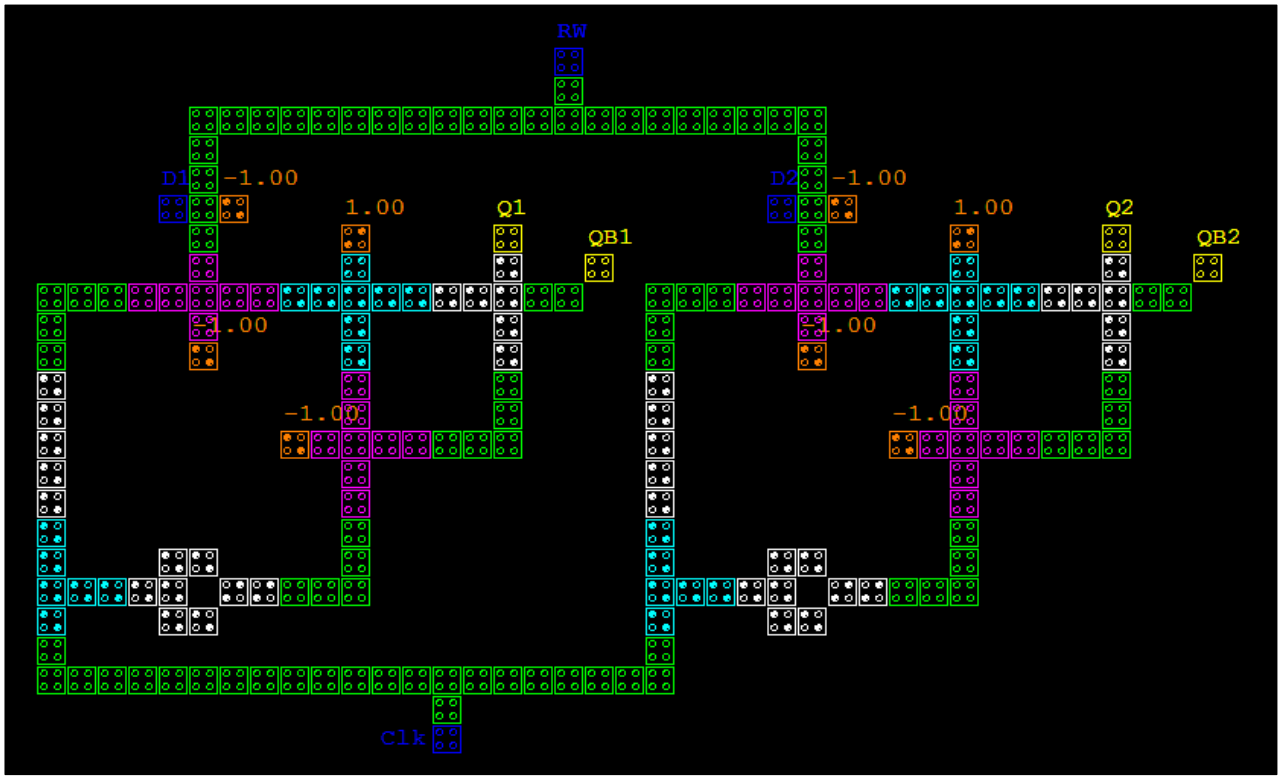


(c)

Fig. 8 Shift registers simulation results (a) 2-bit, (b) 4-bit, and (c) 8-bit.



(a)



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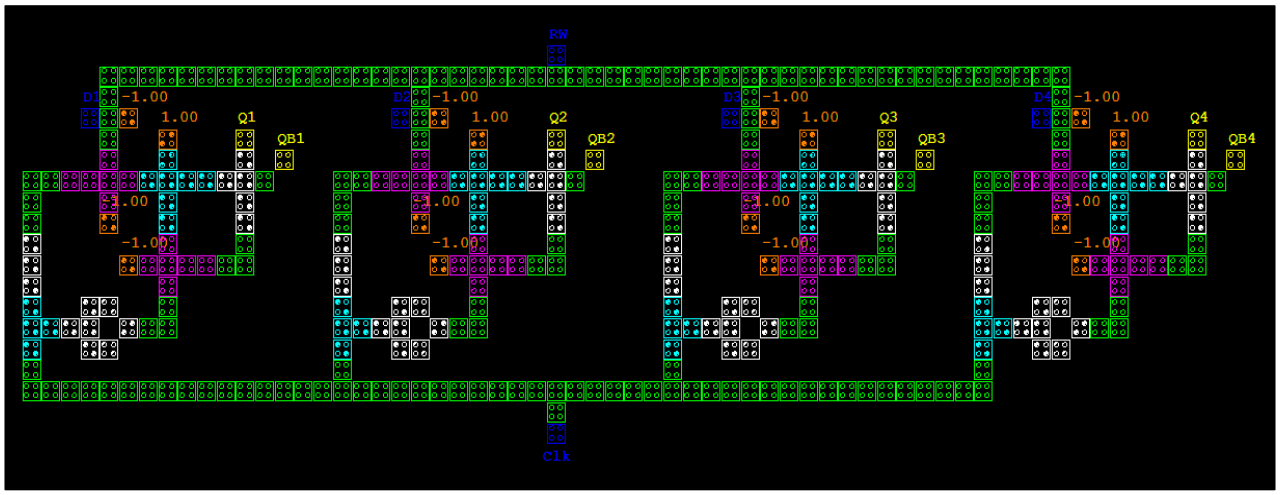
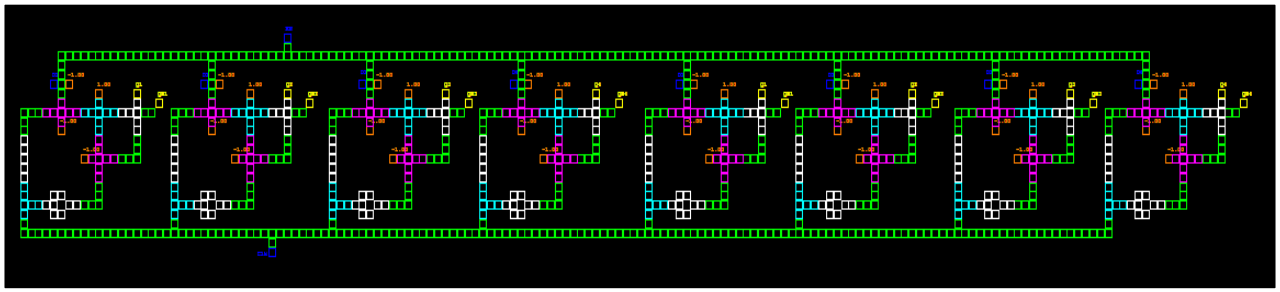
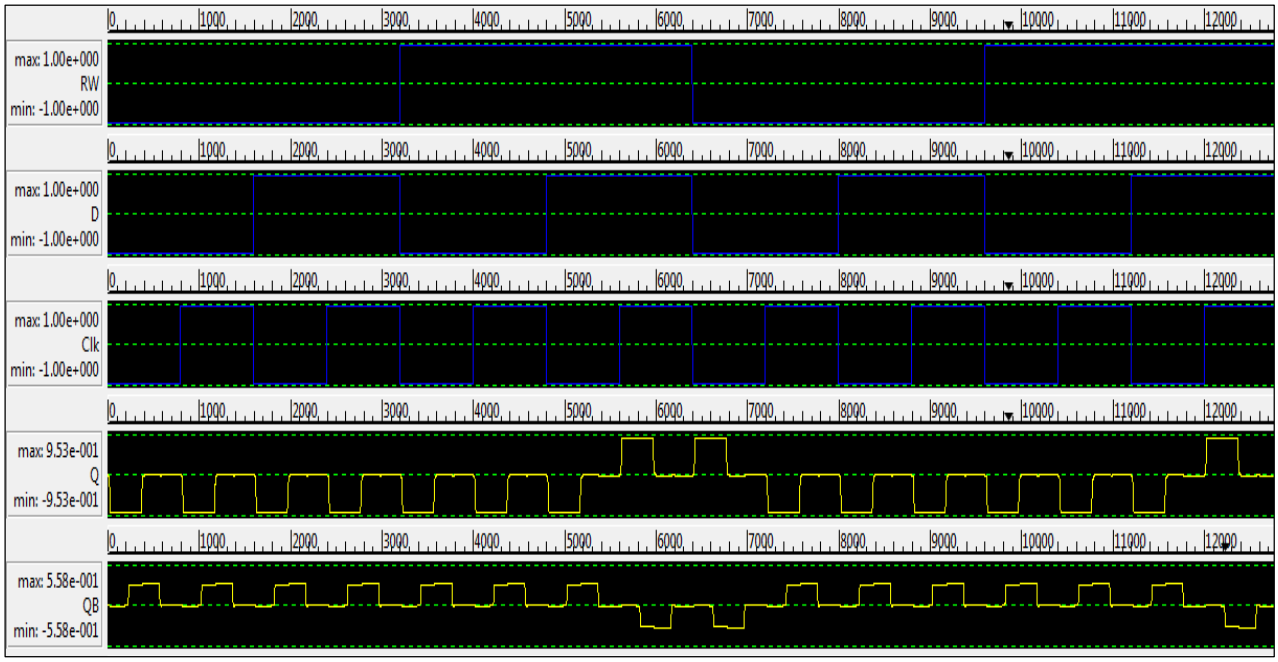


(c)



(d)

Fig. 9 SRAM using QCA implementation (a)1-bit, (b) 2-bit, (c) 4-bit, and (d) 8-bit.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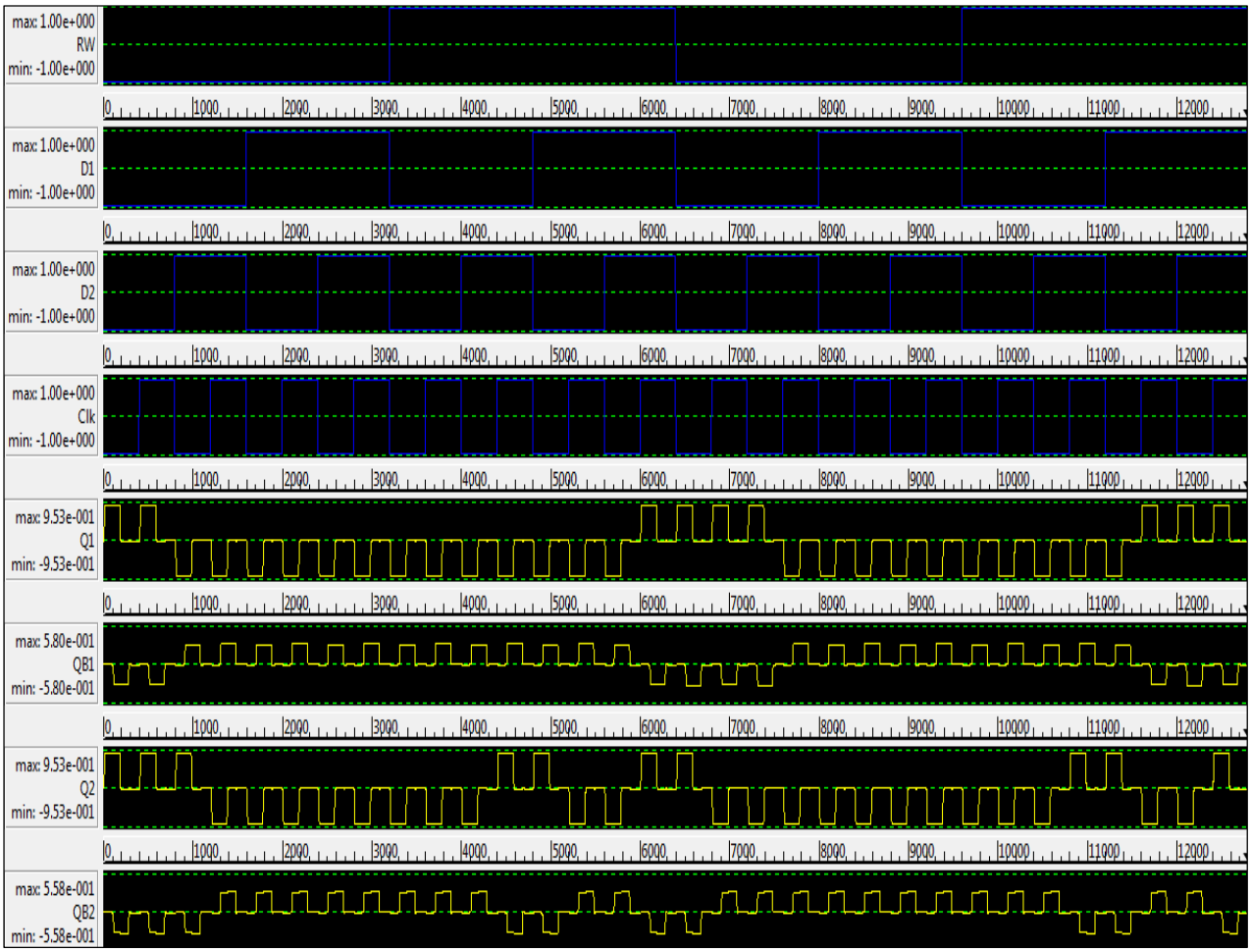
(a)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QB1
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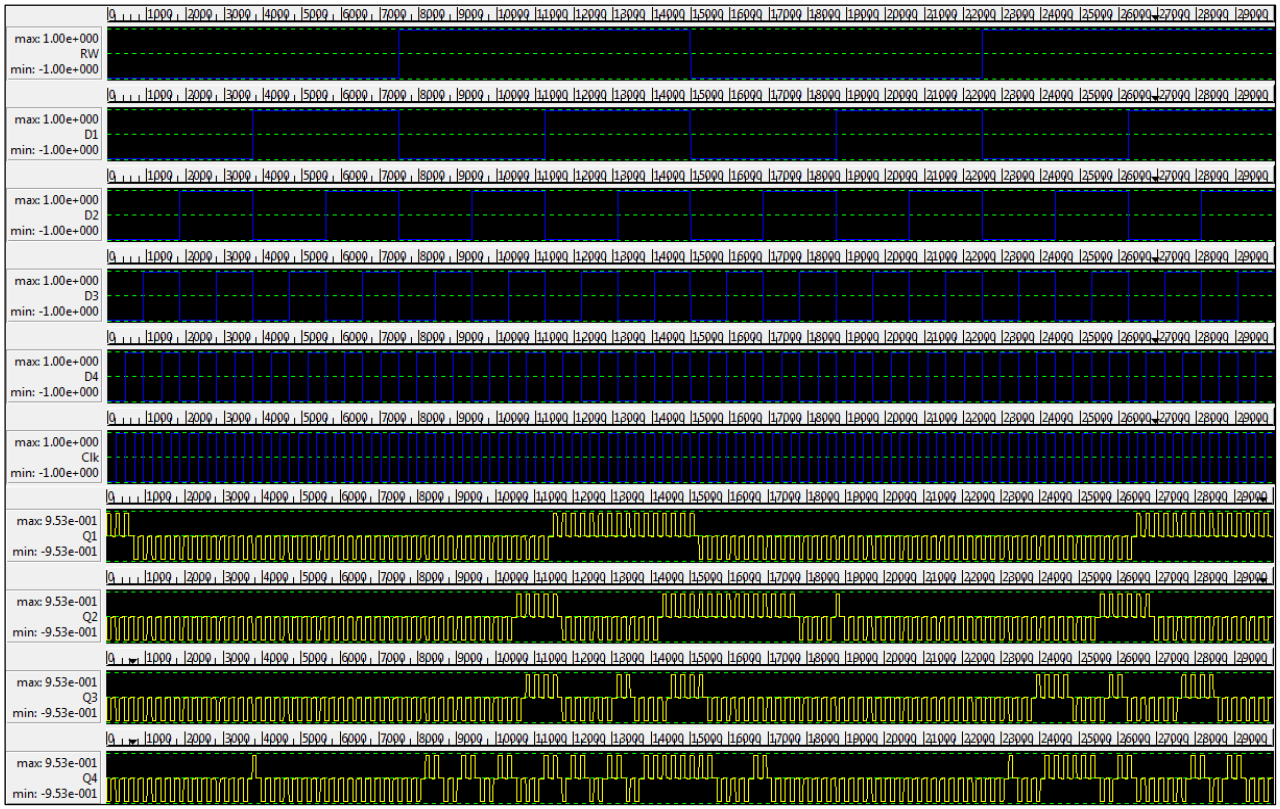

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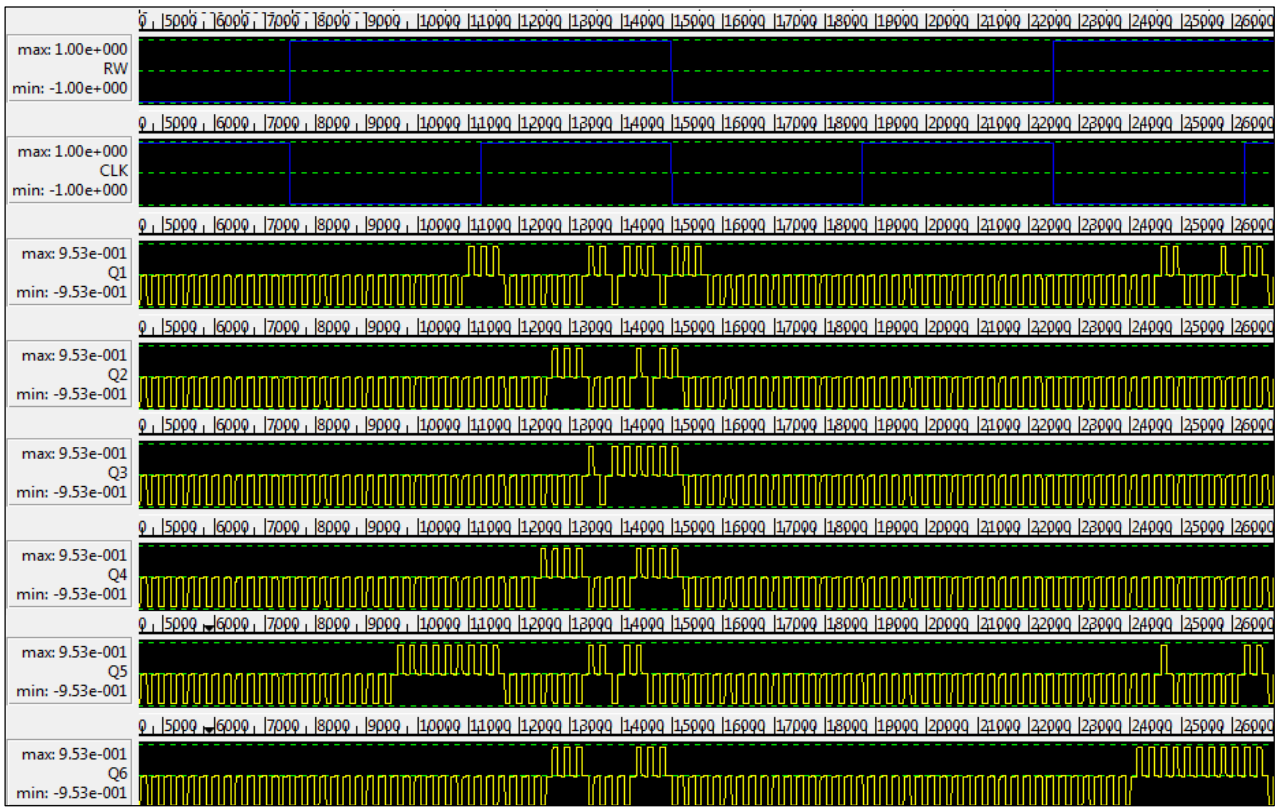

(d)

Fig. 10 SRAM simulation results (a) 1-bit, (b) 2-bit, (c) 4-bit, and (d) 8-bit.

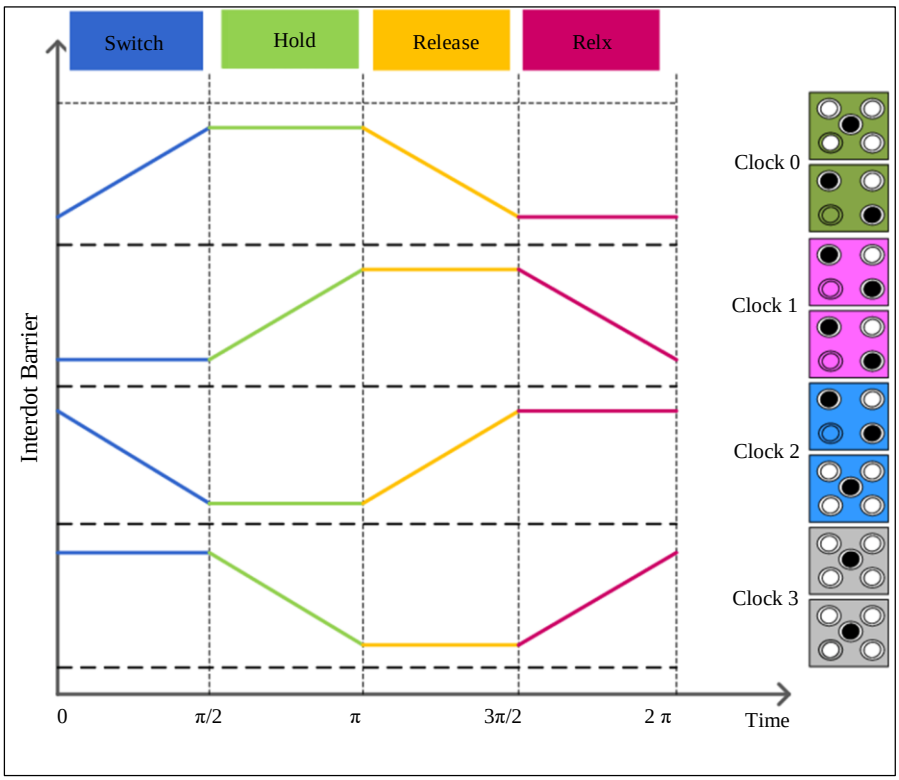

Fig. 11 Clocking zones in QCA

It is crucial to note that the approach taken to design these memory elements mirrors the methodology employed in creating the shift registers. Initially conceived as a 1-bit and 2-bit storage entity, the design gradually evolves, expanding to a 4-bit model and eventually reaching an 8-bit configuration. Consequently, this progressive approach culminates in the development of an 8-bit memory device, essentially functioning as an 8-bit SRAM explicitly tailored for data storage purposes.

The simulations detailed in this paper were conducted using the QCA Designer tool, specifically in version 2.0.3. The methodology involved initially designing the circuits followed by comprehensive simulations. To observe the design timings, clock and clocking zones are required to be considered. The clock not only serves the timing requirement of the designs but also as the power source for the cells in the circuit.

In the foundational designs, the cells were fixed to operate according to the "Clock 0" configuration, establishing their baseline functionality. However, in the more advanced circuits, diverse clocking zones, identified as "Clock 1", "Clock 2", and "Clock 3", were strategically positioned within the design layout to accommodate the proper flow of data.

The clock serves not only as a controlling signal for the data but also serves as the power source for all the cells. Thus, QCA will not require any dedicated power source for its functioning. The clock signal has four distinct zones. These distinct clocking zones were visually represented through distinct colour codes. The colour codes and clocking zones are shown in Figure 11.

The utilization of multiple clocking stages in QCA serves a vital role in enhancing synchronization and refining timing precision within the more complex circuits [37]. These strategic placements of clocking zones enable meticulous control over signal propagation, aiding in the optimization of circuit performance and reliability at higher levels of circuit complexity.

In essence, this systematic process demonstrates the evolution from essential shift registers into sophisticated memory elements such as SRAM, showcasing a hierarchical development approach that incrementally expands the data storage capacity while maintaining functional coherence and efficiency throughout the design progression.

3. Results and Discussion

In this section, the observations are listed first, and then a comparison of the proposed design with other existing works is presented. The validation of the proposed design is carried out using QCADesigner simulation tool 2.0.3. The simulated results are depicted in Figure 8 and Figure 10 for shift register and SRAM cells, respectively. The parameters for the simulation of the designs are,

- Simulation engine : Bistable Aprx.
- Simulation order : Random
- Clock high : 9.8 e-022
- Clock low : 3.8 e-023
- Clock shift : 0
- Layer separation : 11.5nm
- Maximum iterations per sample : 100

Utilizing the defined parameters within the simulation tool, the analysis produced is presented in Figures 8 and 10. These generated graphs can be verified for their logics, which depict the obtained results. A comprehensive study of these findings is detailed in Table 1. This tabulated information provides a structured overview, providing insights into the specifics of the observed outcomes, thereby depicting the understanding of the conducted simulations.

Table 1. Simulation results for QCA designs

Flip-flop Structure	No. of Crossovers	Area (in μm^2) (A)	QCA Cells (B)	Latency (Clock Cycles) (c)	Circuit Cost (A*B*C)
[30]	1	0.11	100	2	22
[31]	0	0.06	67	1.25	5.025
[32]	0	0.05	65	2.25	7.3
[33]	0	0.01	81	2.25	18.2
[34]	0	0.08	88	1.5	10.56
[35]	0	0.12	87	1.25	13.05
[36]	0	0.06	71	1.25	5.33
[37]	0	0.05	52	1.5	3.9
Proposed Design (1-bit Register with R/W)	0	0.09	56	0.5	2.52

Table 2. Comparisons of various SRAM designs implemented using QCA

Sl. No.	QCA Design Implemented	Parameter Observed	Value Obtained
1	2-Bit Shift Register	Total Cells	130
2	2-Bit Shift Register	Simulation Time	1s
3	4-Bit Shift Register	Total Cells	272
4	4-Bit Shift Register	Simulation Time	2s
5	8-Bit Shift Register	Total Cells	557
6	8-Bit Shift Register	Simulation Time	2s
7	2-Bit Memory Element	Total Cells	155
8	2-Bit Memory Element	Simulation Time	1s
9	4-Bit Memory Element	Total Cells	343
10	4-Bit Memory Element	Simulation Time	2s
11	8-Bit Memory Element	Total Cells	713
12	8-Bit Memory Element	Simulation Time	4s

Table 3. Findings of proposed SRAM designs

Proposed SRAM Structures	No. of Crossovers	Area (in μm^2) (A)	QCA Cells (B)	Read/Write Capability
1-Bit	0	0.09	56	Yes
2-Bit	0	0.23	155	Yes
4-Bit	0	0.54	343	Yes
8-Bit	0	1.10	713	Yes

Table 1 suggests that when the design size is doubled, there is a nearly proportional increase in the number of QCA cells, consequently leading to an extended simulation time. To authenticate the conducted research, the comparison was undertaken as a means of validation. This comparative analysis primarily focuses on the flip-flop design, the results of which are outlined in Table 2.

Additionally, to enrich this validation process, several SRAM designs have also been attempted and included for comparison, as elucidated in Table 2. Though many researchers have worked on the designing of SRAM as memory elements, only the most widely cited designs have been used for comparison in the table [30-37].

In Table 2, for comparison of the proposed design of the memory element, a 1-bit memory element is used in all the designs for comparisons, as in all other cited references, the design was proposed for single-bit element functionality. It is evident from the table that the proposed design of a single-bit register has the least latency and circuit cost along with Read/Write signal to enhance the design SRAM. Nevertheless, the proposed design can be extended to any number of bits as per design requirements.

The design of a single-bit SRAM is shown in Figure 9(a). This design includes a Read/Write signal (R/W) along with complemented output (QB). The design was then extended for 2-bit realization, as shown in Figure 9(b) and tested with simulation tools. After getting satisfactory results, the design was further extended to 4-bit and 8-bit SRAM structures shown in Figures 9(c) and (d), respectively.

The table of findings from the realization of the proposed SRAM cell, 1-bit, 2-bit, 4-bit and 8-bit, is depicted in Table 3. Table 3 presents a comprehensive overview of the proposed design of SRAM as memory units. This table serves as a parametric measure that evaluates the outcomes of the research undertaken against prior works. By incorporating insights from similar studies in the field, this comprehensive comparison enhances the credibility and depth of the findings, providing validation of the research endeavours.

It is very clear from the comparison table that the proposed design has the least number of QCA cells and clock latency compared with the other designs. This leads to the lowest circuit cost, as seen from the last cell in Table 2. For detailed analysis, Table 3 represents the findings of the proposed design for extended sizes of SRAM, as only a single-bit SRAM was utilized in Table 2 for comparison with other existing designs of single-bit size.

4. Conclusion

In summary, the accomplishment of designing memory elements hinges on a systematic, step-by-step approach known as hierarchical design. This method not only eases the creation of intricate circuits but also offers robust solutions for debugging and troubleshooting throughout the design process. The systematic nature of this approach allows for pinpointing and rectifying issues at any stage of the design phase.

The primary strength of this design and the design methodology lies in the area occupancy, latency and circuit cost of the proposed 8-bit SRAM design. The incorporation of the Read/Write signal adds significant value to the designs. Operating within a structured framework, the methodology cleverly employs cell blocks strategically to achieve precise, logical functions. By employing this hierarchical approach, the creation of both shift registers and memory elements tailored for data storage is fine-tuned for data storage efficiently. This optimized process streamlines the development of these components, ensuring their efficiency and effectiveness in storing and managing data within the circuitry.

4.1. Future Scope

The authors intend to advance their work by employing a similar methodology to design higher-level circuitry. Additional features can be incorporated into the design for further enhancement of the SRAM functionality. This strategic approach involves piecing together intricately designed components to construct a specialized circuit tailored for specific applications, thereby showcasing the potential and versatility of QCA technology in broader circuit design endeavours.

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