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Original Article

Analysis of Level Shifting Multicarrier Based Hybrid Multilevel Inverter with Open Circuit Fault-Tolerant Capability Using Single and Multiple Switch Fault

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Abstract *- MLI is widely used in applications such as renewable energy systems, electric vehicles, HVDC, FACTS devices, etc. This paper analysis the Fault tolerant operation of a hybrid multilevel inverter. The proposed multilevel inverter structure utilizes only eight unidirectional switches, four diodes, and 4 DC sources employing Geometric Progression (GP) based binary asymmetric DC source configuration to produce 31-level output. The phase disposition pulse width modulation method is applied to create the commutating pulses to the proposed inverter. The fault analysis deals with fault identification, isolation, and compensation. The fault-tolerant block does the fault identification. The isolation and compensation of fault are done by the FDI block in which the faulty switch is detected and it is substituted with a backup auxiliary switch. The open circuit fault is inspected, and the results are analyzed using Simulation in MATLAB/Simulink environment. In case of fault tolerance, additional backup auxiliary switches are added so as to compensate for the fault. Therefore, the fault-tolerant 31-level inverter circuit transforms into 16 switches, four diodes, and 4 DC sources. All the switches employed in the proposed structure are unidirectional; thus, using less no of components to achieve 31 31-level fault-tolerant multilevel inverters with increased reliability and low cost is proposed. Also, the power quality is analyzed by evaluating the Total Harmonic Distortion (THD) for all cases with and without fault. The feasibility of the circuit is examined through Simulation. From the results, it is evident that the proposed circuit can resist the single and multiple switch faults.*

Keywords *- Hybrid Multilevel Inverter (HMLI), Phase Disposition Pulse Width Modulation (PDPWM), Fault Detection, and Isolation unit (FDI), Fault-Tolerant Unit (FTU), Total Harmonic Distortion (THD), Reliability, Fault-tolerant, Single switch fault, Multiple switch fault.*

1. Introduction

In recent years, multilevel inverters have been extensively employed in high-power applications for several reasons, including improved output quality, reduced switching stress, high voltage capability, and fault tolerance. Multilevel inverters are used in applications such as renewable energy sources (solar, wind, hybrid of solar and wind), industrial applications such as motor drives, electric vehicles, Hybrid electric vehicle, Plugin hybrid electric vehicles, FACTS devices, inverters, and generators.

The improved power quality is achieved in multilevel inverters by attaining multiple levels at the output voltage waveform to resemble the shape of a sine waveform. In general, the multilevel inverters are classified as a) Diode Clamped Multilevel Inverter [1-3] - uses diodes to clamp voltage at different levels. The number of clamping diodes used decides the output voltage levels. b) Flying capacitor Multilevel Inverter [4-6] - uses a capacitor to store energy and produces a stepped output waveform. A large no of voltage levels is achieved. c) Cascaded H-bridge Multilevel Inverter [7-9] - uses series connected H-bridge modules to create stepped output waveform. d) Hybrid Multilevel Inverter [10-12] - the combination of two or more of the above types to create steeped output.

On the other hand, these traditional MLI configurations are restricted by problems such as an increase in the no of devices frequently exposed to switches to faults resulting in low reliability and increased economic loss [13]. Despite the fact that these multilevel topologies are highly diverse from one another, they still share the same reliability problem associated with the chance of semiconductor device failures [14-16]. Thus, new multilevel inverter topologies are needed to be designed to improve reliability with increased power quality. The hybrid multilevel inverters incorporate two or

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more types of inverters to produce large no of output voltages with less number of switches.

The essence of reliability in engineering is to prevent the creation of failures and faults [17]. Failure of switches occurs due to open circuit faults and short circuit faults. When the switches are subjected to open circuit and short circuit faults tends to improper function of the inverter, resulting in distorted multilevel output voltage [18]. The primary function of a fault-tolerant system is to sustain the operation under faulty situations [19].

Open circuit fault is caused by a variety of reasons, such as failure of the gate driver, breakage in the internal connection of the circuit due to heat, and lift-off wire from the circuit [20, 21]. When an open circuit fault occurs, stress on the components increases, causing additional problems. Also, the OC fault results in high THD, causing low power quality [22]. A short circuit fault is the most serious fault. SC leads to increased current causing severe damage to the entire components of the circuit in a short time [23]. This type of fault is caused by overvoltage, overheating, failure of the freewheeling diode, etc. The short circuit fault can be converted into an open circuit fault by connecting a fast fuse in series with the switches so that at SC faulty case, the fuse opens, causing an open circuit fault [24].

Many researchers have presented fault-tolerant techniques in conventional multilevel inverters to increase the reliability of the circuit. Fault-tolerant topologies of diode clamped multilevel inverter [25, 26], flying capacitor [27, 28] and cascaded H-bridge inverter [29, 30] are investigated, resulting in increased reliability, but the complexity of the system is increased. To overcome these hybrid multilevel inverter topologies is analyzed with fault-tolerant capabilities [31, 32].

Steady-state circumstances are the main focus of many fault analysis investigations. It's possible that the dynamic behavior of multilevel inverters under fault conditions hasn't been thoroughly investigated. Researching the dynamic effects and transient response during and after a fault could be very beneficial. Effective fault detection and mitigation solutions require an understanding of how many problems happening concurrently or sequentially affect the system's performance and dependability.

This article examines a hybrid multilevel inverter structure that can create an output voltage waveform with 31 levels. The proposed multilevel inverter structure utilizes only eight unidirectional switches, four diodes, and 4 DC sources. The level shifting multicarrier modulation technique is involved to obtain low THD resulting in high power quality. The fault-tolerant topology is created for the proposed structure by adding the backup auxiliary switches in parallel with the main switches. Hence, the circuit transforms into 16 switches, four diodes, and 4 DC sources to operate as a fault-tolerant circuit. The open circuit fault is evaluated. Single switch fault and multiple switch fault cases are analyzed by using the MATLAB/Simulink simulation tool. Also, the power quality of the system is evaluated in faulty instances as well as before and after faults.

2. Proposed Multilevel Inverter

The structure of the proposed hybrid 31-level inverter is displayed in Figure 1. The circuit incorporates two parts: a level generator and an H-bridge inverter. The switches with a diode and a DC source are connected to form a group. Four groups of this type are connected in series to form the level generator. The output of the level generator acts as input to the H-bridge inverter.

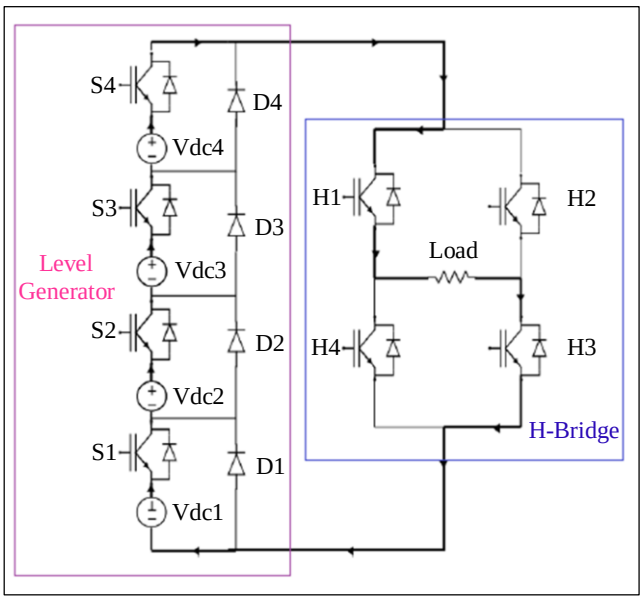

Fig. 1 Proposed hybrid multilevel circuit

2.1. Level Generator Circuit

The level generator consists of four switches, four diodes, and four DC sources. The DC sources are in asymmetric binary progression. If the DC sources are of different values, it is said to be asymmetric. The progression of DC sources may be binary or trinary configuration. If the succeeding source has a value equal to twice the preceding source, then it is said to be binary.

Example $V_1 = V_{dc}$, $V_2 = 2\ V_{dc}$, $V_3 = 4\ V_{dc}$, $V_4 = 8\ V_{dc}$, $V_5 = 16\ V_{dc}$ and so on. Similarly, if the succeeding source has the value equal to thrice the preceding source then it is said to be in trinary. Example $V_1 = V_{dc}$, $V_2 = 3\ V_{dc}$, $V_3 = 9\ V_{dc}$, $V_4 = 27\ V_{dc}$, $V_5 = 81\ V_{dc}$ and so on. The proposed hybrid multilevel inverter uses the asymmetric binary configuration. Here V_1=6V, V_2 =12V, V_3=24V and V_4 =48V. The V_{max} of the output voltage is calculated by

$$V_{max} = V_1 + V_2 + V_3 + V_4 \quad (1)$$

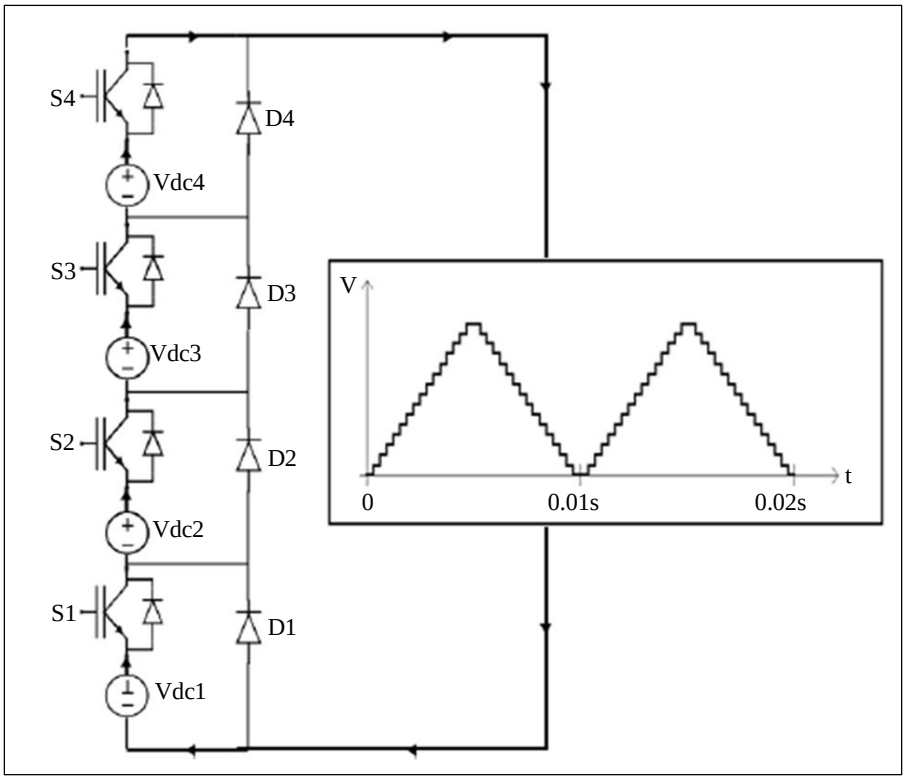

Fig. 2 Level generator circuit

Table 1. Switching states of proposed 31-level inverter

S. No.	Switching States	Conducting Switches	Conducting Diode	Voltage Levels	Output
1	I	-	-	0	0
2	II	S1	D2,D3,D4	$+1V_{dc}$	+6V
3	III	S2	D1,D3,D4	$+2V_{dc}$	12
4	IV	S1,S2	D3,D4	$+3V_{dc}$	18
5	V	S3	D1,D2,D4	$+4V_{dc}$	24
6	VI	S1,S3	D2,D4	$+5V_{dc}$	30
7	VII	S2,S3	D1,D4	$+6V_{dc}$	36
8	VIII	S1,S2,S3	D4	$+7V_{dc}$	42
9	IX	S4	D1,D2,D3	$+8V_{dc}$	48
10	X	S1,S4	D2,D3	$+9V_{dc}$	54
11	XI	S2,S4	D1,D3	$+10V_{dc}$	60
12	XII	S1,S2,S4	D3	$+11V_{dc}$	66
13	XIII	S3,S4	D1,D2	$+12V_{dc}$	72
14	XIV	S1,S3,S4	D2	$+13V_{dc}$	78
15	XV	S2,S3,S4	D1	$+14V_{dc}$	84
16	XVI	S1,S2,S3,S4	-	$+15V_{dc}$	90

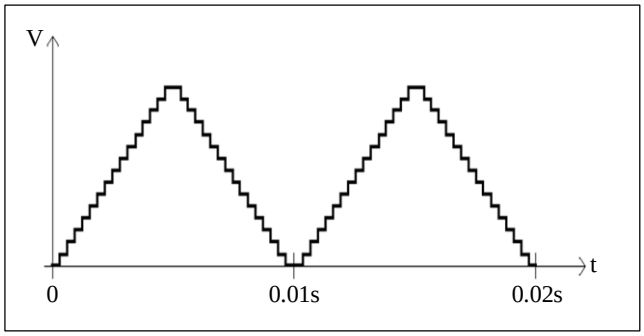

Fig. 3 Sample output voltage waveform of level generator circuit

The level generator is used to create the outputs only in the positive output voltage. As a result, the level generator produces output voltage with a maximum amplitude (Vmax) of 90V. When all switches are in off conditions, then the output will be zero. The other voltage levels are obtained by proper switching between the switches. Here, the bypassed diode technique is used to attain the necessary voltage level. Table 1 describes the switching pattern of the level generator.

2.2. H-Bridge Inverter Circuit

The H bridge inverter is a standard single-phase inverter. The level generator output voltage is always zero and only positive. The output of the level generator acts as input to the H-bridge inverter. The purpose of the H-bridge is to convert the positive output levels from the level generator to positive and negative levels. This is achieved by employing a H-bridge inverter. The structure of an H-bridge inverter consists of four switches: H1, H2, H3, and H4. When the switches H1 and H3 come on, then the output is positive. Likewise, the switches H2 and H4 are turned on to produce negative output. Zero level is achieved when all the switches are in off condition. For one fundamental period, the switches of the H-bridges are on and off only once. Also, the switches need to handle high voltage. Therefore, the switches must operate at high voltage with less switching frequency. Thus, the 31-level output is achieved at the output. The output voltage is illustrated in the Figure 4.

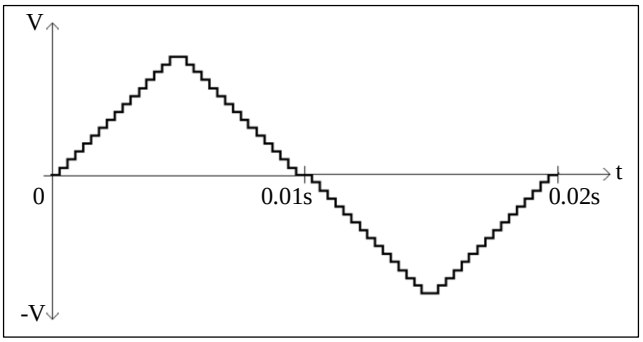

Fig. 4 Sample 31 level output voltage waveform of H-Bridge inverter circuit

The output voltage of the proposed 31-level MLI is the sum of voltages generated by the DC sources. Let "S" be the number of DC sources then the output voltage level is given by using the equation,

$$No.of levels = 2^{S+1} - 1 \quad (2)$$

The equation gives the number of switches,

$$No.of Switches = S + 4 \quad (3)$$

The equation gives the number of bypassed diodes,

$$No.of Diodes = S \quad (4)$$

If S =4, then No. of levels =31, No. of switches =8, No. of Diodes = 4.Hence, the corresponding circuit structure will be the 31-level proposed topology, which is shown in Figure 1. Table 2 describes the comparison of the circuit components used in the proposed hybrid multilevel inverter with the conventional multilevel inverter types.

Table 2. Comparison of proposed with conventional MLI

Circuit Components	Diode Clamped Multilevel Inverter	Flying Capacitor Multilevel Inverter	Asymmetrical Cascaded H-Bridge Inverter	Symmetrical Cascaded H-Bridge Inverter	Proposed Hybrid 31-Level Inverter
Main Switching Devices	60	60	60	60	8
Main Diodes	-	-	-	-	4
Clamping Diodes	870	-	-	-	-
DC Bus Capacitor	30	30	15	4	-
Balancing Capacitor	-	435	-	-	-
DC Input Sources	1	1	15	4	4

From the table it is clear that the proposed MLI uses minimum no of components to produce 31 levels at the output. Thus, the structure can be realized with low cost and the size of the MLI is small compared to the conventional MLI.

3. Modulation Techniques

The primary goal of the multilevel inverter's modulation approach is to produce an output voltage that is similar to a sinusoidal waveform.

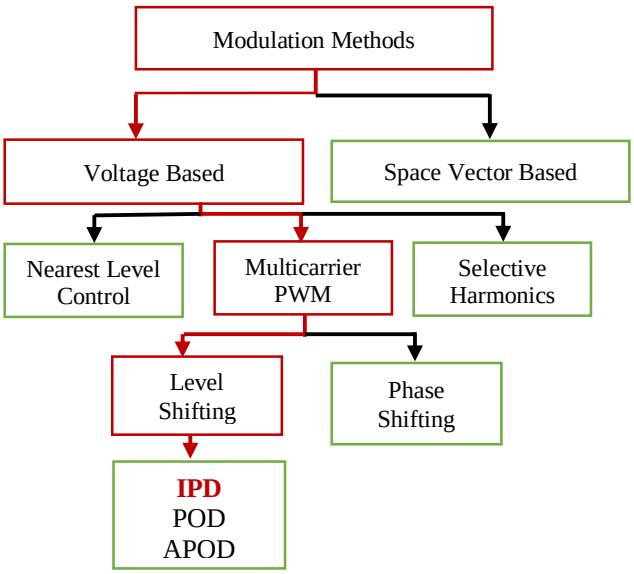

Fig. 5 Different modulation strategies

In order to minimize switching loss and reduce harmonics, numerous modulation schemes have been established. Based on changing frequency, the modulation techniques employed in multilevel inverters can be categorized, as shown in Figure 5. Power semiconductors can undergo a lot of commutations using techniques that operate at high switching frequencies during a single period of the fundamental output voltage. The traditional carrier-based Sinusoidal PWM (SPWM), which employs the phase-shifting technique to minimize the harmonics in the load voltage, is a widespread technique used in industrial applications.

3.1. Level Shifting PWM

In the present investigation it explores several kinds of multilevel sine-triangle PWM and measures their effectiveness under optimum operating conditions. For level-shifted multicarrier modulation, there are three possible PWM techniques with differing phase relationships:

a. In-Phase Disposition (IPD) - the carriers are in phase with each other.
b. Phase Opposition Disposition (POD) - a phase difference of 180˚ for carriers above and below the zero reference.
c. Alternate Phase Opposition Disposition (APOD) - neighboring carriers are out of phase with each other at 180˚.

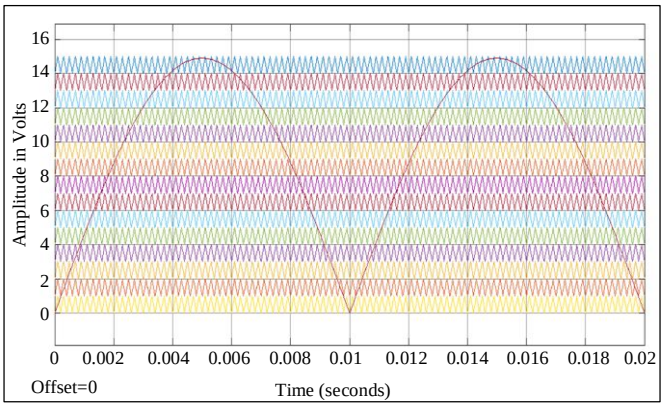

Fig. 6 Multicarrier IPD PWM waveform

The proposed hybrid multilevel inverter structure used the In-Phase Disposition method to create the gate signals of the inverter. The sine and the carrier waveforms are shown in Figure 6.

4. Fault Analysis

This article deals with the fault analysis of a 31-level inverter. In general, the faults may be due to many reasons. Of these, the most popular are due to,

1. Defective switches in manufacturing.
2. Problems with the quality of the material used in the semiconductors.
3. Failure of the interfaces due to mechanical destructions.
4. Incorrect switching signals provide incorrect turn on and turn off creating inappropriate results.
5. Failure due to the increase in temperature.

Due to these reasons, the switch failure is caused by two types of faults, namely open circuit fault and short circuit fault. Here, the open circuit fault is analyzed. Fault analysis occurs in three stages.

1. Identification of fault
2. Isolation of faulty switch
3. Fault compensation

4.1. Identification of Fault

The first step of fault analysis deals with the identification of fault. When the output signal is lacking in some of the stages of output confirms that the system suffers from OC or SC fault.

4.2. Isolation of Faulty Switch

The second stage is fault isolation. The isolation of the faulty component is necessary in order to maintain the functionality of the circuit and to avoid the malfunction of the entire system. Generally, fault isolation can be attained by modulation-based or hardware-based [17]. The isolation of the defective components is done by using additional components such as TRIACs [33-35] and fuses [36]. This structure uses a switch to isolate the faulty component.

4.3. Fault Compensation

Generally, fault compensation is done in two categories. Either the compensation backup switch is connected or by implementing the backup switching technique. For analysis purposes, we adapt the fault compensation by using the backup axillary switch. This type of auxiliary switch compensation may increase the number of switching devices. Since the no of components is increased, creating an increase in the complexity of the circuit, size, cost and weight of the system. The action of fault compensation is necessary in order to achieve the regular operation of the system.

4.4. Fault-Tolerant Analysis in Proposed Multilevel Inverter

The fault-tolerant system of the 31-level single-phase inverter is shown in the Figure 7. The fault-tolerant system consists of the following subsystems. They are,

1. Injection of fault by a slider switch
2. Fault control system
3. Fault Isolation and compensation unit

4.4.1. Injection of Fault by a Slider Switch

The figure illustrates the fault injection block. This system is realized by using the slider switches. Each switch state is demonstrated with the help of a slider switch.

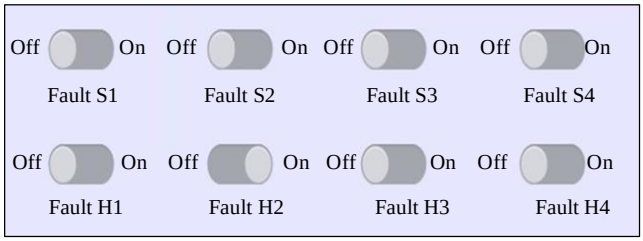

Fig. 7 Injection of fault by slider switch block

Eight slider switches are used to create the fault injection unit. There are two possible states of a switch: a healthy state and a faulty state. Signal 1 represents the healthy state, whereas the signal 0 represents the defective state. The state is changed in the simulation by sliding the switch from one state to another.

4.4.2. Fault Control Unit

Figure 8 illustrates the circuit of the fault control block. Here, the fault control is created separately for each switch present in the proposed circuit. The level generator consists of four IGBTs, and the H bridge also consists of another 4 IGBTs. Hence, the fault control unit has eight identical systems created for each IGBT. The fault control receives the signal from the injection of fault by the slider switch unit. The control signal maybe 1 or 0, depending upon the state of fault. Signal 0 indicates the fault state of a switch, whereas signal 1 represents the healthy state of a switch. If it receives signal one, then the control unit allows signal 1 to the isolation unit, demonstrating that the switch is in a healthy state. If it gets the signal 0, then it sends a step signal to the isolation unit to indicate that the switch is in a faulty state and it needs to be isolated. The step signal is nothing but a signal 0 with a specified time delay.

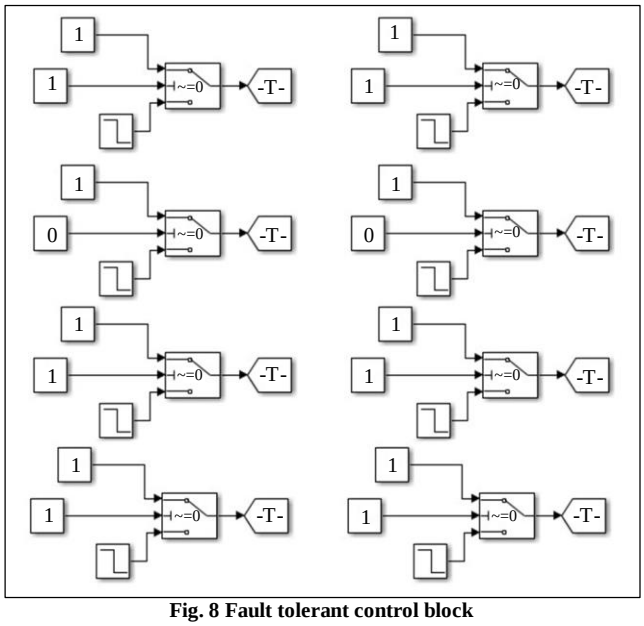

Fig. 8 Fault tolerant control block

4.4.3. Fault Isolation and Compensation Unit

The purpose of this unit is to identify the location of the faulty switch and need to isolate the faulty switch. Then, the next step is to make the backup secondary switch come into one state.

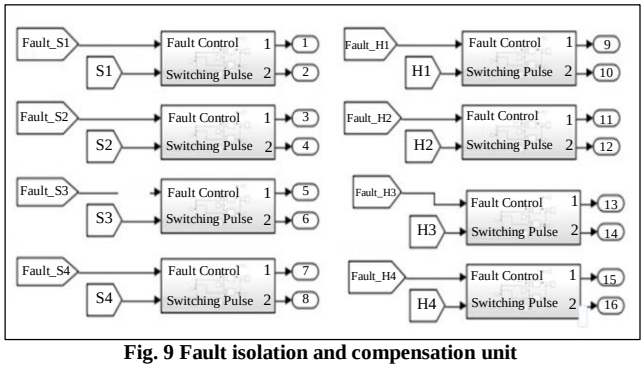

Fig. 9 Fault isolation and compensation unit

In this unit also uses separate subsystems for each IGBT. Here, it consists of 8 subsystems. This unit receives input from the generation of switching signals unit and the fault control unit. In the healthy state, the primary IGBT is turned on with the help of the switching signals. Under faulty state, it is necessary to locate the defective switch and isolate it by making the gate signal of the faulty switch zero also, it is necessary to turn on the secondary IGBT associated with the defective switch for regular operation.

The fault switching model is shown in Figure 10. It consists of a constant zero input, a fault control signal, and the gate signals to the switches. Under normal operation, the

switch is in a healthy state, so the fault signal provides the gate signals to the primary IGBT and sequentially turns off the secondary IGBT with the gate signal 0. Under an open circuit fault, the fault control signal is 0, indicating the faulty state of a switch; then, this unit isolates the faulty switch by applying a 0 gate signal to the primary IGBT. At the same time, the backup redundant IGBT is turned on by using the gate signal with some time delay like that of the practical case. Figure 11 illustrates the complete structure of the Hybrid Multilevel Inverter, producing 31 levels at the output with fault-tolerant capability. The fault compensation is achieved by adding standby auxiliary switches in parallel with the main switches of the level generator as well as the H-bridge inverter of the proposed circuit.

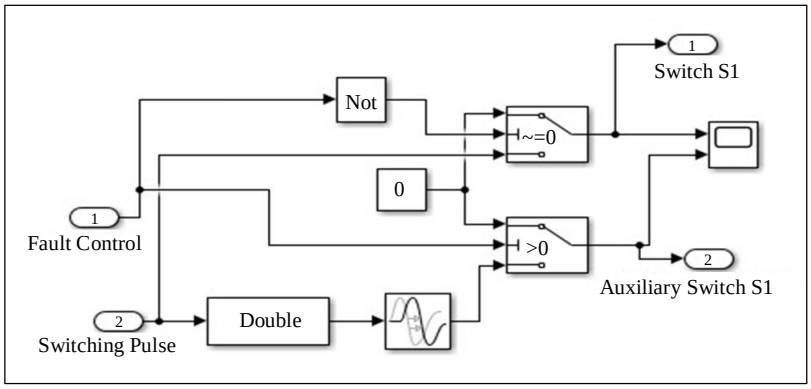

Fig. 10 Fault tolerant control switching model

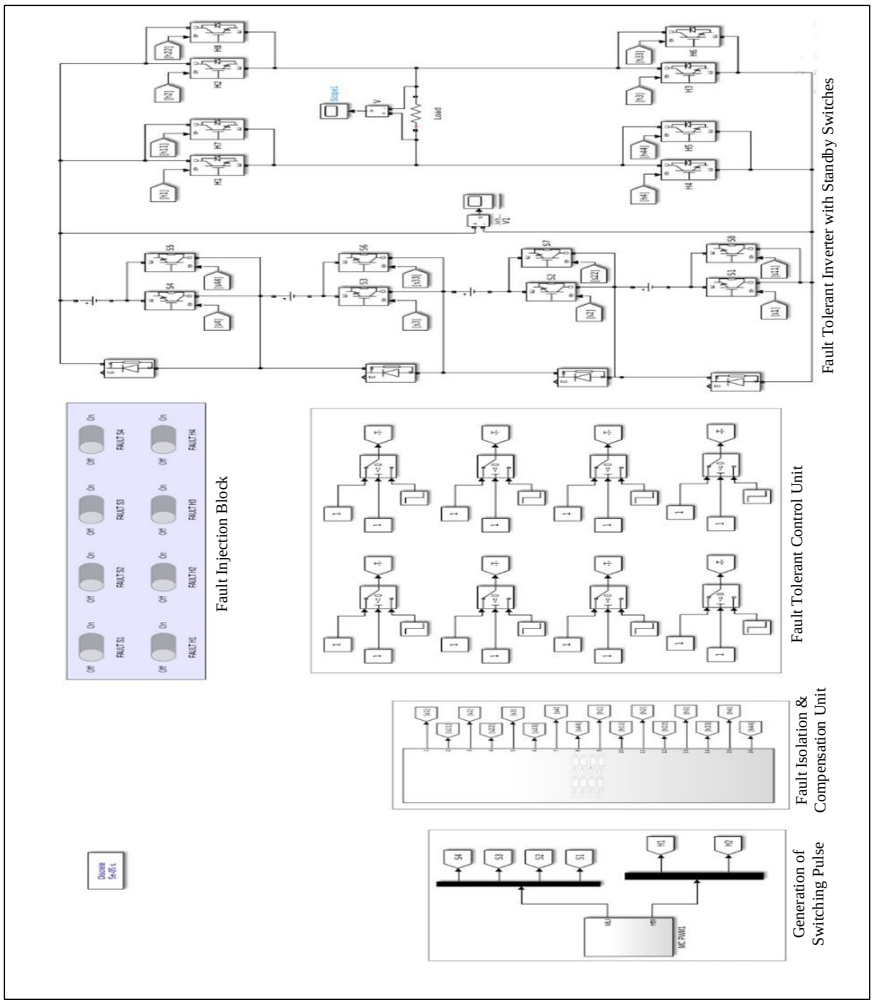

Fig. 11 Proposed fault tolerant 31-level hybrid multilevel inverter

5. Results and Discussion

To check the fault-tolerant capability of the proposed multilevel inverter, the analysis is carried out with a single switch fault and two switch faults.

6. Normal Operation

During normal operation of the inverter, it produces 31 levels at the output. The switching table of the proposed inverter is given in Table 1.

The gate pulses are produced with the S-PDPWM technique, and the carrier signals are shown in Figure 12. It conveys that during regular operation, only the main switch is turned on where as the auxiliary switch remains at off condition.

The output voltage with multiple levels (31 levels) is illustrated in Figure 13. In the Simulation, we achieved the voltage of maximum amplitude (Vmax) as 86V.

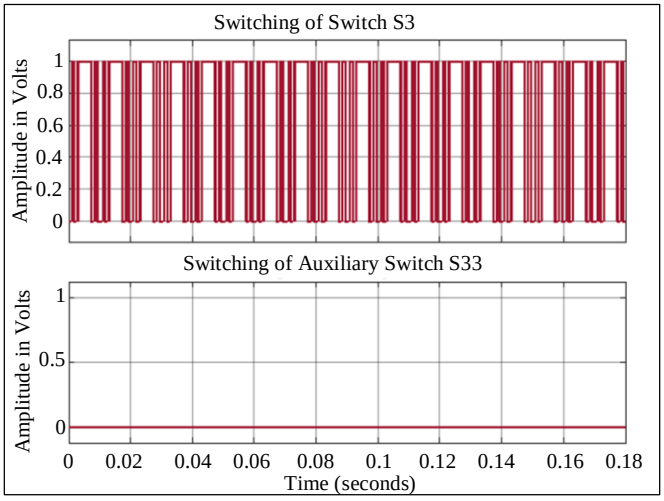

Fig. 12 Switching pulse of switch S3 in normal operation

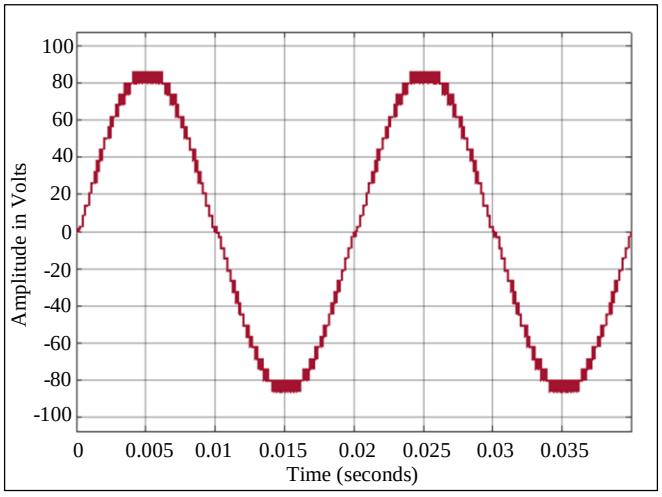

Fig. 13 31-level output voltage waveform

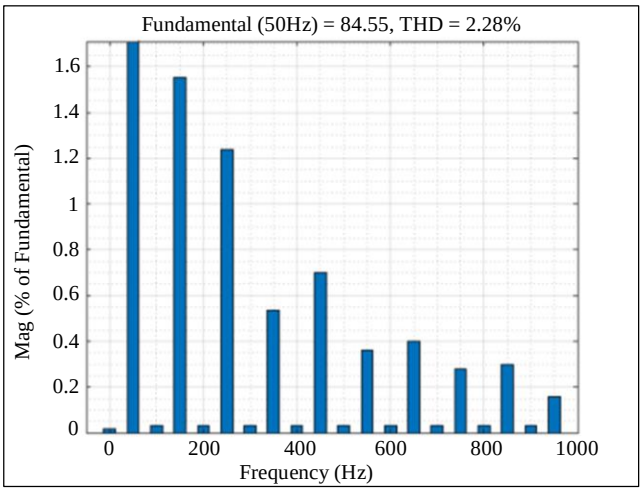

Fig. 14 THD during normal operation

The Total Harmonic Distortion of the output voltage is calculated by using FFT analysis in MATLAB/Simulink. The THD of 2.28% is achieved in the Simulation and is shown in Figure 14.

6.1. Single Swicth Fault Analysis

The proposed circuit consists of two parts. Level generator with four switches S1, S2, S3, and S4 and H-bridge inverter with four switches H1, H2, H3 and H4. So, the analysis occurs in two cases.

6.1.1. Fault in Switches of Level Generator

Fault in Switch S1

When the fault occurs in S1, the switching pulse is generated in the following manner. At first, the gate pulse of switch S1 turns to zero at 0.06sec. After some time delay the auxiliary switch associated with the switch S1 is turned on for fault compensation. The fault compensation occurs at 0.12s. The faulty state happens at the interval 0.06s to 0.12s. The switching pulse is shown in Figure 15.

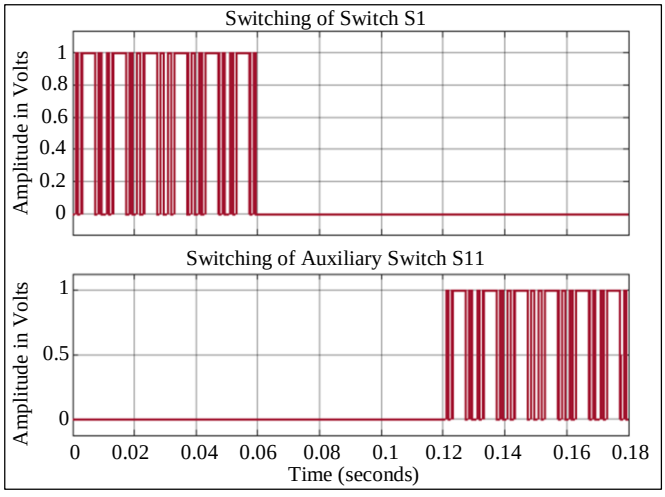

Fig. 15 Switching to switch S1 and auxiliary switch S11

Under fault at S1, the inverter produces 15 levels at the output. The output voltage waveform is given in the Figure 16. The THD is calculated for three cases. Before fault, with fault, and after fault compensation.

The THD before and after fault compensation is 2.28%, which is the same as that of the normal operation condition. Under fault at switch S1, the circuit produces 15 levels at the output with a THD of 4.62%.

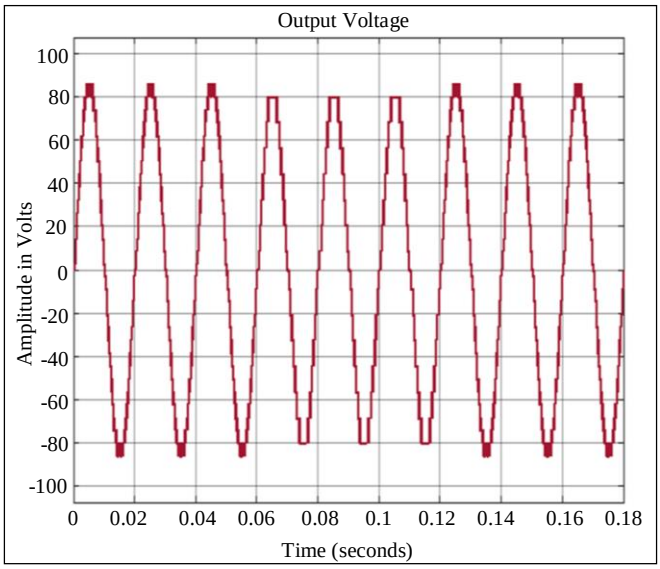

Fig. 16 Simulation of fault in switch S1 under normal, faulty, and fault compensated mode

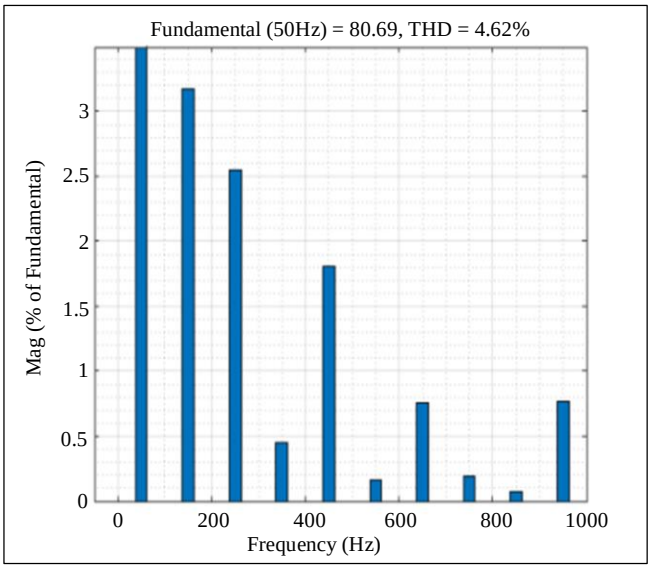

Fig. 17 THD when switch S1 is under fault

Fault in Switch S2

When the fault occurs in switch S2, the DC voltage source associated with S2 is open-circuited, thus producing the seven levels at the output voltage. The THD is calculated as 8.97% at the faulty period.

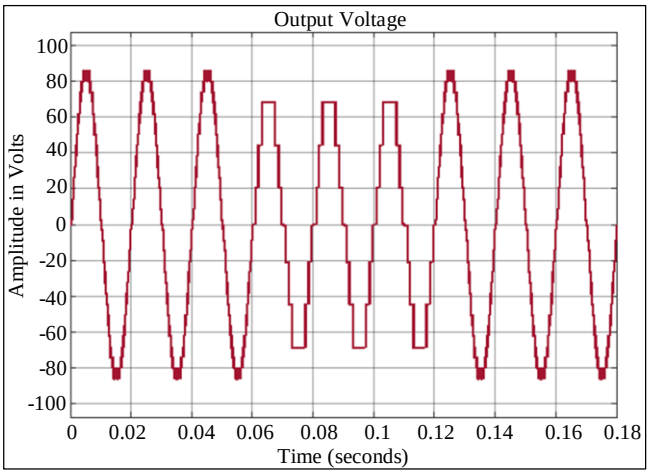

Fig. 18 Simulation of fault in switch S2 under normal, faulty, and fault compensated mode

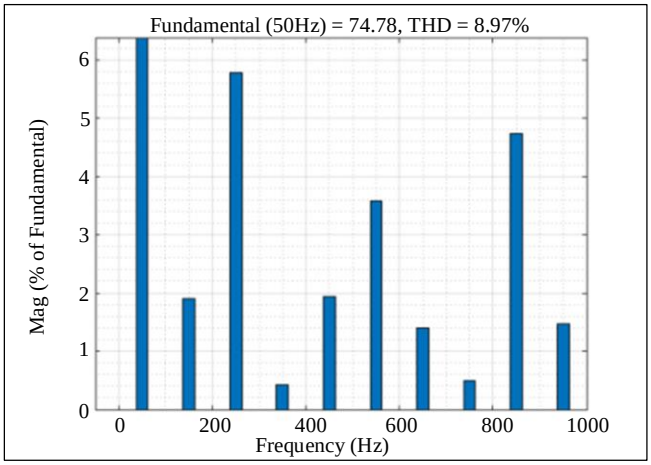

Fig. 19 THD when switch S2 is under fault

Fault in Switch S3

When the fault occurs in switch S3, the DC voltage source associated with S3 is open-circuited, thus producing the output waveform as shown in Figure 20.

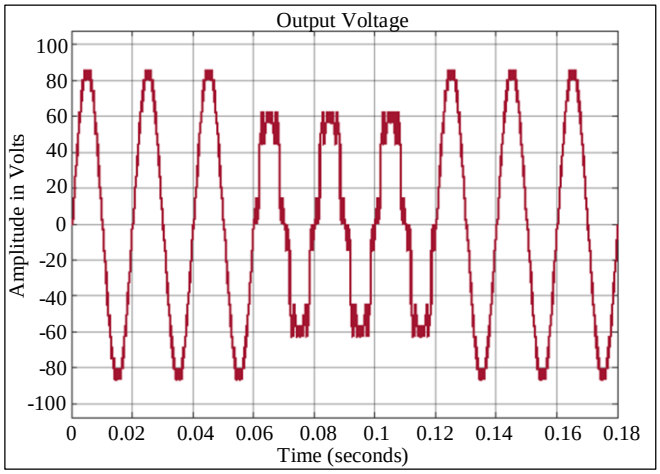

Fig. 20 Simulation of fault in switch S3 under normal, faulty, and fault compensated mode

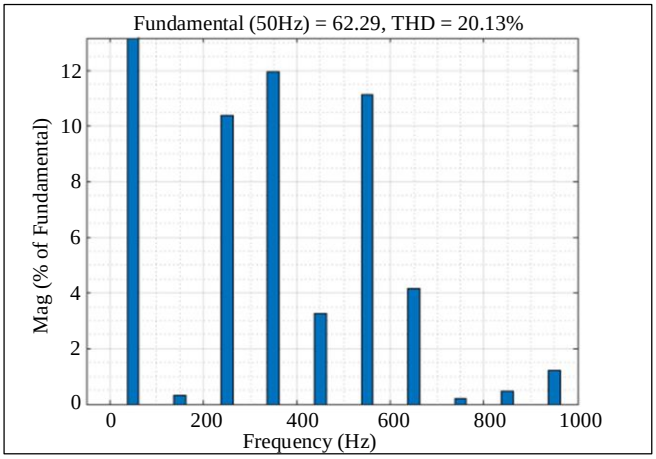

Fig. 21 THD when switch S3 is under fault

Figure 20 illustrates that the output voltage waveform is distorted when switch S3 suffers from a fault. The THD is obtained as 20.13%.

Fault in Switch S4

When the fault occurs in switch S4, the DC voltage source associated with S4 is open-circuited thus producing the output voltage waveform as shown in Figure 22.

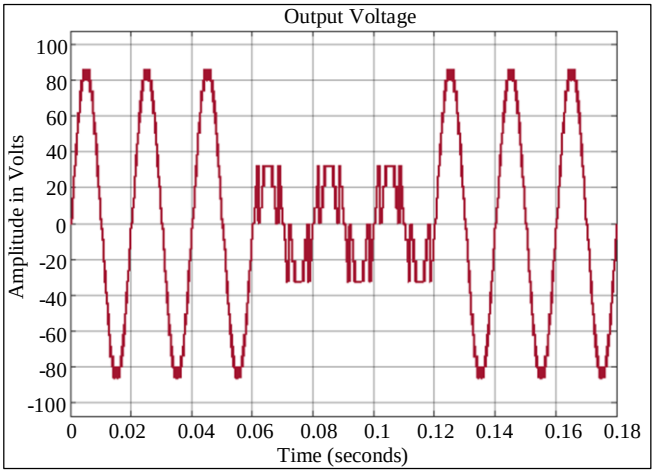

Fig. 22 Simulation of fault in switch S4 under normal, faulty, and fault-compensated mode

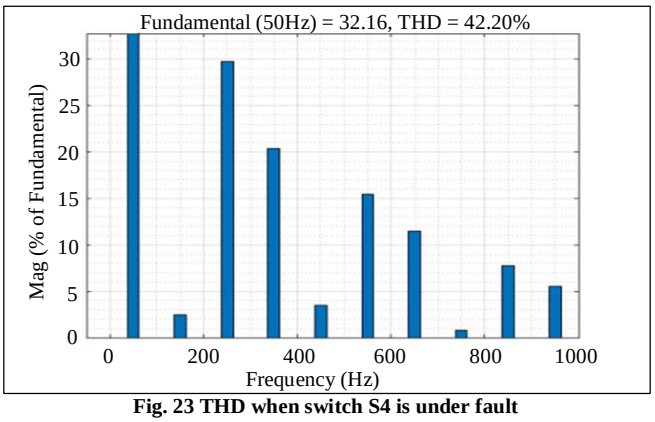

Fig. 23 THD when switch S4 is under fault

Figure 22 demonstrates that the output voltage waveform is heavily distorted during a fault at switch S4. The switch S4 is associated with a high value of DC source; hence, it suffers more. Since the distortion is heavy, the THD is obtained as 42.20%, which is considerable.

6.1.2. Fault in Switches of H-Bridge Inverter

The open circuit fault analysis of the h bridge inverter is examined through Simulation, and the results are illustrated.

Fault in Switch H1

The switch H1 is subjected to an open circuit fault. When H1 is in fault mode, the output produces only negative voltage levels at the output, causing drastic changes in the output levels.

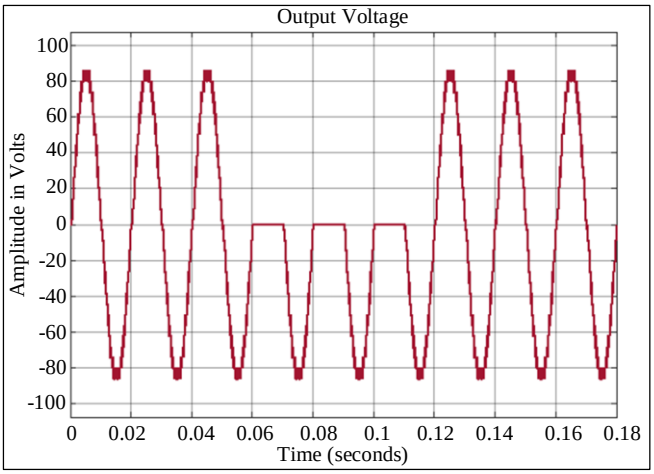

Fig. 24 Simulation of fault in switch H1 under normal, faulty, and fault-compensated mode

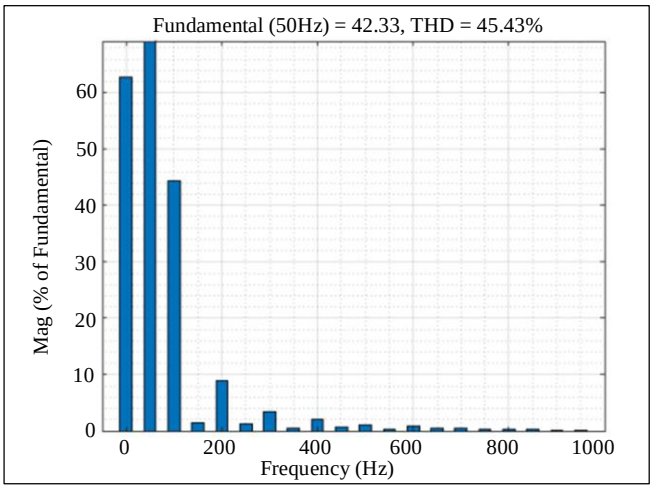

Fig. 25 THD when switch H1 is under fault

Fault in Switch H2

The switch H2 is subjected to an open circuit fault. When H2 is in fault mode, the output produces only positive voltage levels at the output, causing drastic changes in the output levels.

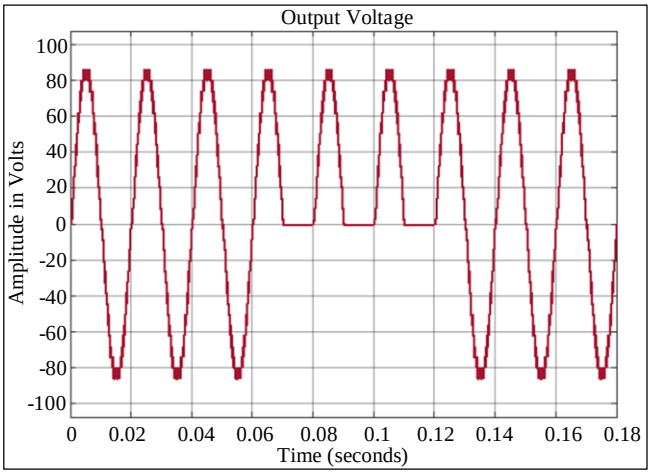

Fig. 26 Simulation of fault in switch H2 under normal, faulty, and fault-compensated mode

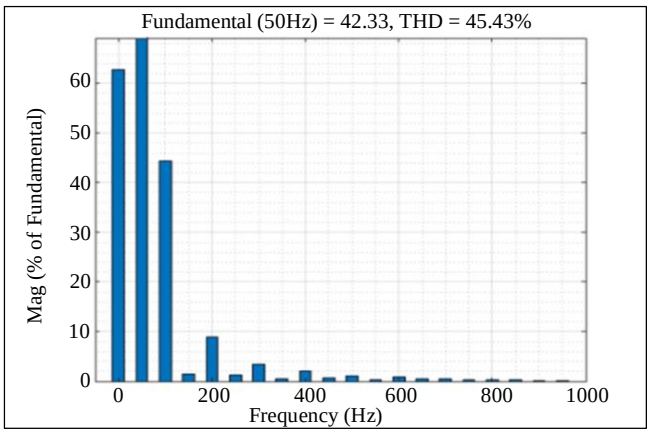

Fig. 27 THD when switch H2 is under fault

Fault in Switch H3

The switch H3 is subjected to an open circuit fault. When H3 is in fault mode, the output produces only negative voltage levels at the output, causing drastic changes in the output levels.

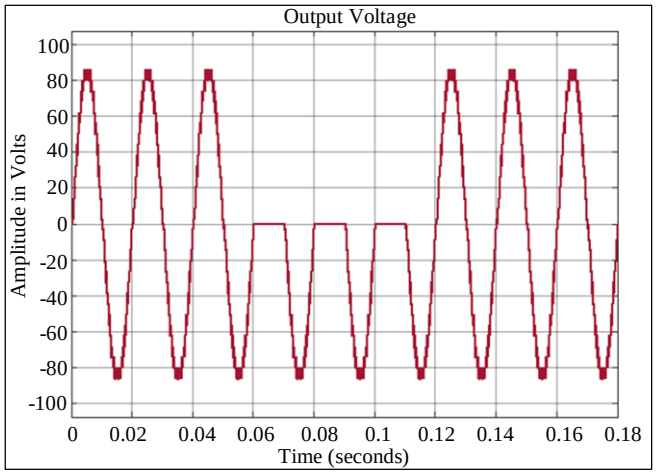

Fig. 28 Simulation of fault in switch H3 under normal, faulty, and fault-compensated mode

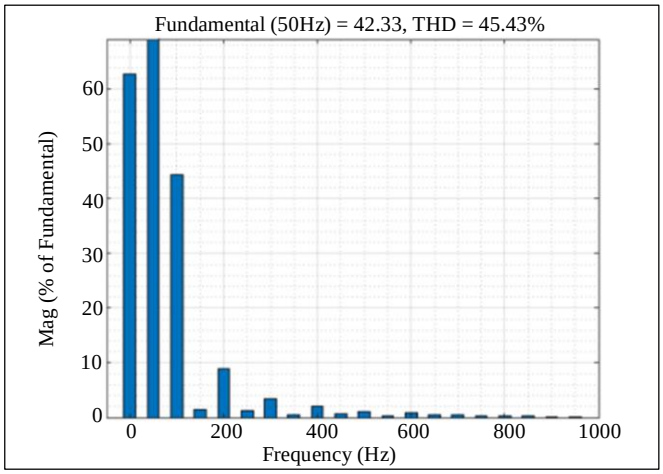

Fig. 29 THD when switch H3 is under fault

Fault in Switch H4

The switch H4 is subjected to an open circuit fault. When H4 is in fault mode, the output produces only positive voltage levels at the output, causing drastic changes in the output levels.

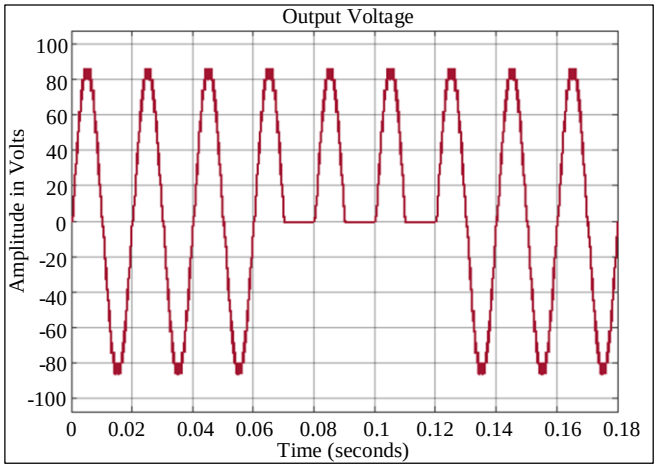

Fig. 30 Simulation of fault in switch H4 under normal, faulty, and fault-compensated mode

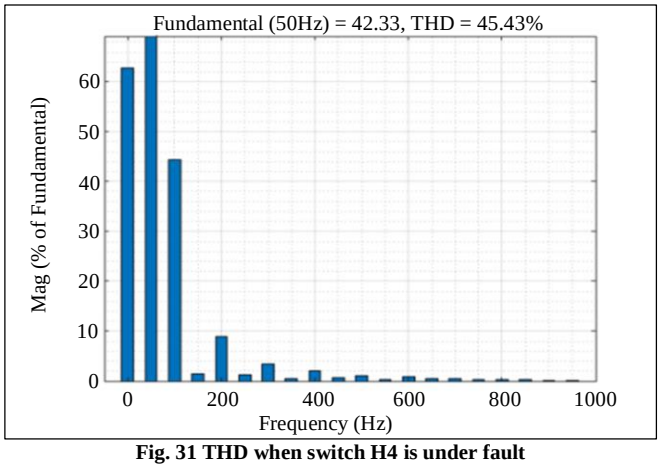

Fig. 31 THD when switch H4 is under fault

From the results, it is evident that when the fault occurs in H1 as well as in H3, in both cases it produces only negative voltage levels. Under fault at H2 as well as at H4, in both cases, it produces only positive voltage levels. THD is very large due to the absence of voltage levels at the output.

6.1.3. Multiple Switch Fault

In this examination, only the level generator of the proposed multilevel inverter is examined with two switch faults.

Fault in Switch S1S2

In this case, at a particular period both the switch S1 and S2 are subjected to open circuit fault. When both switches are faulted, the circuit produces the output with seven voltage levels. Since two switches are faulted, the THD is 10.60%. From the results, it is clear that even though switches S1 and S2 are faulted, it is capable of producing multilevel output.

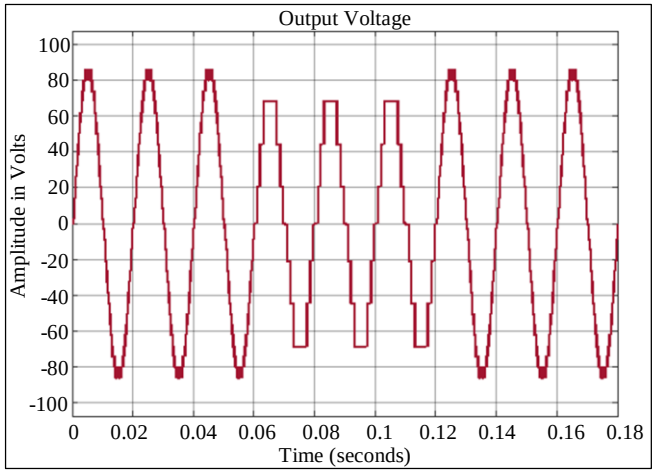

Fig. 32 Simulation of fault at switches S1 and S2 under normal, faulty, and fault-compensated mode

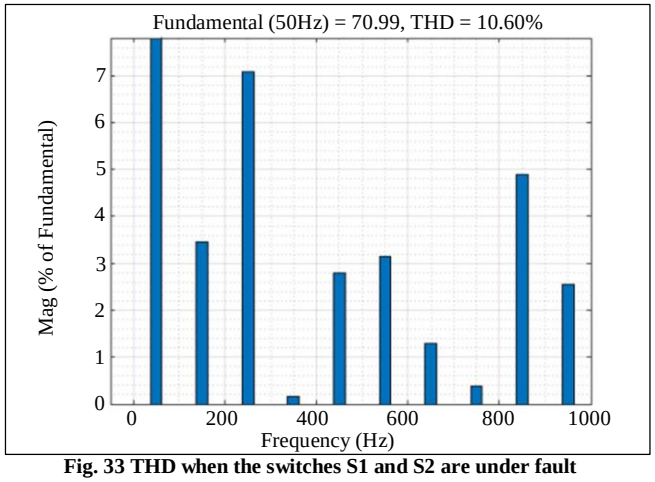

Fig. 33 THD when the switches S1 and S2 are under fault

Fault in Switch S1S3

In this case, at a particular period both the switch S1 and S3 are subjected to open circuit fault. When both switches are faulted, the circuit produces the output with five voltage levels. The power quality is low since the duration of the output voltages is different. The width and height of the output voltage levels are different, causing high THD.

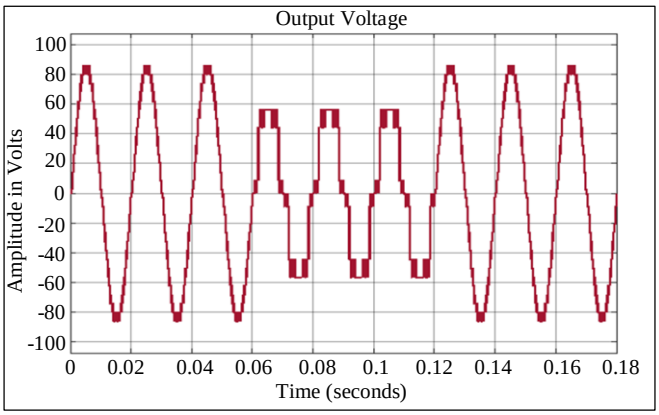

Fig. 34 Simulation of fault at switch S1 and S3 under normal, faulty, and fault-compensated mode

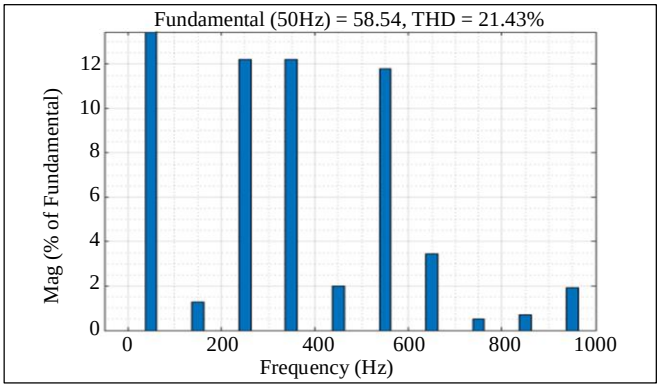

Fig. 35 THD when the switches S1 and S3 are under fault

Fault in Switch S1S4

In this case, at a particular period both the switch S1 and S4 are subjected to open circuit fault. The output voltage waveform during faulty conditions is shown in Figure 36. Since the output waveform suffers from significant distortions, the THD is large.

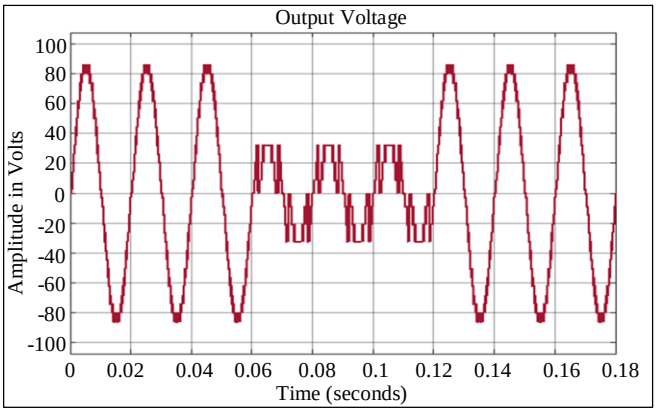

Fig. 36 Simulation of fault at switches S1 and S4 under normal, faulty, and fault-compensated mode

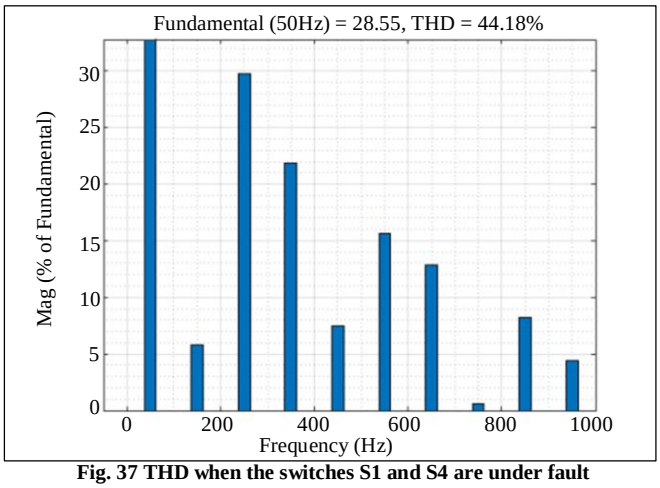

Fig. 37 THD when the switches S1 and S4 are under fault

Fault in Switch S2S3

In this case, at a particular period both the switch S2 and S3 are subjected to open circuit fault. The output voltage waveform during faulty conditions is shown in Figure 38.

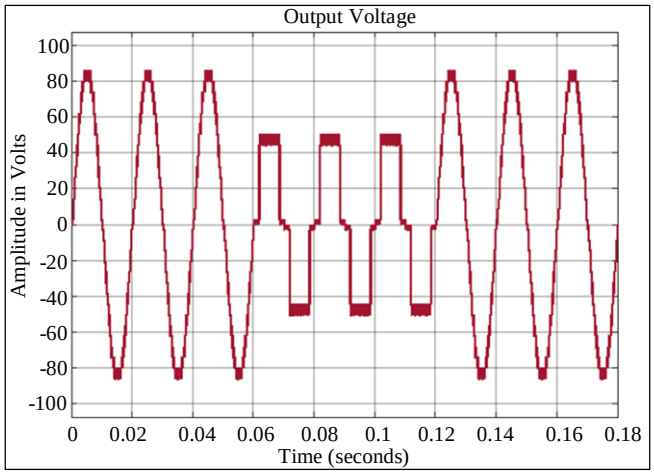

Fig. 38 Simulation of fault at switch S2 and S3 under normal, faulty, and fault-compensated mode

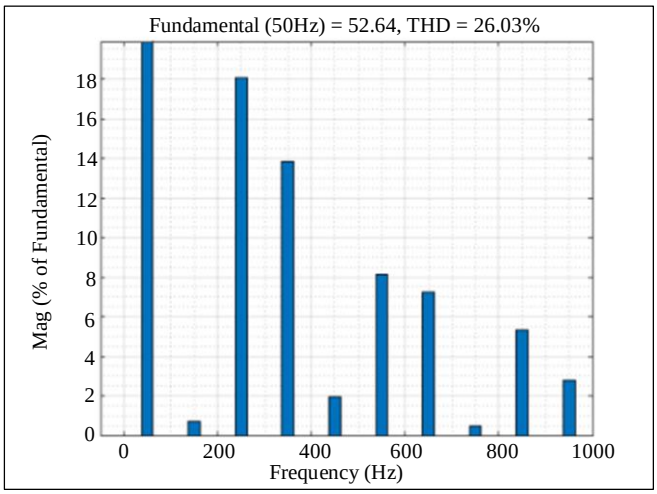

Fig. 39 THD when the switches S2 and S3 are under fault

Fault in Switch S2S4

In this case, at a particular period both the switch S2 and S4 are subjected to open circuit fault. The output voltage waveform during faulty conditions is shown in Figure 40.

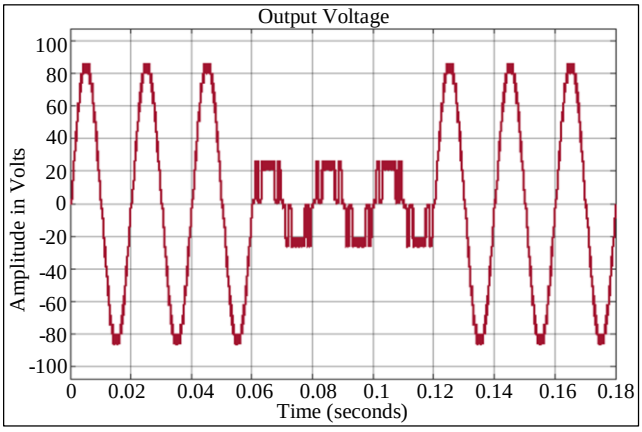

Fig. 40 Simulation of fault at switch S2 and S4 under normal, faulty, and fault-compensated mode

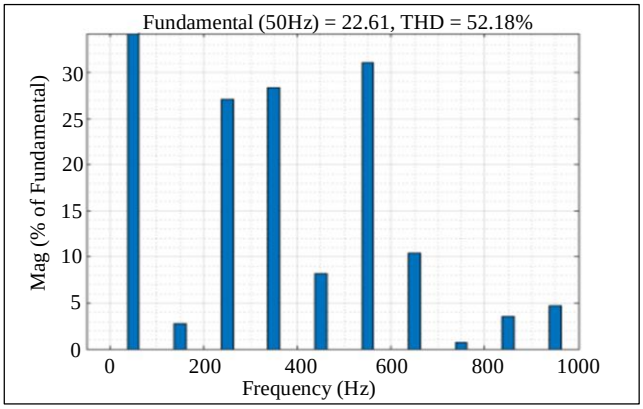

Fig. 41 THD when the switches S2 and S4 are under fault

Fault in Switch S3S4

In this case, at a particular period both the switch S3 and S4 are subjected to open circuit fault. The output voltage waveform during faulty conditions is shown in Figure 42.

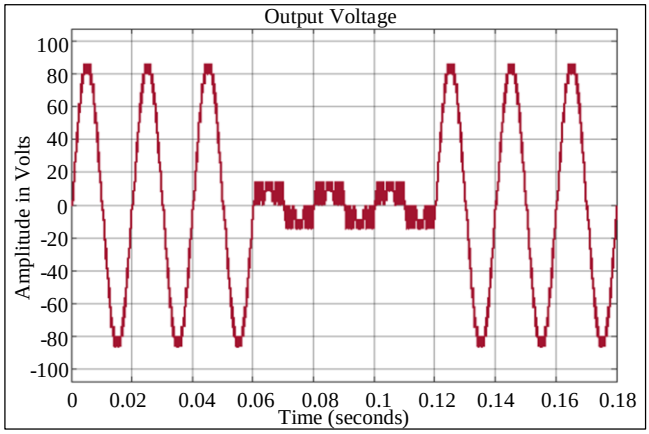

Fig. 42 Simulation of fault at switch S3 and S4 under normal, faulty, and fault-compensated mode

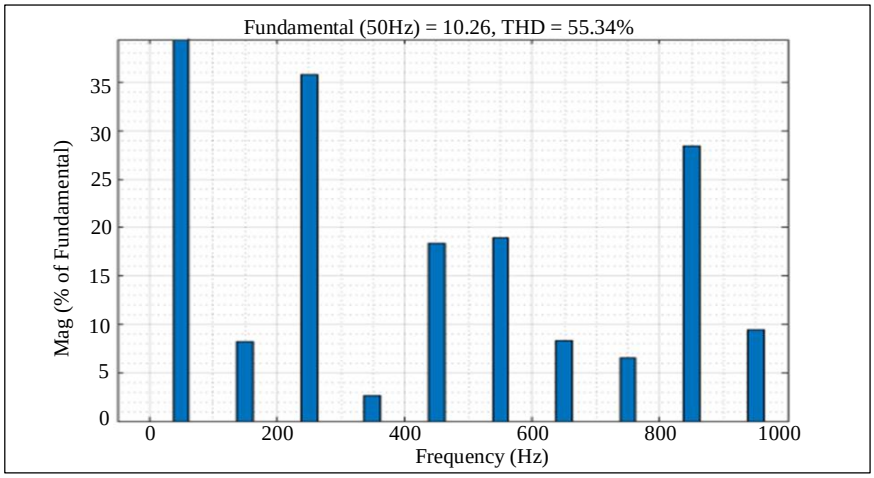

Fig. 43 THD when the switches S3 and S4 are under fault

Table 3. Comparison of fault tolerant MLI with proposed fault tolerant MLI

Reference Paper	Type of MLI	No. Output Levels	No. of Power Switches	THD
[31]	Hybrid MLI	5	14	-
[32]	Modular Multilevel Converter	9	8	-
[37]	Cascaded Switched Capacitor MLI	9	9	-
[38]	Cascaded H-Bridge MLI	7	24	18%
[39]	Hybrid MLI	7	12	-
Proposed	Hybrid Cascaded H Bridge	31	8	2.28%

Table 3 shows the comparison of no of components used in the fault-tolerant MLI. From this, it is understood that for 31 levels, the proposed fault-tolerant MLI structure used less no of components.

Many factors, including a malfunctioning gate motor, a heat-related break in the circuit's interior connection, and a lifted wire from the circuit, might result in an open circuit issue. When an open circuit fault happens, the components are under more stress, which leads to further issues. Low power quality is also caused by significant THD from the OC problem. When a system is fault-tolerant, more backup auxiliary switches are installed to make up for the failure. Furthermore, the components used here are very minimal.

7. Conclusion

The fault-tolerant 31-level inverter structure is proposed and evaluated using Simulation. The circuit comprises 16 switches, 4 diodes, and four separate DC sources. Of these, the 8 Switches act as the backup auxiliary switches which are connected in parallel with the main switches. If the fault occurs at the main switch, then the associated auxiliary switch comes to an on state in order to compensate for the fault that occurred. Here, Single-switch faults and multiple-switch faults are analyzed. The proposed circuit works well in fault-tolerant mode, and the THD calculated during fault mode is tabulated in the Table 4.

Table 4. THD values during fault mode

Faulty Switch	THD (%)
No fault	2.28
S1	4.62
S2	8.97
S3	20.13
S4	42.20
H1	45.43
H2	45.43
H3	45.43
H4	45.43
S1S2	10.60
S1S3	21.43
S1S4	44.18
S2S3	26.03
S2S4	52.18
S3S4	55.34

From the above table, it is evident that if the fault occurs on the lower stages of the switches S1 and S2, the degradation is low. If the fault occurs on a higher order of switches, such as S3 and S4, then the power quality is very low. In the case of the H-bridge inverter, it is noted that fault should be avoided in the H-bridge for proper operation of the proposed circuit. In case of multiple switch faults, whenever the switch S3 and S4 are faulted the distortion is more than that of switch S1 and S2. Also, controllers can be employed so that the total harmonic distortion can be further controlled in the future.

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