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Original Article

Efficient Design of Ripple Carry Adder with No-Crossover using an Optimized and Scalable QCA Full-Adder

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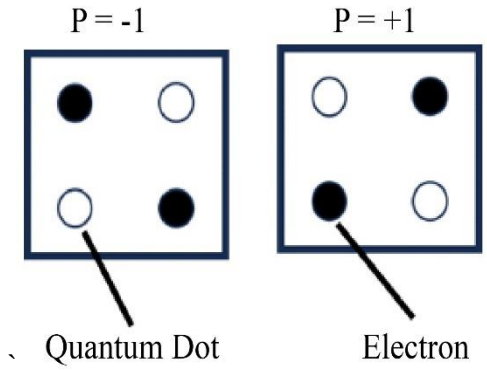
Abstract *- QCA has emerged as a leading nanocomputing technology and is positioned as a substitute for CMOS VLSI technology. This study presents an optimal and scalable coplanar QCA Full Adder with No-Crossover (QFANC) design using a Modified XOR gate (MXOR) structure that contains a part of the majority gate. The proposed QFANC design utilizes 13 QCA cells and is employed to efficiently design QCA Ripple Carry Adder circuits with no-crossover (QRCANC) with input sizes of 4-bit and 8-bit to demonstrate its scalability. The simulation and functional verification are performed using the QCA Designer (v2.0.3) tool. Energy dissipation of proposed designs and equivalent QFAs reported in the literature is estimated using the QCA Designer-E tool. Comparative analysis across various metrics implies that the suggested QFANC design is optimal with a reduction of 15% in area, 7% in cell complexity, and 3% in energy dissipation associated with the finest scalable QFA design reported.*

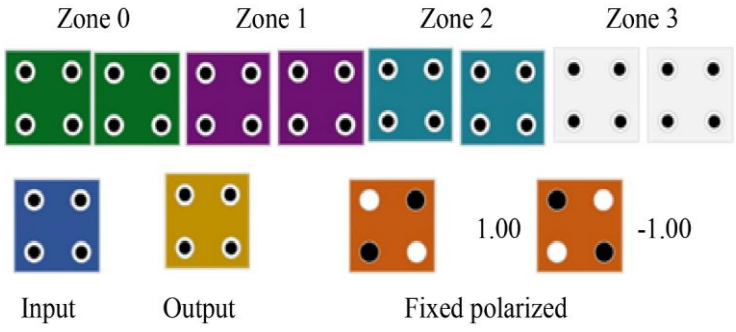
Keywords *- Coplanar, No-crossover, Scalability, QCA Full Adder (QFA), QCA RCA (QRCA), Quantum dot Cellular Automata (QCA).*

1. Introduction

In 1993, Quantum-dot Cellular Automata (QCA), a nanotechnology-based computing method, was first introduced by Lent et al. [1], which operates by allowing QCA cells to communicate with each other [2]. This innovation empowered a small-scale, low-power digital circuit design with diminished latency. A standard QCA cell uses four quantum dots placed at the square's corners. Because the two electrons repel each other, they tunnel into and occupy antipodal dots [3]. Figure 1 (a) illustrates the two possible stable electron polarizations, P= +1 and P= -1 symbolizing binary values logic '1' and '0' [4]. The switching action of a cell between these two logic states is affected by the coulombic interaction of adjacent cells [5]. In QCA design, any Boolean function can be realized by employing three essential primitives: the binary wire, the Majority voter, and the inverter gate [6]. To apply clocking, QCA circuits are structured into clock zones, and cells in each zone are sequentially assigned to one of four clock phases [7]. The various representations of the QCA cells based on the purpose they are used for are depicted in Figure 1 (b). Wire crossing enables multiple QCA wires to intersect without interaction or interference, and it remains a crucial aspect of QCA architecture for realizing complex digital circuits. Three types of crossover techniques have been used so far in QCA design: Multilayer, Coplanar, and Clock-zone based crossover. In the Multilayer technique, wire crossing occurs on separate physical layers, enabling wires of the same cell type to intersect as long as adequate vertical separation is maintained to prevent signal leakage. Coplanar (or rotated-cell-based) wire crossing allows two signal paths to intersect on the same physical layer without interference by using 45-degree and 90-degree QCA cells on each path. At the same time, the clock zone-based wire crossing technique assigns different clock phases to the intersecting paths to achieve interference-free crossing. Full adders are the essential basic blocks in the digital circuit design, such as multipliers, Digital Signal Processors (DSPs), Arithmetic Logic Unit (ALU), etc. Consequently, much research has focused on developing compact and efficient full adders on the QCA platform, just as in earlier technologies. Similarly, the Ripple Carry Adder (RCA), being the simplest N-bit Parallel adder, is commonly used in many digital applications. In CMOS technology, it is often labelled as the slowest adder architecture and is therefore replaced by faster designs like the Carry Look-Ahead Adder (CLA) or Carry Select Adder (CSA). However, the QCA-based Ripple Carry Adder (QRCA) can potentially achieve lower delay due to its simple structure.



(a)



(b)

Fig. 1 (a) Basic QCA cell, and (b) Colour representation of cells based on the purpose they are used.

In QCA-based arithmetic circuits, researchers have primarily used Majority gates and inverters as the core elements. Several 3-input and 5-input majority gate variants have been developed and used, together with the inverter gates, in a range of architectures derived from optimized logical expressions. To enhance structural robustness, novel Majority gates with a greater number of cells were introduced; however, these designs often resulted in increased area and latency. Additionally, circuit complexity increased due to the signal-crossing requirements. Several recent publications explored innovative XOR gate designs using the electrostatic intercellular interaction principle. This approach minimizes the reliance on majority gates and hence lowers the overall circuit complexity. Later studies further simplified the circuit design by introducing QCA Full Adder (QFA) structures that use electrostatic interaction alone, eliminating the need for a separate majority gate. Consequently, circuit optimization was achieved in design metrics such as cell count, area, latency, and particularly circuit complexity due to the absence of signal crossovers. However, in most of these designs, not all the input cells are directly accessible, as they are surrounded by regular circuit cells. This limitation hampers the scalability and restricts the applicability of such designs in higher-order architectures. Although researchers have shown significant attention in presenting the optimized Full adder designs, attempts to integrate these adders into efficient and crossover-free RCA architectures with correct output functionality and low complexity have been largely insufficient.

Objectives of the work carried out are:

1. To present a modified XOR gate (MXOR) structure for improved scalability.
2. To propose a scalable and efficient QFA with no crossover (QFANC).
3. To design an efficient and easily extendable QRCA with no crossover (QRCANC), leveraging the simplicity and efficiency of QFANC.

The proposed circuits are analysed regarding cell complexity, area, circuit complexity, latency, and energy dissipation to prove their superiority. The rest of this article is as follows: Section 2 reviews relevant literature on existing full adder designs. Section 3 presents proposed architectures, while Section 4 discusses the simulation results and comparative performance. Finally, the work in this article is concluded in Section 5.

2. Literature Review

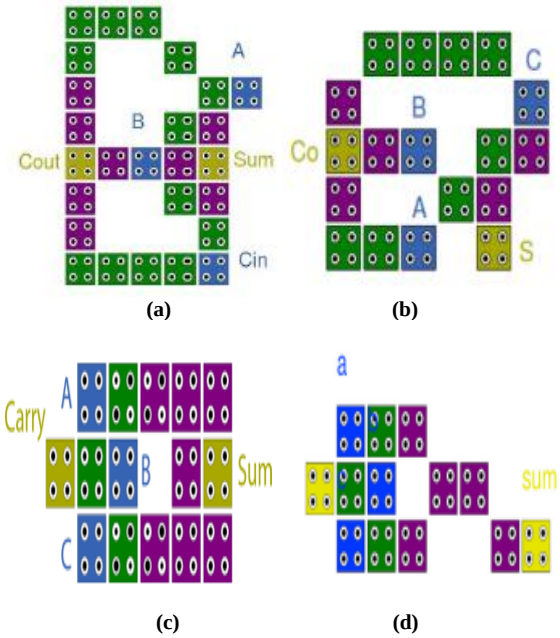
Authors in [11–17] mainly attempted to introduce novel Majority gate structures and subsequently proposed various QCA Full Adders (QFA) based on these gates. The works in [18–21] developed novel XOR gate structures by exploiting electrostatic interactions between cells. These designs enabled QFA implementations that use only two gates: an XOR gate and a Majority gate. However, these QFA designs rely on one of the three wire crossing techniques. The Designs in [11, 17, 20] used the multilayer wire crossing method, which

significantly increases fabrication complexity in QCA technology. In [19, 21], the authors used the rotated cell-based crossover technique, which impacts the circuit size, compatibility, and design complexity. QFA designs [12] and [14] depended on Clock zone-based crossover that introduces optimization challenges and strict clock-zone synchronization.

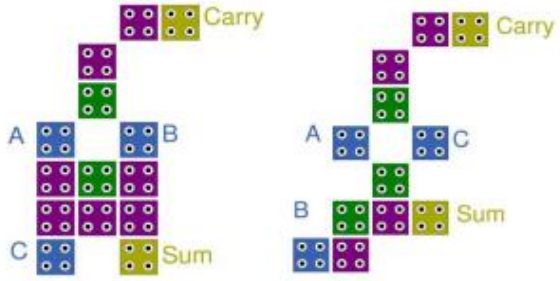
To overcome crossover-related limitations, authors in [22–31] presented simpler designs that avoid the use of crossovers altogether, thereby reducing circuit complexity. Despite this advantage, the QFAs in [22–25] suffer from poor input-cell accessibility, and when these adders are used in larger circuits, signal accessibility becomes a significant issue, eventually forcing the use of crossovers again. For example, S. Babaie et.al [22] presented the QFA shown in Figure 2 (a), which features inaccessible B input and therefore used a multilayer crossover technique to implement an ALU circuit.

Similarly, Figure 2(b) shows the 18-cell QFA proposed in [24], where input cell B is not accessible; hence, the authors used a clock-zone-based crossover while designing QRCA, which increased area, latency, and overall complexity. The QFAs in [26–31] removed the need for a majority gate during carry generation, reducing cell count, but many of these adders still lack scalability.

For instance, the QFAs in [26, 27] shown in Figures 2 (c) and (d) respectively, are not scalable, and their employment in RCA designs offered no improvements, and hence, making accurate output uncertain. Although two QFA designs were introduced in [28], the authors did not demonstrate scalability by implementing these adders in higher-order circuits.



(a) (b) (c) (d)



(e) (f)

Fig. 2 Recent non-scalable QFA designs correspond to: (a) Ref. [22], (b) Ref. [24], (c) Ref. [26], (d) Ref. [27], (e) Ref. [28] Design-1, and (f) Ref. [28] Design-2.

Authors in [29, 30] reported scalable 14-cell QFA designs that can be used to build RCAs without crossovers. Even so, the 4-bit RCA in [29] is ignored, and this leads to inconsistent outputs in simulation; moreover, the latency reported in the paper does not match the obtained results. On the other hand, the QFA in [30] suffers from relatively higher latency (0.75), thereby impacting the overall latency of any n-bit RCA built from it. In [31], a 17-cell QFA is proposed and implemented in an 8-bit RCA design, but reintroduces clock zone-based crossings. Though the QFAs in [35] are compact, when they were reconstructed and simulated under standard QCA rules, the expected and obtained waveforms did not match, confirming that the proposed designs are functionally incorrect. A detailed review of recent QFA utilization in RCA designs is given in previous study, and it is pointed out that many recent QFA implementations focus too much on optimization while ignoring scalability issues. Examples of such drawbacks can be seen in Figures 2(a)-2(d), where the input cell b is not easily scalable, and in Figures 2(e) and 2(f), where inputs A, B, and C, respectively, become difficult to route. The review concludes that more effort is required to develop QFAs that can be effectively integrated into RCA designs without compromising accuracy or increasing design complexity. A summary of physical and performance parameters of the key QFA and QRCA designs reported in the literature is presented in Section 4.

3. Proposed Designs

Here, a novel QFA with No-Crossover (QFANC) is introduced using a Modified XOR gate (MXOR) initially and then utilized to design new structures for 4- and 8-bit ripple carry adders without using any wire crossing.

3.1. Design of QFANC Circuit

The full adder with 3-input variables (A, B, and C_{in}), computes two output functions: Sum and Carry. These logical relationships are expressed in Equations 1 and 2.

$$Sum = A \oplus B \oplus C_{in}$$

$$= \overline{A}\,\overline{B}C_{in} + \overline{A}B\overline{C_{in}} + A\overline{B}\,\overline{C_{in}} + ABC_{in} \quad (1)$$

$$Carry = AB + BC_{in} + AC_{in} = M(A, B, C_{in}) \quad (2)$$

Figure 3 (a) shows the basic architecture used to implement the QCA full adder, as adopted in [18-25], which requires an XOR gate for Sum and a Majority gate for Carry output generation. Since all three inputs are connected to both the XOR gate and the Majority gate, a crossover is required at the highlighted location to make input B accessible. This crossover increases the circuit complexity and may also affect the latency. In this paper, a new architecture is introduced that utilizes an existing majority gate structure within an XOR gate instead of a separate one, as shown in Figure 3 (b).

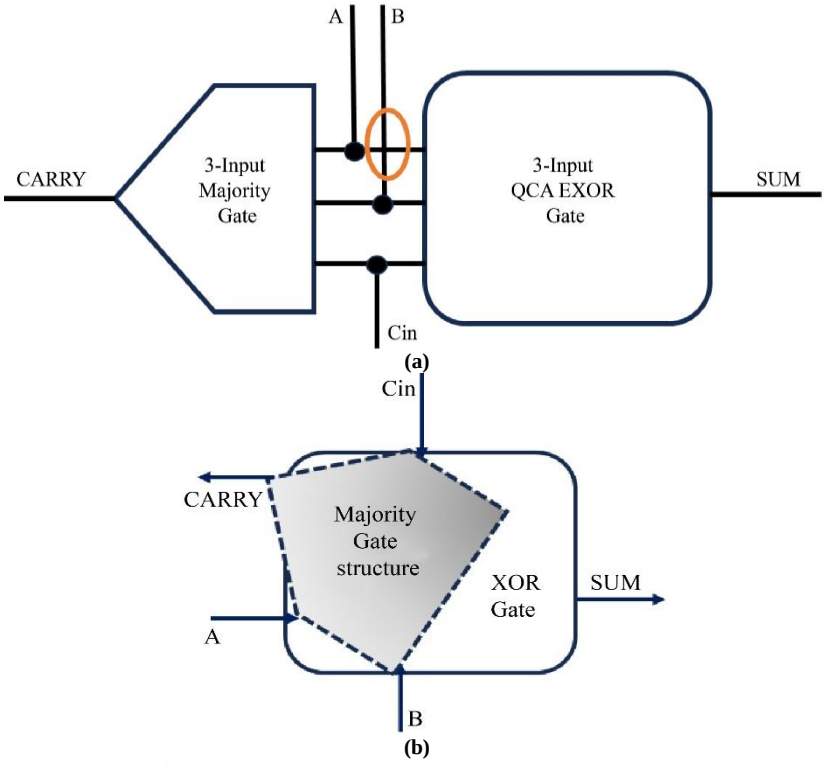


Fig. 3 (a) Block schematic of QFA architecture used in Ref [18-25], and (b) QFA architecture used in this paper.

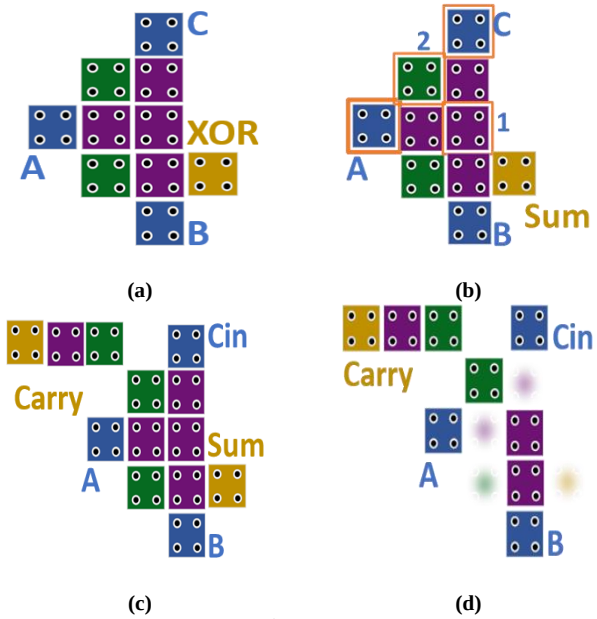


Fig. 4 (a) Cellular layout of MXOR gate, (b) spotlighted cells representing the majority gate structure residing in MXOR, (c) QCA layout of QFANC, and (d) Featured EMG for the carry output.

The XOR gate presented by Seyed-Sajad [23] is modified by placing the output cell in its symmetrical counterpart, and the total structure is rotated left to its vertical position. The modification aims to improve the flexibility of the entire adder structure. The MXOR structure, as depicted in Figure 4(a), comprises a part of the majority gate structure emphasized in Figure 4 (b). This helps to complete the full adder design with only 3 extra cells precisely placed for carry output, as in [31].

The proposed QFANC design shown in Figure 4 (c) requires only 13 QCA cells and is best suited for easy cascading in the RCA design with no crossover. Figure 4(d) provides an overview of the entire Existing Majority Gate structure (EMG) within QFANC, which is responsible for carry generation.

3.2. Design of QRCANC Circuit

A multi-bit adder is basically formed by cascading a number of 1-bit full adders. In a Ripple Carry Adder (RCA), the carry output of each stage feeds the carry input of the succeeding stage. Figure 5 illustrates the N-bit QCA-based RCA architecture implemented in this paper. In QCA design, synchronization among all output bits is required by inserting

the necessary delay cells at the input and output stages. Proposed adder circuit latency is 2 clock phases, so it is implemented in 2 clock zones, clock zones ‘0’ and ‘1’. If the QFANC circuit is given with the inputs at clock ‘0’ phase, the output is available in Clock ‘1’ phase. For an N-bit adder, the output of the last stage is delayed by (N+1) clock phases, out of which 2 clock phases are provided by the nth stage adder circuit cells. So, the last stage adder inputs should be externally given with N-1 clock phase delay cells. Similarly, the output of the stage ‘0’ adder should be delayed externally by N-1 clock phases.

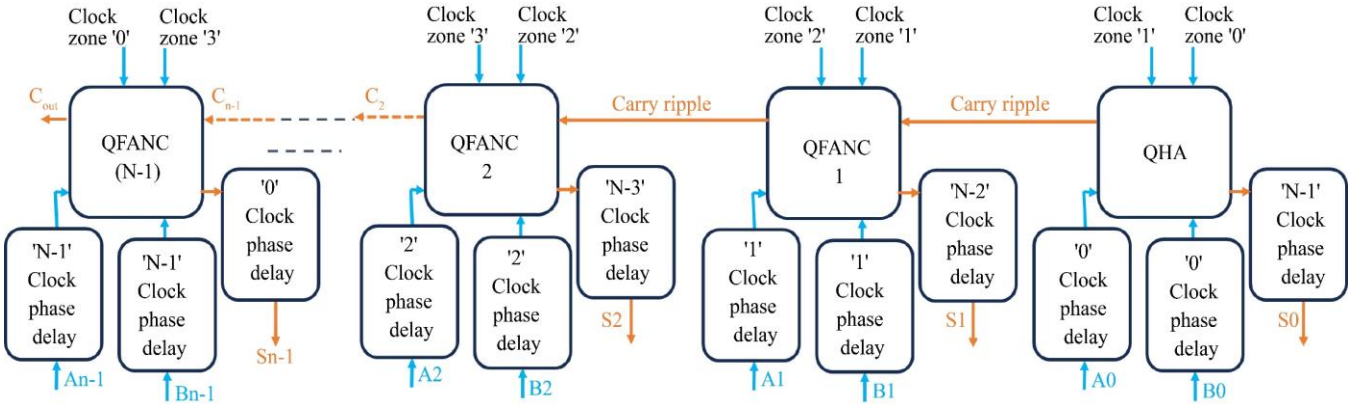
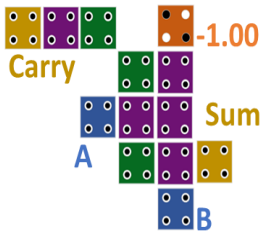
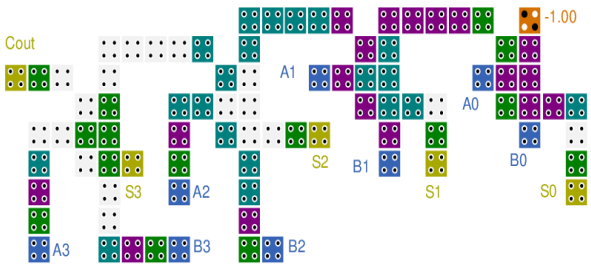


Fig. 5 Block representation of N-bit RCA implementation in QCA technology

This subsection details the designs of both 4- and 8-bit QRCANCs based on QHA and QFANC. The RCA design in this paper employs a Half Adder for the least significant bit addition, while 1-bit Full Adders handle the remaining bits. The QCA Half Adder (QHA) structure is obtained by setting the Cin input of the QFANC fixed polarized to '-1', as illustrated in Figure 6(a). As per the given architecture, the 4-bit QRCANC design shown in Figure 6 (b) requires zero delay cells at the input and 3 delay cells (i.e. N-1) at the output of the QHA (stage ‘0’) adder, and vice versa for the Stage (N-1) adder.



(a)



(b)

Fig. 6 Cellular representation of (a) QHA, and (b) 4-bit QRCANC.

Any higher-order QCA design that necessitates a crossover may affect the overall complexity. The design of QFANC eliminates the need for crossover when cascading, significantly lowering QRCANC's complexity.

To ensure accurate output, the full adder structure of each stage has maintained clock zone symmetry at all inputs. For example, stage ‘0’ does not require any delay cells at the inputs. Stage ‘1’ requires only one delay cell each at A1 and B1, so only one cell is used at carry input, but in the next stage onwards, the delay cells at An and Bn inputs are so arranged that they also compel the usage of 2 cells at carry input also.

The 4-bit QRCANC is designed by considering all the design constraints to ensure reliable output, and it requires only 86 QCA cells. Further, it is easily extendable to any n-bit size. The construction is simple and eliminates the signal crossovers, so the area optimization with reduced complexity is attained without compromising the output reliability. Figure 7 depicts an 8-bit QRCANC design with 236 QCA cells.

4. Simulation Results and Performance Analysis

This section describes the simulation process and performance analysis of the presented designs with parameters like complexity, latency, and energy dissipation.

4.1. Simulation Results

The suggested designs are implemented using the QCA Designer (v2.0.3) tool [8]. The tool provides two simulation engines: Bistable approximation and Coherence vector. In this work, the circuits are simulated in bistable mode for functional verification, and Figure 8 shows the default parameter settings used in the simulations.

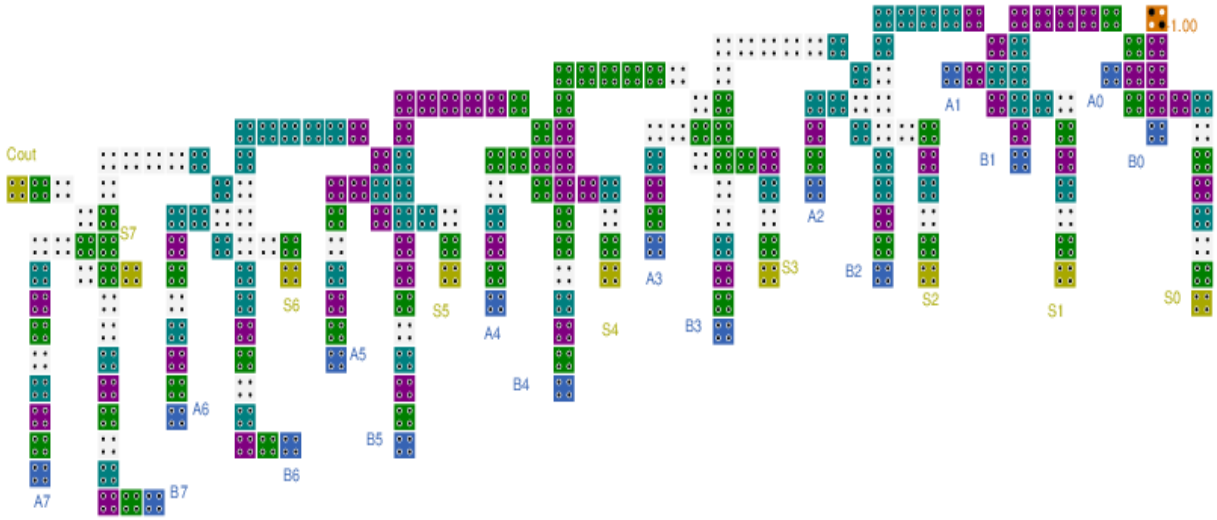


Fig. 7 Cellular layout of 8-bit QRCANC

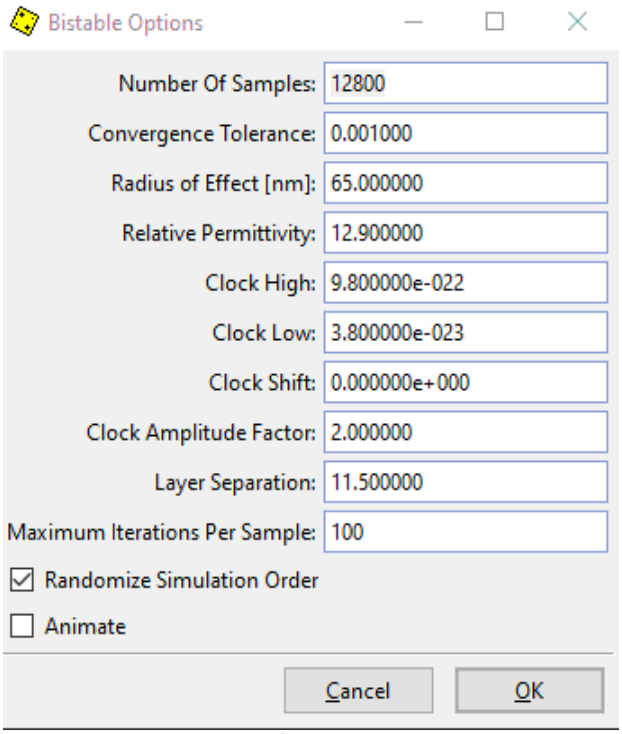
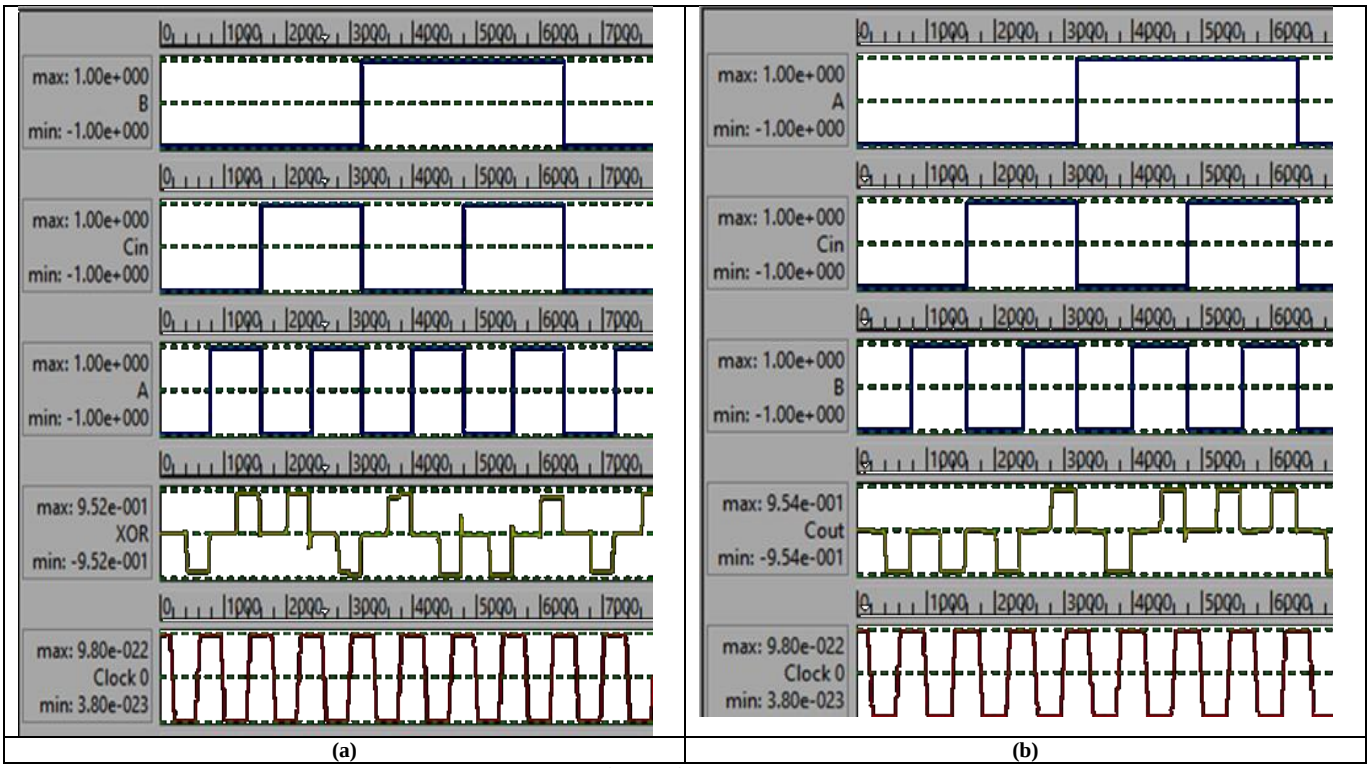


Fig. 8 Options setting for bistable simulation engine

The MXOR gate, EMG, and QFANC, requiring only 8 input combinations, are simulated in the exhaustive mode. The corresponding results of MXOR and EMG are shown in Figures 9 (a) and (b). The MXOR gate using 10 cells takes up an area of 0.008 μm^2 with 0.5 clock cycles of delay. The EMG structure of nine cells dwells in an area of 0.0097 μm^2 with 0.5 clock cycles of latency. QFANC takes up 0.0115 μm^2 of area, and Figure 10 depicts a 0.5 latency experienced by both outputs. The 4- and 8-bit QRCANCs are simulated in vector table mode as they have a large set of input combinations. For reporting the results, a limited number of input combinations are applied, and simulated waveforms are shown in vector form. 4-bit QRCANC engages an area of 0.1µm2, and the simulated waveforms shown in Figure 11 illustrate a delay of 1.25 clock cycles. In the same way, the 8-bit QRCANC takes up 0.38 µm2 of space and has a latency of 2.25 clock cycles, as shown in Figure 12. All these designs generate outputs with strong polarization. The lowest value of the maximum polarization observed at the output bit S6 is 9.47e-1, which is notable.



(a) (b)

Fig. 9 Simulated waveforms of (a) MXOR gate, and (b) EMG.

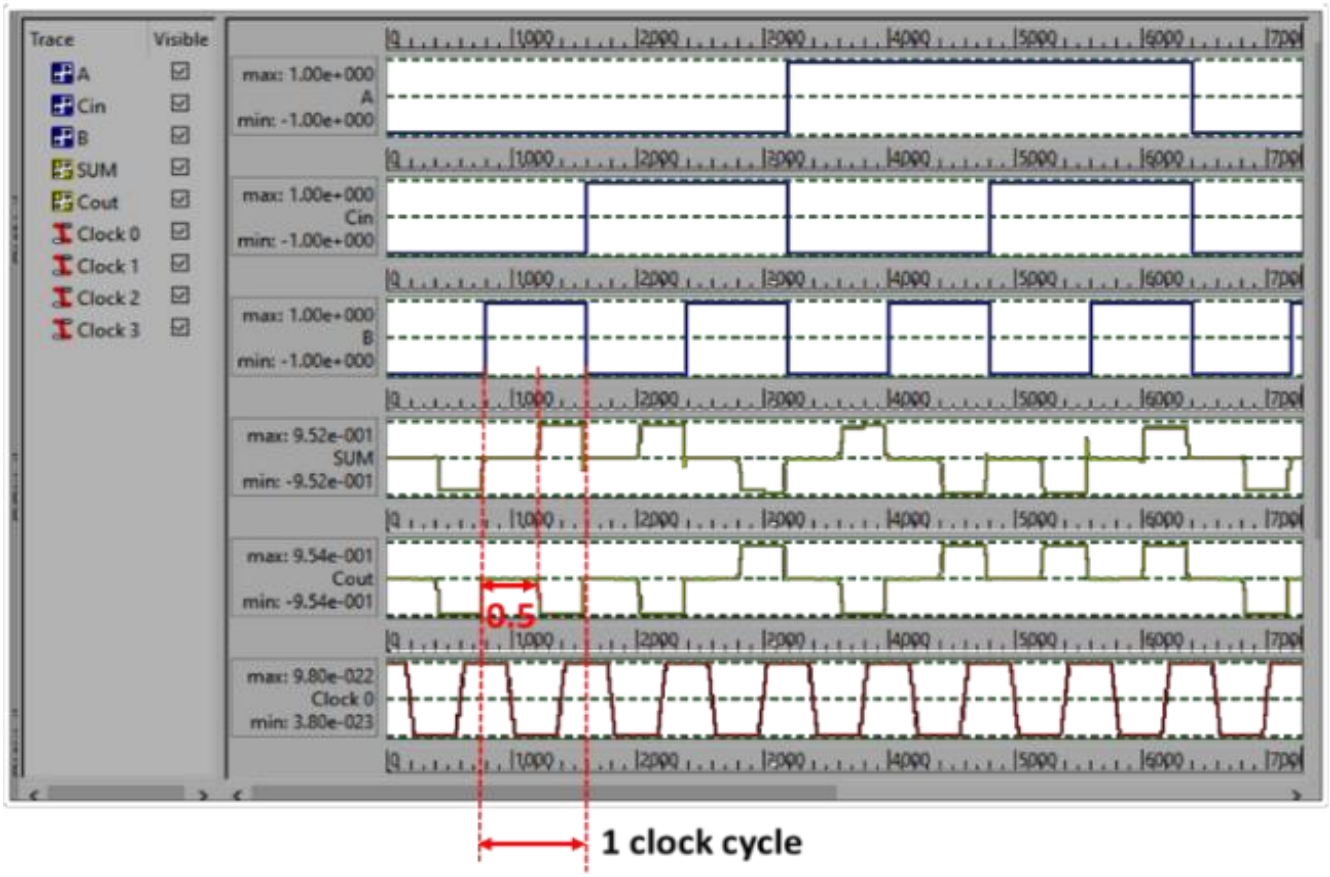


Fig. 10 Simulation results of QFANC

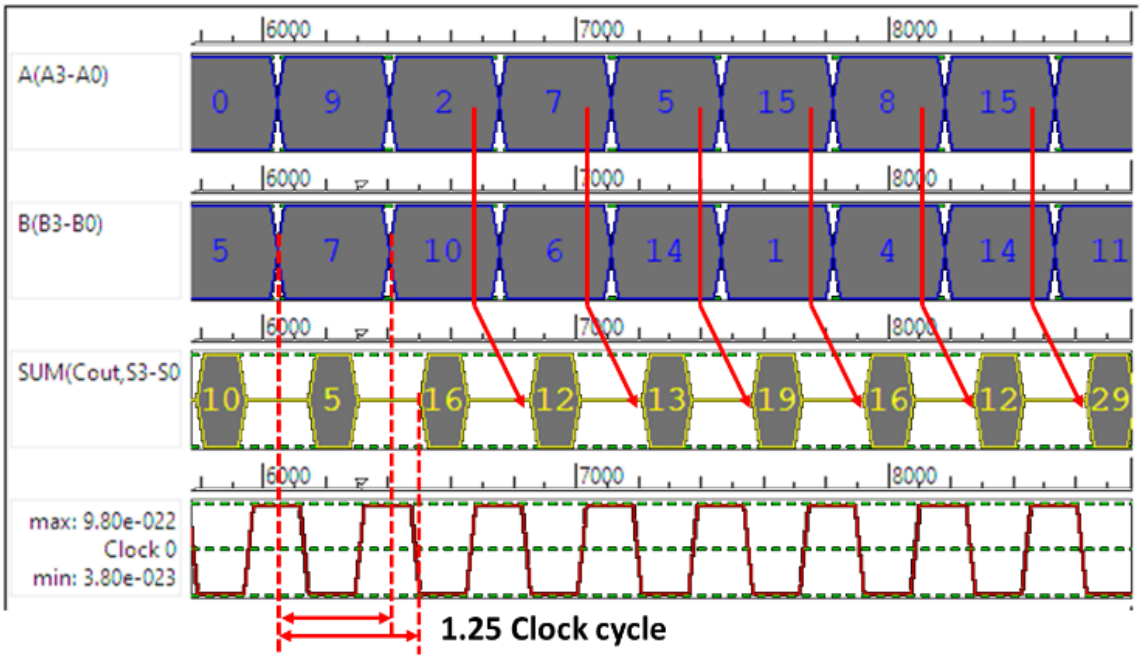


Fig. 11 Simulation results of 4-bit QRCANC

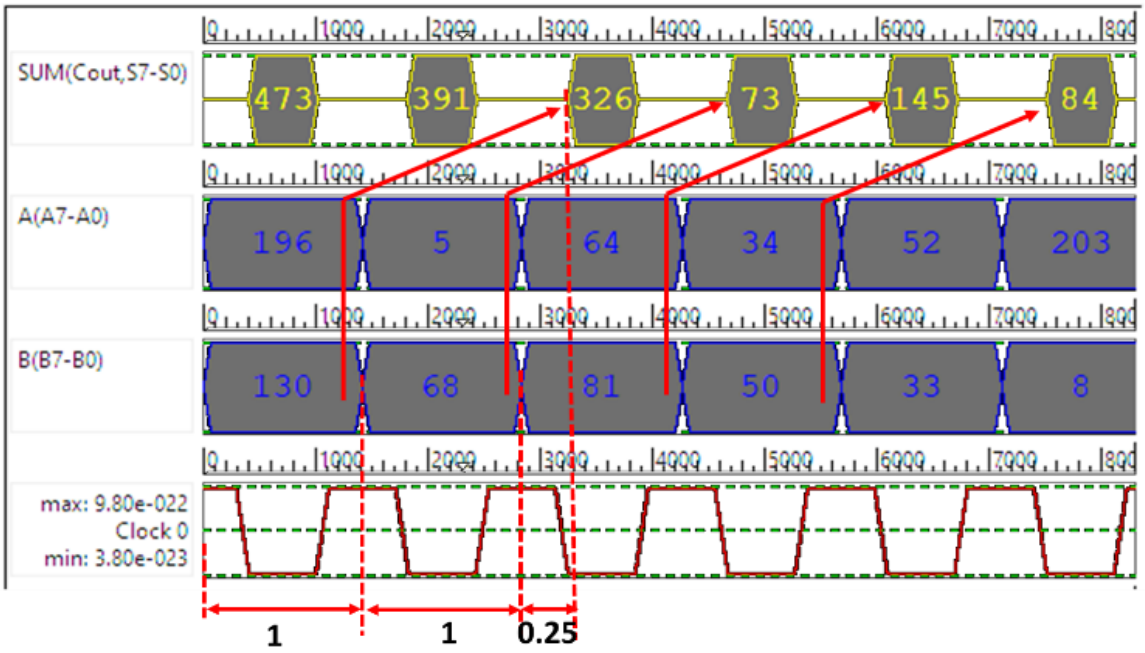


Fig. 12 Output waveforms of 8-bit QRCANC

4.2. Performance Analysis

The performance evaluation of QCA designs typically involves assessing factors such as the number of cells used (cell complexity), occupied area in µm2, latency in terms of clock cycles, type of crossover (complexity), and energy dissipation. Table 1 presents a comparison between the presented and existing QFAs. Synthesis cost is also evaluated using the QCA cost function given in Equation 3 [24, 36, 37], and the corresponding results are recorded in Table 1.

$$\text{QCA Cost Function} = \text{Area} * \text{Latency}^2 \quad (3)$$

However, the recent designs are emphasizing the compactness through electrostatic interaction between cells, by ignoring the input and output cell accessibility, i.e., Scalability. This aspect can significantly impact circuit complexity as it requires wire crossovers when implemented in higher-order designs. Hence, from Table 1, the QFA designs [15, 16, 18, 22-28, 33] can be neglected for

comparison as they are not scalable. Figure 13 represents the full progress of the proposed QFANC over the existing scalable QFAs [12, 13, 19, 21, 29, 30-32, 34]. As depicted in the graph, the QFANC exhibits 7% and 14% optimisation in terms of cell complexity and QCA synthesis cost compared to the best scalable QFA with no crossover reported in [29].

Table 1. Comparison between QFANC and existing QFAs

QFA Design	Cell Complexity	Area (μm^2)	Latency (Clock cycles)	QCA Cost	Crossover used (Circuit Complexity)	Input and Output Cell Accessibility
[12]	71	0.06	1.25	0.094	Clock-zone-based	Yes
[15]	48	0.05	0.75	0.028	No	No
[17]	38	0.02	0.75	0.011	Multilayer	Yes
[16]	27	0.02	0.5	0.005	No	No
[19]	41	0.04	0.5	0.01	Coplanar	Yes
[18]	29	0.02	0.5	0.005	No	No
[22]	26	0.03	0.5	0.008	No	No
[13]	71	0.07	1	0.07	Clock-zone-based	Yes
[23]	20	0.016	0.75	0.009	No	No
[21]	40	0.03	0.5	0.008	Coplanar	Yes
[24]	18	0.01	0.5	0.0025	No	No
[25]	28	0.02	0.5	0.005	No	No
[26]	15	0.007	0.5	0.002	No	No
[27]	13	0.009	0.5	0.002	No	No
[28] Design-1	12	0.014	0.5	0.004	No	No
[28] Design-2	14	0.011	0.5	0.003	No	No
[29]	14	0.014	0.5	0.004	No	Yes
[30]	14	0.016	0.75	0.009	No	Yes
[31]	17	0.02	0.5	0.005	No	Yes
[32]	51	0.06	0.5	0.015	Coplanar	Yes
[33]	13	0.02	0.5	0.005	No	No
[34]	36	0.01	1	0.01	Coplanar	Yes
QFANC	13	0.012	0.5	0.003	No	Yes

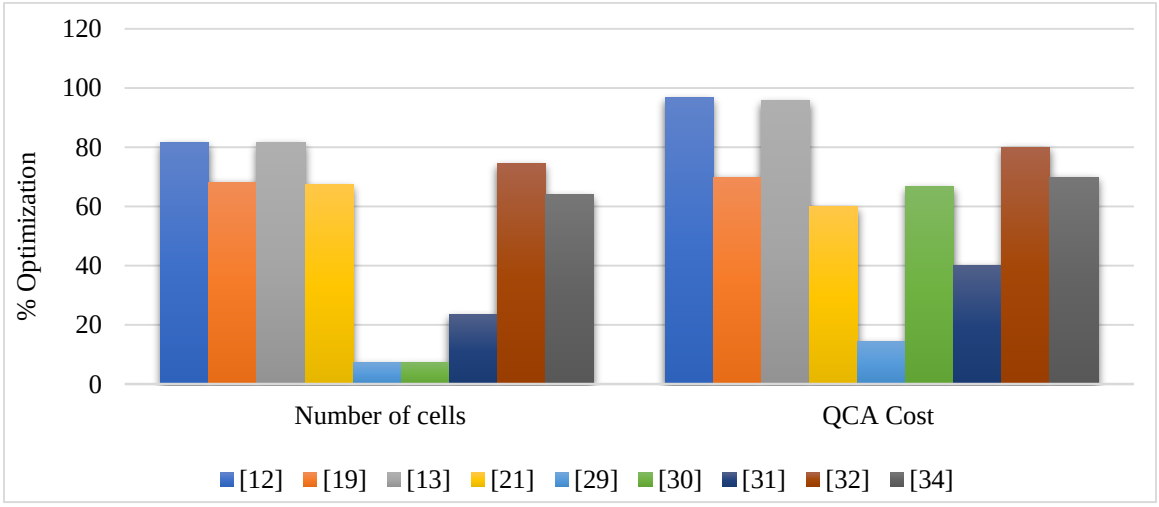


Fig. 13 Optimization of the QFANC over the existing scalable QFAs

The authors conduct a comparative study of 4- and 8-bit QRCAs with previous designs that follow proper design principles, such as placing the delaying cells to maintain synchronization at the input and output, appropriately cascading successive adder sections, and implementing crossovers when necessary. Therefore, the comparison excludes the RCA designs suggested in [26, 27, 29]. Table 2 organizes the simulated outcomes of the presented QRCANC and existing designs across various metrics for comparative analysis.

Table 2. Simulated outcomes of proposed 4- and 8-bit QRCANC in various aspects compared to existing designs

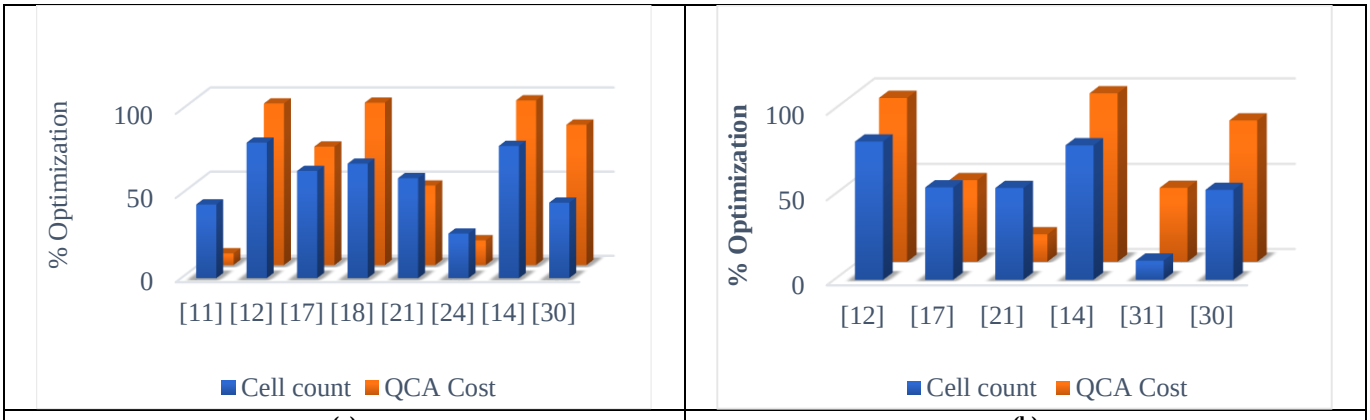
QRCA	Design in Ref	Cell Complexity	Area (μm²)	Latency (clock cycles)	Cross-over Used
4-bit	[11]	153	0.11	1.25	Multilayer
	[12]	442	1	2	Clock-zone based
	[17]	237	0.24	1.5	Multilayer
	[18]	269	0.37	3.5	Clock-zone based
	[21]	212	0.194	1.25	Coplanar
	[24]	117	0.12	1.25	Clock-zone based
	[14]	401	0.41	4.25	Clock-zone based
	[30]	156	0.19	2.25	Not required
	This paper	86	0.1	1.25	Not required
8-bit	[12]	1254	3	4	Clock-zone based
	[17]	517	0.59	2.5	Multilayer
	[21]	513	0.452	2.25	Coplanar
	[14]	1122	2.31	8	Clock-zone based
	[31]	266	0.67	2.25	Clock-zone based
	[30]	501	0.62	4.25	Not required
	This paper	236	0.38	2.25	Not required

Optimization obtained by the proposed 4-bit and 8-bit QRCANC designs over existing designs is represented in Figures 14 (a) and (b), respectively. The 4-bit QRCANC exhibits a 45% and 83% reduction in cell count and QCA cost, respectively, compared to the scalable RCA, with no crossover reported in [30]. An optimization of 26% in cell complexity and 15% in QCA synthesis cost is noted over the best reported clock zone-based QRCA [24]. The 8-bit QRCANC reports a 43% and 11% decline in cell complexity and QCA cost, respectively, compared to clock zone-based QRCA in [31]. 53% and 83% optimization in cell count and QCA cost are noticed compared to a no-crossover 8-bit QRCA design reported in [30].

4.3. Energy Dissipation Analysis

Energy dissipation of the proposed circuits is evaluated using QCA Designer-E (QD-E) [9], an enhanced extension of QCA Designer 2.0.3 released by Sill Torres et al. in 2018. Although QCA Pro [10] is an extensively utilized tool in the prior work, QD-E is preferred here because it offers full compatibility with layouts created in the QCA Designer 2.0.3 environment.

In addition, QD-E provides a dedicated simulation engine: Coherence vector (w/ Energy), specially used for energy dissipation analysis. The simulated energy values of the suggested designs are summarized in Table 3.



(a) (b)

Fig. 14 Percentage optimization of (a) 4-bit QRCANC, and (b) 8-bit QRCANC.

Table 3. Analysis of QFANC and QRCANC designs based on energy dissipation

Design	Sum_Ebath (eV)	Error (Sum_Ebath) (eV)	(Avg_Ebath) (eV)	Error (Avg_Ebath) (eV)
QFANC	7.01e-3	-6.82e-4	6.37e-4	-6.20e-5
4-bit QRCANC	4.90e-2	-4.83e-3	4.46e-3	-4.39e-4
8-bit QRCANC	1.25e-1	-0.19e-2	1.13e-2	-1.08e-3

Estimation is also performed for the equivalent QFAs presented in [24-30] on the QD-E platform for relative comparative analysis, and the total and average values are arranged in Table 4. A 3% reduction in energy dissipation is obtained in QFANC over the QFA [29], which exhibited the least.

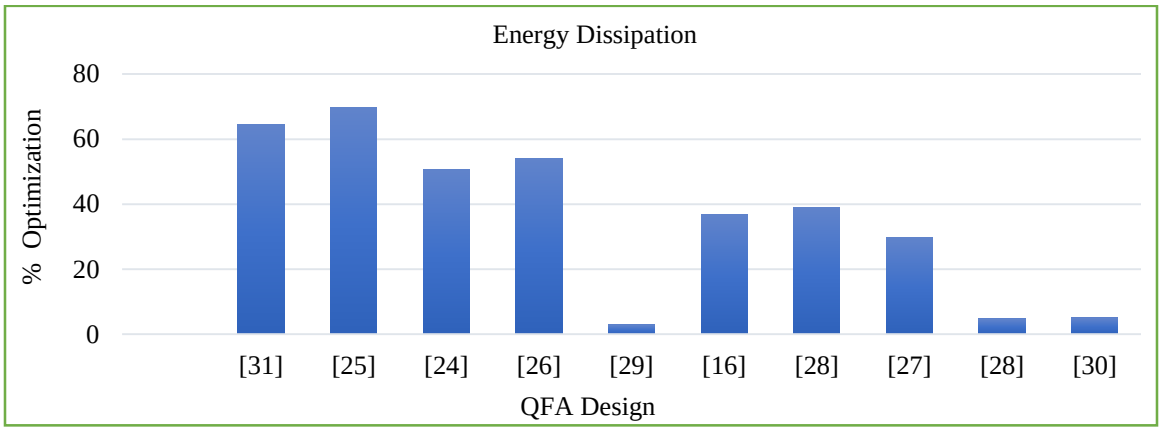


Fig. 15 Energy enhancement of the proposed QFANC over others

Table 4. Energy dissipation analysis of suggested QFA and QRCA designs and existing QFAs evaluated in QD-E

QFA Design	Energy Dissipation (Total) in eV	Energy Dissipation (Average) in eV
[16]	1.11e-2	1.01e-3
[24]	1.42e-2	1.29e-3
[31]	1.98 e-2	1.80e-3
[25]	2.31e-2	2.10e-3
[26]	1.53e-2	1.39e-3
[29]	7.23e-3	6.58e-4
[27]	1.00e-2	9.10e-4
[28]-1	1.15e-2	1.04e-3
[28]-2	7.36e-3	6.69e-4
[30]	7.38e-3	6.71e-4
QFANC	7.01e-3	6.37e-4

5. Conclusion

This work introduces a 13-cell 1-bit QFA with No-Crossover (QFANC) built on a Modified XOR gate (MXOR) structure, leveraging electrostatic intercellular interaction. 4- and 8-bit QRCANC designs are developed that are easily extendable to any N-bit size without increasing the circuit complexity. Though optimization was the focus of research, significant attention was paid to designing higher-order circuits following the basic design principles to ensure reliable output. The QFANC exhibits a 15% decrease in area, a 7% decrease in cell complexity, and a 3% decrease in energy dissipation compared to the best QFA design reported in the literature. The QRCANC, with considerable performance improvement in various parameters, confirmed its efficiency, attributed to the scalability of the presented QFA.

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