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Original Article

Design and Analysis of 18nm finFET based 4-bit Shift Registers Using Transitional Hybrid Logic Flip-Flop

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Abstract - *A shift register remains a kind of sequential logic circuitry primarily employed for the storage of digital data across many digital devices to enhance the functionality of digital circuits. The present paper presents an energy-effective shift register that employs a novel flip-flop involving an implicitly conditioned crossover architecture. The suggested flip-flop exhibits excellent reliability with minimal power usage. Employing four clocked devices in conjunction with the transitional condition approach further enhances the speed. In the simulations for the suggested architecture, the Serial In-Serial Out (SISO) and Parallel In-Parallel Out (PIPO) shift registers used the least amount of power. The architecture has just 16 devices and has been simulated using 18 nm finFET technology utilizing a 0.7 V power supply. The proposed flip-flop design employs hybrid logic transistors that reduce power consumption by at least 45% when compared to previous designs across various process corners. Also, the proposed flip-flop uses less power by atleast 15% across a wide supply voltage range of 0.7V to 1V, outperforming earlier devices in this respect. The suggested flip-flop is at least 20% quicker than current FFs across all process corners. The recommended 4-bit shift registers achieve the PVT criterion. It uses less power and operates slower at the Slow-Slow (SS) process corner and vice-versa at the Fast-Fast (FF) process corner. Furthermore, when the temperature rises, power utilization increases while delay decreases.*

Keywords - *PIPO, SISO, Flip-Flop, 18nm, finFET.*

1. Introduction

For years, several digital electronic devices have extensively used the shift register. This part of the circuit makes it easier to switch between serial and parallel connections while data is being sent, and it may also work as a circuit with delay. The shift register represents an important part of digital circuits that are used in sensors, active-matrix displays, memory devices, and real-time digital signal-processing processors [1, 2]. The efficiency of technological processes has increased by making parts smaller. This has made electronic devices work better, and shift registers have become much more useful. Consequently, minimizing the additional integrated circuitry design space and reducing power usage within shift register architecture evolves into more critical as capacity increases [3, 4]. A conventional configuration in the shift register has N-bit flip-flops arranged in sequence.

The circuitry under this design is rapid and efficient. However, the design fails to meet the demands of reduced overhead plan space and decreased power usage. The master-slave latched structure maintains the same data across two latches throughout one clock cycle. Consequently, the master-slave latch often demonstrates excessive area and consumes more electrical power. Clearly, when shift registers are made with master-slave latches and no compensation circuitry, data could be sent to many outputs at the same time, which could lead to a problem [5-7].

The shift register circuitry employs a Flip-Flop (FF) as an essential memory element [8, 9]. Developing a high-performance, low-power shift register necessitates a focus on the development of efficient flip-flops [10]. In contemporary CMOS technologies, low power usage has been described as the paramount issue, particularly for portable functions and portable electronics. The power utilization of the clock module is predicted to be half of the entire system's power [11]. Consequently, the flip-flops constitute a significant proportion of the silicon area as well as power usage within the entire system [12]. Pulsed Flip-Flops (P-FFs), along with master-slave flip-flops, constitute the two categories of flip-flops. Lin et al. [13] showed a highly reliable flip-flop operating at lower voltage and power levels, lowering the total number of transistors while increasing speed, energy consumption, and efficiency. Park et al. [14] created a DCSFF having 24 devices with reduced dynamic power consumption by 98% and 32%, respectively, when compared to standard flip-flops. Yin et al. [15] suggested an asymmetrical flip-flop

design with a unique toughened arc, which increased thresholds by a factor of ten over ordinary D flip-flops. A Redundancy Elimination-Based Flip-Flop (REFF) was suggested by Shin et al. [16] as a way to lower the voltage from 1 V to 0.3 V while keeping static and contention. In their paper [17], Lee et al. proposed a DET-FF that operates consistently at lower voltages, protects input data across both clock edges, and consumes less power than SET flip-flops. You et al. [18] used innovative sense amplifier levels and reengineered single-ended latching circuits to create a SAFF capable of operating at elevated speeds with little power utilization, hence enhancing energy efficiency and reducing latency.

Sadiq et al. [19] developed a flip-flop design that significantly reduces latency along with power usage compared to conventional master-slave flip-flops. This implies there is reduced clock overload, power consumption, and total transistor count. Cadence Virtuoso accomplished the findings by advancing 18nm FinFET technology and simulating a Monte Carlo model. The findings indicated great stability when compared to earlier designs. Furthermore, the Master-Slave (MS) latch architecture stores identical data in two latches within a single clock cycle.

Badal et al. [20] presents an energy-efficient shift register that employs a novel flip-flop. The suggested flip-flop exhibits excellent efficiency along with minimal power consumption. The circuitry consists of a sampling circuit with 6 transistors and a keeper circuit. Using four timed devices in conjunction with the transitional condition approach improves the velocity. The simulation results indicate that the suggested topology exhibits a minimum power consumption. The architecture has 16 devices and has been simulated using 130 nm CMOS technological advances, as well as a 1.2 V power source.

The ongoing miniaturization associated with planar MOSFETs during the past forty-five years has resulted in a significant increase in the transistor count inside Integrated Circuits (ICs). Moving forward, the present pattern in the nanometre regime presents significant challenges because of a significant rise in subthreshold current leakages (IOFF) [21]. Because deeply scaled MOSFETs have shorter channel lengths, the drain potential changes the electrostatic forces in the channel. This means that the gate can't regulate the channel as well as it should. The gate fails to fully close the channel when in off-mode, resulting in an elevated Ioff across the drain as well as the source. Limited research has been conducted on the use of FinFET-based flip-flops and shift registers. Figure 1 delineates the fundamental contrast amongst FinFET and also traditional FET.

Despite the aforementioned conversations, the concurrent demands for the reduction of power usage remain unachieved in the work reported so far. This paper presents a conditioned crossover flip-flop design to improve area efficiency at low operating voltages. This study suggests a cross-implicit-pulse hybrid logic flip-flop-based shift register as a way to get around the problems with the current MS latch architecture. The suggested technique necessitates just a single latch to execute the same functions identical to the MS latch within a conventional shift register. Consequently, the suggested shift register design minimizes power consumption by decreasing the transistor count. Section 2 includes the operating features of the recommended flip-flop and shift register. In Section 3, the proposed simulated findings from the design are presented in comparison to the current designs. Section 4 presents the conclusion.

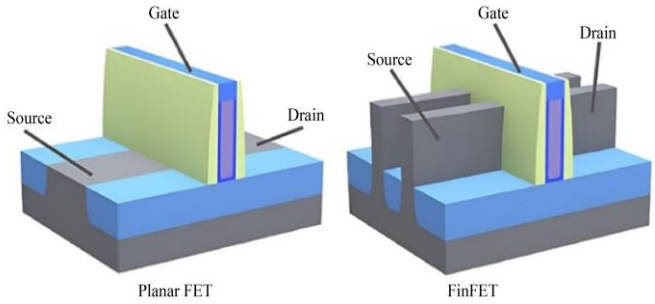

Fig. 1 Analysis of FinFET and planar FET components [22]

2. Methodology Adopted

A low-powered finFET-based shift register is currently being developed to address the present need for energy-efficient and cost-effective electronics. The technology articulates the model properties linked to the devices employed in the design. The Cadence Virtuoso EDA tool constructs and simulates the suggested flip-flop and shift register. We have integrated and simulated each component using an 18nm technology.

2.1. Proposed Implicit Hybrid Logic Based Flip-Flop

The modified low-powered flip-flop consists of two inputs with a single output and two output topologies. When the inputs are the same, the output inversely correlates with the inputs to operate. Figure 1 illustrates the schematic depiction of the proposed flip-flop. The circuit has a functional front-end phase and a static output, making the suggested structure a hybrid implicit pulsating flip-flop. The suggested structure consists of three elements:

1. A basic muller C-element composed of 4 devices, namely PM2-PM3, NM5-NM6;
2. A sampling circuitry consisting of five devices, namely NM3, NM4,NM1,NM0 and PM0; and
3. A keeper circuit, identified as PM4-NM7, PM5-NM9 and NM8. The nodes Dbar along with node X are recognized as complementing input data for the muller C-element.

Initially, at the onset of the clock's rising edge and with the data being provided low, device M2 activates, causing

device M1 to flip on briefly due to the sustained high level of CLKB, which is referred to as the transparency window. Consequently, the devices (NM3 and NM4) become operational throughout this brief period. Upon the transfer of data from '1' towards '0,' Dbar attains a value of 1, prompting the two NM3 and NM4 devices to shift from the node Dbar to the intermediate node X. Currently, X has been pre-charged to activate the devices NM5 & NM6, resulting in the node Q being pushed down.

Whenever CLKB remains lower, the state of the transparency window deactivates. Simultaneously, whenever the input signal becomes higher or the change from '0' towards '1' occurs, the Dbar signal decreases. As previously mentioned, devices NM3 and NM4 become operational momentarily at the arrival of the clock's rising edge, which will cause node X to experience being pulled down along this pathway. Whenever each of the inputs related to the muller C-element remains low, the resultant value happens to be high, causing node Q to turn into 1, which then drives QB low. Inverting circuit PM1-NM2, VDD, and device NM1 will be linked in series with the help of a pull-down circuit to create an adequate latency within this phase. The developed flip-flop comprises an overall of 16 devices, resulting in a minimal configuration. Furthermore, changes do not occur in the inner nodes at each cycle of the clock unless D necessitates output charges; hence, power usage is minimized. The method implemented in this architecture is referred to as a 'conditioned crossover.'

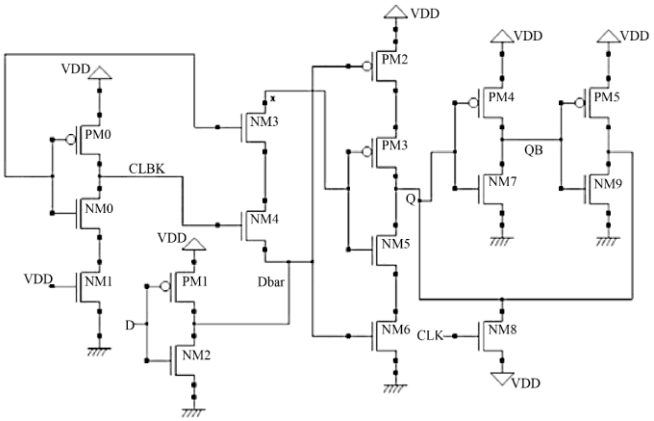

Fig. 2 Proposed conditioned crossover hybrid logic Flip-Flop

2.2. Design of Recommended Low Power Shift Registers

The shift register comprises an assemblage of flip-flops. Multiple flip-flops have connectivity, resulting in the final result of a single flip-flop function providing the data being supplied for a different one. A shared clock simultaneously sets or resets multiple flip-flops. The register enables each flip-flop to independently retain the data from its adjacent counterpart. The memory capacity concerning a register indicates the total number of bits associated with digital data it has the ability to accommodate. Each flip-flop adhering to a shift register represents one bit of stored data. The suggested flip-flop integrated shift register would be suitable for devices with low power requirements and rapid connectivity applications that operate in real-time. This work delineates the design of SISO shift registers, and PIPO shift registers employing the proposed flip-flop, functioning at an operating voltage of 0.7 V and implementing 18 nm finFET technology. Figures 3 and 4 demonstrate an illustration of 4-bit parallel in/parallel out, as well as four-bit series in/series out shift registers.

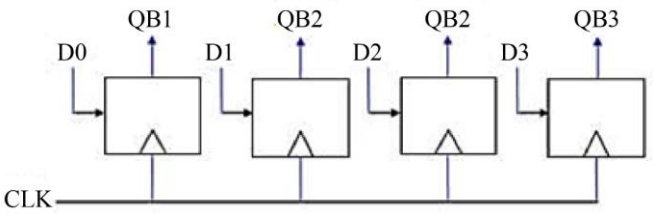

Fig. 3 Representation of 4-bit Parallel In Parallel Out(PIPO) shift register

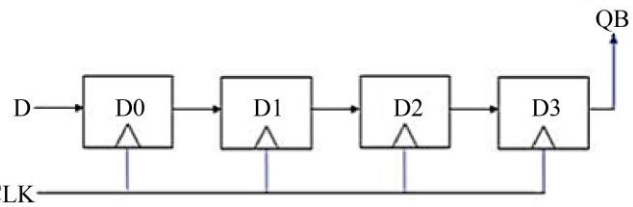

Fig. 4 Representation of 4-bit Serial In Serial Out(SISO) shift register

3. Results and Discussions

The suggested shift register designs and their components are evaluated in the research using Cadence Virtuoso EDA software. It compares their performance using 18nm finFET devices, taking into account power consumption and latency. The research replicates current flip-flop topologies as well as the anticipated flip-flop using 18nm FinFET technology. The study investigates several process features and computational aspects.

Table 1. Configuration of specifications for the simulation process

Parametric Variable	Value
Technology (nm)	18
Source Voltage (V)	0.7V
Device	finFET
Temperature (^{0}C)	27
Transistor Dimensions(W/L ratio)	NFET:1/1 PFET:2/1

In semiconductor manufacturing, all three factors (process, voltage, and temperature) directly influence the performance of each cell. The corners, referred to as "square corners," function as reference points for establishing the optimal operational parameters for the chip. The operating circumstances of a device have been defined by two primary variables: the operational voltage (V) and the temperature (T),

which may range from -25^0 to 75^0 degrees Celsius. Fluctuations in PVT significantly affect the performance associated with flip-flop cells, impacting power usage, latency, and total effectiveness. This study performed a comprehensive analysis of the PVT variations throughout both proposed and currently operating cells to provide precise comparisons. The investigation research was conducted and compared with various different cells under examination. The transient study of the suggested flip-flop is shown in Figure 5. Current and recommended flip-flops had been developed and modelled to verify that the recommended flip-flop had the requisite functionality regarding power usage and speed. The PVT assessment conducted on the flip-flop architectures yielded significant information about their performance over diverse PVT circumstances. The findings indicated that the architecture is resilient to fluctuations in PVT.

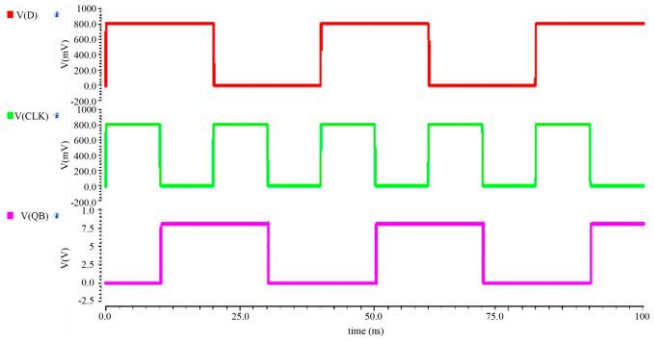

Fig. 5 Transient simulation waveform of proposed FF

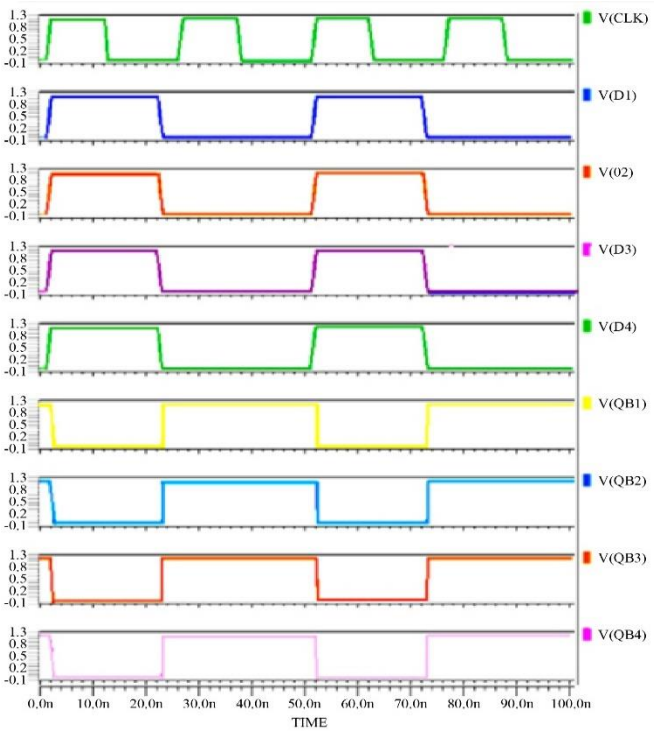

Fig. 6 Transient Simulation waveforms of proposed 4-bit PIPO shift register

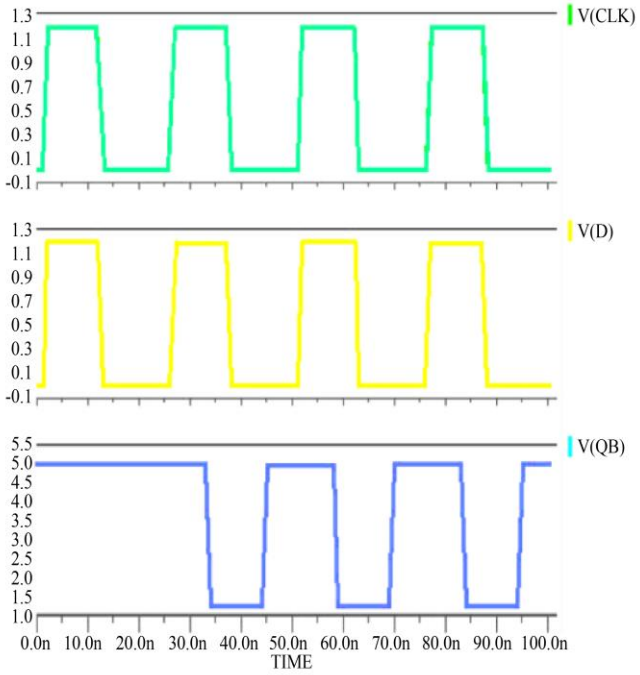

Fig. 7 Transient Simulation waveforms of proposed 4-bit SISO shift register

Figures 6 and 7 demonstrate the Proposed 4-bit PIPO shift register waveforms and proposed 4-bit SISO shift register, respectively. Within PIPO shift registers, each of the information bits, encompassing both inputs as well as outputs, execute parallel tasks. The integrated flip-flops become activated through a clock signal. Figures 3 and 4 illustrate that D1 to D4 denote the parallel inputs, while QB1-QB4 signify the parallel results. Upon clock activation, every input value (D1–D4) can be seen at the associated outputs (Q1–Q4) concurrently. This type of shift registers functions as an intermittent storage system or serves as a delay mechanism. The rate of shift in clock pulses indicates the magnitude of the delay. This type of register lacks interconnections among individual flip-flops, as sequential moving of data seems unnecessary. SISO shift registers accept information a single bit, starting a time within a sequential manner. It produces the stored data within a serial format at its final result.

3.1. Analysis of Proposed FF

Optimal power utilization is especially important for minimal power activities as it empowers numerous processes to operate concurrently and effectively, resulting in improved system performance. Figure 8 shows Figure 9 shows that the proposed flip-flop uses less power by atleast 15% across a wide supply voltage range of 0.7V to 1V, outperforming earlier devices in this respect. The design is also more efficient than earlier devices across a wide supply voltage range, suggesting the possibility of improved system performance. This is done using fewer PFET transistors and mixed logic, reducing circuit complexity.

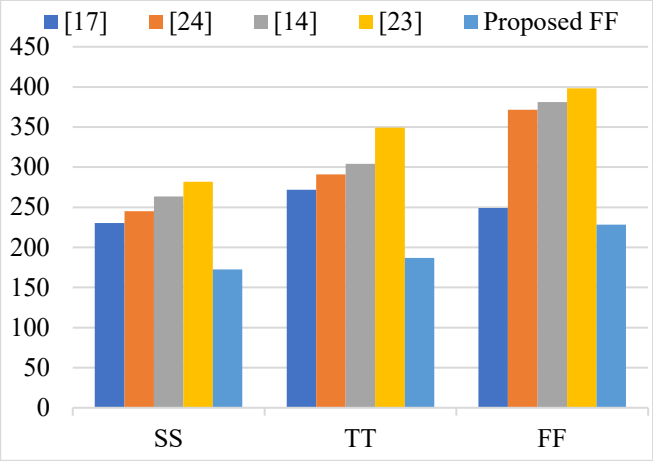

Fig. 8 Power utilization of the suggested flip-flop (FF) w.r.t current FFs under various process variations

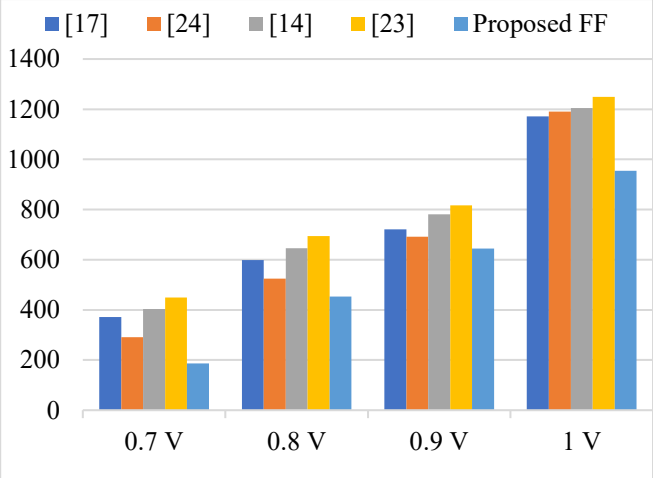

Fig. 9 Power utilization of the suggsted flip-flop (FF) w.r.t current FFs under various source voltage variations

The recommended flip-flop consumes much less power than typical implementations all over a temperature that ranges from -25°C to 75°C. The proposed configuration employs solely hybrid logic transistors, reducing power consumption by at least 35% despite temperature variations. The corresponding data is demonstrated in Figure 10.

The FF circuitry design, which only uses these transistors, aims to save power by employing fewer PFET transistors and mixed logic while reducing circuit complexity. The PVT assessment shows that the suggested flip-flop cell can fulfil power consumption requirements. The proposed circuitry aims to reduce delay in the signal inputs and the signal outputs in proposed flip-flop designs through the elimination of PFETs within the slave circuit design.

The suggested delay duration and effectiveness are consistent with VLSI technology criteria. The PVT research assesses the durability of the shown flip-flop in a range of physical environments. The delay that exists between the input nodes and output nodes is calculated for the complete voltage range, 0.7 V to 1.0 V. The suggested flip-flop is at least 20% quicker than current FFs across all process corners, as demonstrated in Figure 11.

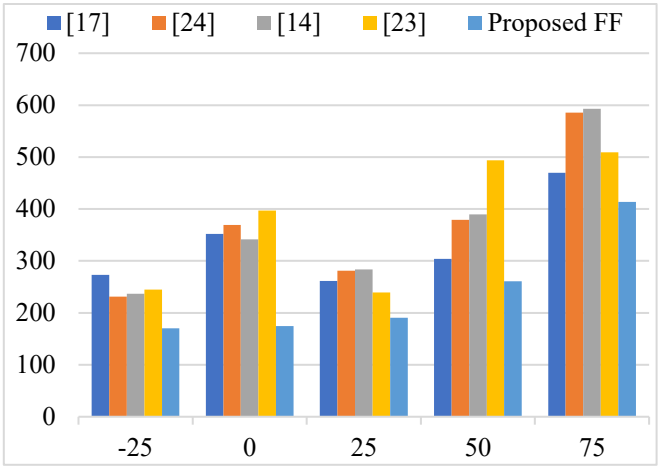

Fig. 10 Power utilization of the proposed Flip-Flop (FF) compared to current FFs w.r.t variations in temperature

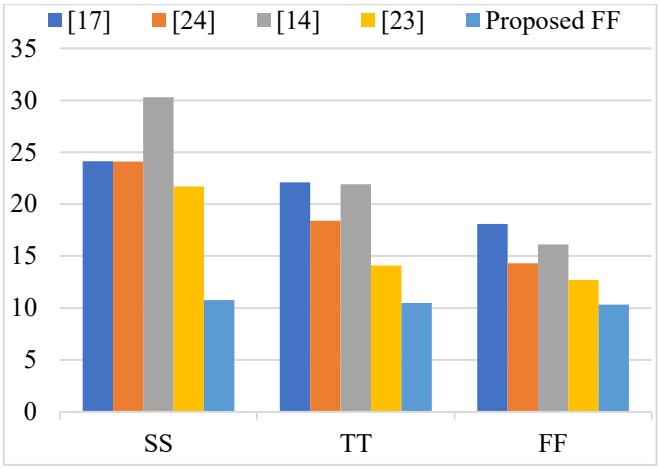

Fig. 11 Delay of the suggsted Flip-Flop (FF) w.r.t current FFs under various process variations

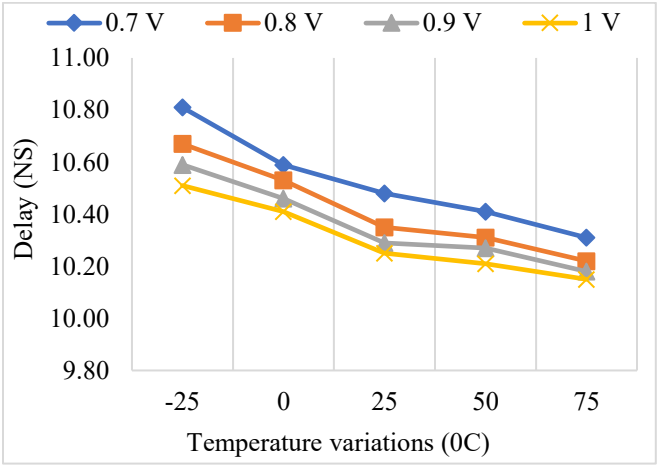

Fig. 12 Delay of the suggsted Flip-Flop (FF) w.r.t current FFs under various temperature variations

This article assesses the delay across the temperature spectrum of -25^0 - 75^0 Celsius. We do the assessment throughout the whole voltage range ranging from 0.7 to 1.0 V. Figure 12 demonstrates the corresponding variation of delay with respect to temperature. The suggested solution exhibits FF circuitry's ability to reduce power usage while minimizing circuit complexity. Ideal power utilization is especially important for low-power operations because it enables multiple operations to operate concurrently and effectively, resulting in improved system performance.

Table 2. Performance analysis of delay and power consumption of the proposed Flip-Flop (FF) for various clock frequency variations

Clock Frequency (GHz)	Power Consumption(nW)	Delay (ns)
0.05	176.6	11.48
0.1	232.2	10.3
0.2	259.3	10.6

To investigate the power-delay tradeoff, the proposed flip-flop device was simulated with various clock speeds and supply voltages. The findings are shown in Table 2. As shown in Figures 6-10, increasing the clock rate from 0.05 to 0.2 GHz decreases latency from 11.48 ns to 10.6 ns while increasing power consumption from 176.6 nW to 259.3 mW. Furthermore, decreasing supply voltages saves power consumption while increasing delay. The suggested design, as shown in Table 2, strikes an acceptable balance between power consumption and delay; however, the tradeoff analysis implies that more optimization may be accomplished by adjusting the clock rate and source voltage.

3.2. Analysis of Proposed Shift-Registers

According to section 3.1, in accordance with the examination of the FFs, the suggested FF performs better in terms of power consumption and latency. As a result, the planned FF has been implemented in the 4-bit SISO and PIPO registers. The PVT study of the 4-bit SISO and PIPO registers was performed to determine the stability of the shift registers.

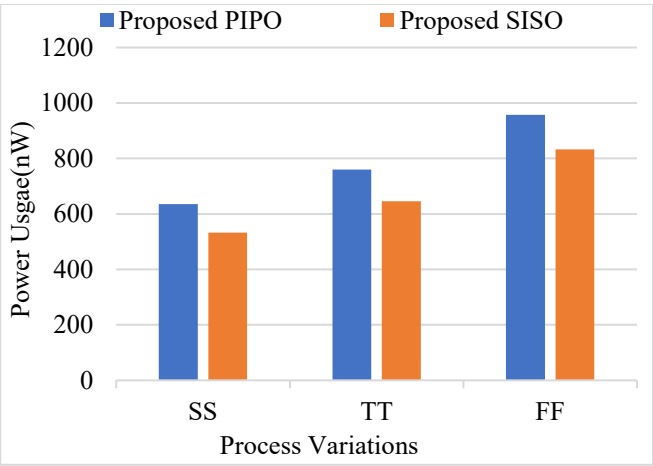

Fig. 13 Power utilization of the suggsted 4-bit shift registers under various Process variations

Figures 13-17 demonstrate that the recommended 4-bit shift registers achieve the PVT criterion. It uses less power and operates slower at the SS corner and vice versa at the FF corner. Furthermore, when the temperature rises, power utilization increases while delay decreases.

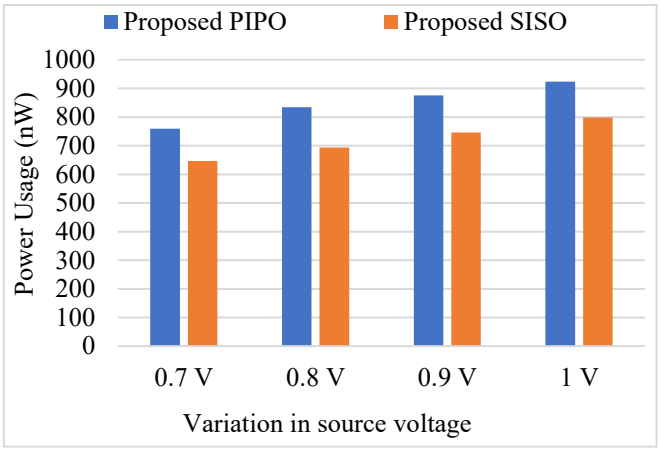

Fig. 14 Power utilization of the suggsted 4-bit shift registers under various source voltage variations

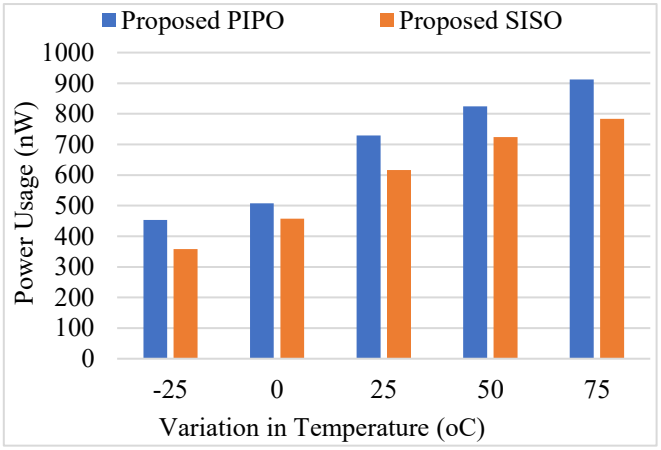

Fig. 15 Power utilization of the suggsted 4-bit shift registers under various temperature variations

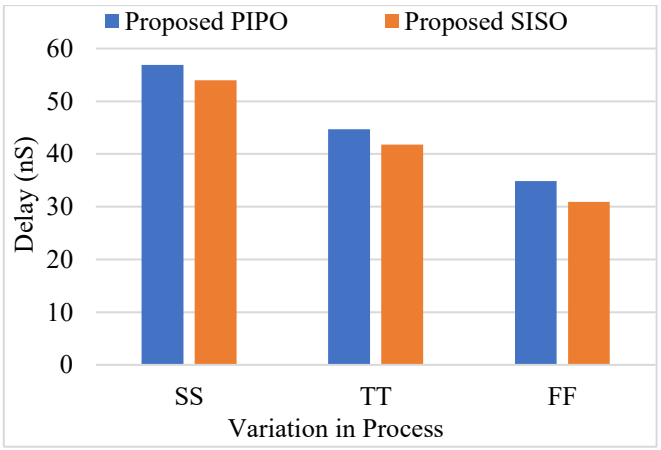

Fig. 16 Delay of the suggsted 4-bit shift registers under various Process variations

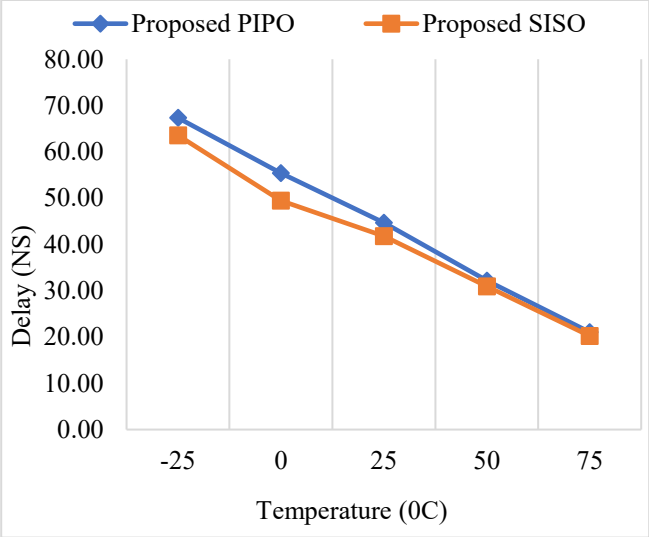

Fig. 17 Delay of the suggsted 4-bit shift registers under various temperature variations at 0.7V

4. Conclusion

This article presents low-power, compacted 4-bit PIPO, as well as SISO shift registers that include an implicitly triggered hybrid logic flip-flop. The suggested flip-flop has been designed with four clocked devices, which decreases power utilization. The suggested circuit has been designed using fewer transistors than its equivalents. The design has 16 devices, and it has been simulated with 18 nm finFET technology with a 0.7 V power supply. The suggested flip-flop architecture employs hybrid logic transistors that decrease power consumption by a minimum of 45% compared to earlier designs across many process corners. The suggested flip-flop consumes at least 15% less power throughout a broad supply voltage range of 0.7V to 1V, surpassing previous devices in this aspect. The proposed flip-flop is at least 20% faster than existing flip-flops across all process variations. The proposed 4-bit shift registers meet the PVT requirement. Moreover, when the temperature escalates, power consumption intensifies while latency diminishes.

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