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Original Article

Design of Stable 10T FinFET SRAM Cell for Operation in Sub-Threshold Regime

Ajjay S. Gaadhe[1], Yuvraj V. Parkale[2]

[1]*Department of Electronics and Telecommunication, PCET's Pimpri Chinchwad College of Engineering, Pune, India.*
[1,2]*Department of Electronics and Telecommunication, SVPM's College of Engineering, Malegaon (BK), Savitribai Phule Pune University, Baramati, Pune, India.*

[1]*Corresponding Author : ajjaygaadhe@gmail.com*

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Abstract - *The growing prevalence of portable electronic devices has led to an increased reliance on static random-access memory (SRAM) as a critical element in contemporary VLSI circuit design. To meet the rising demand for energy-efficient operation, sub-threshold SRAM design has gained attention for its ability to reduce power consumption. However, this approach presents challenges in maintaining adequate stability. This work investigates the development and evaluation of a 10-transistor (10T) FinFET SRAM bit cell to enhance stability. The paper provides complete design parameters along with an analysis of fin dimensions because they control the electrical performance in 10T SRAM cells. When properly set, fin width and height configurations allow drive strength and leakage balance, leading to increased noise margin performance. The proposed fin configuration and a separate read and write path establish an effective breakdown between read and write operations. The separation between read and write operations and control of drive strength of transistors enhances the stability of the entire system by preventing read disturbances when writing occurs, as well as write disturbances during reading. All simulations were executed through the Microwind 3.9 environment operated with 14 nm FinFET process technology. The results indicate that the 10T SRAM cell demonstrates significantly enhanced stability compared to the conventional CMOS and 6-transistor (6T) FinFET design. In particular, the 10T cell exhibits improvements of 65% in Read Static Noise Margin (RSNM) compared to conventional CMOS technology, maintaining the Write Static Noise Margin (WSNM) with incremental improvement. Besides, 10T FinFET cell demonstrates 4% improvement in RSNM and WSNM compared t 6T FinFET at the 14 nm technology node. These findings suggest that careful device sizing and architectural modifications can enhance SRAM reliability in advanced technology nodes.*

Keywords - *VLSI, Microelectronics, FinFET, Write ability, Read stability, Static noise margin, Power.*

1. Introduction

The advancement of System-on-Chip (SoC) technology and nanotechnology has significantly contributed to the growing importance of Static Random Access Memory (SRAM) in VLSI circuit designs. In recent years, SoC architectures have evolved rapidly, integrating diverse components onto a single chip to support high-performance and compact systems. SRAM plays a vital role in these architectures by providing high-speed, low-latency data storage, essential for a wide range of real-time and embedded applications. As SoC designs become increasingly complex, maintaining the stability of on-chip memory elements has become a critical concern. Technology scaling has been widely adopted to enhance performance parameters such as power consumption and silicon area. However, as technology nodes shrink, SRAM cells become more vulnerable to process variations and external noise, which can compromise their stability [1, 2]. Dynamic power reduction through voltage scaling is common in low-power design strategies. While this approach achieves substantial power savings, it also reduces the Static Noise Margin (SNM), thus affecting the overall reliability of the memory [3]. In SRAM cell design, key design metrics include stability, area, power, and access delay. Increased design complexity and higher transistor density in a limited silicon area contribute to increased delay [4]. Moreover, low-threshold voltage (Vth) transistors can degrade performance, whereas higher Vth values may increase leakage current and further impact cell stability [5]. To extend the battery life of portable devices, designers often adopt power-saving strategies, leading to aggressive CMOS scaling. This trend contributes to improved performance in speed, power efficiency, and reduced area [6]. Researchers have increased SRAM cell density by scaling down device dimensions to boost system performance. However, this scale-down approach introduces several challenges in the nanometer regime. As feature sizes shrink, maintaining high yield, performance consistency, and reliability becomes increasingly difficult.

With the ongoing advancement of technology, there is an increasing demand for microprocessors that combine higher speeds with lower power consumption. As transistor dimensions shrink, chip density rises, increasing the demand for careful power management. With continuous scaling, leakage power has significantly contributed to overall power dissipation. Voltage scaling remains an effective method to reduce power consumption in SRAM cells [7]. However, lowering the supply voltage in scaled CMOS technologies can significantly affect data stability, limiting the reliability of the SRAM cell. Consequently, simply decreasing VDD is not a sustainable solution, as the resulting increase in leakage current can compromise SRAM stability. While CMOS technology has traditionally been favored for SRAM design, its effectiveness diminishes at smaller process nodes [8]. This is largely due to short-channel effects (SCEs). Although various techniques, such as adopting high-k dielectric materials, have been employed to mitigate these effects, SCEs remain a significant challenge. FinFET technology has emerged as a promising candidate due to its superior electrostatic control and reduced leakage characteristics, making it well-suited for future low-power SRAM applications [9].

Scientific teams at the University of California, Berkeley, in 1999 created FinFET technology as an advanced version of standard planar CMOS technology to facilitate nanoscale applications [10]. The gate surrounds the channel three-dimensionally, thanks to its distinctive structure of vertical fins protruding from the substrate, thus enabling superior electrostatic control. The structure effectively controls leakage currents and SCEs as device dimensions become smaller. Equation 1 specifies the effective channel width measurement for a FinFET system.

$$Wch = N\ (2 * Hfin + Tfin) \quad (1)$$

N : Number of fins,
Hfin : The fin height
Tfin : Fin thickness

Researchers agree that FinFETs work optimally for SRAM development because these features enable lower leakage power consumption, enhanced drive current, and reduced switching voltage operations [11]. The performance characteristics of SRAM cells built with FinFET technology are improved by enhanced static noise margin and faster switching ability, according to research in [12]. A conventional 6T SRAM cell using FinFETs encounters substantial issues because it fails to write properly at low supply levels. The half-select problem makes unaccessed memory cells unstable during both read and write operations, according to [13]. Several SRAM architectures have been explored to improve SNM, power, and performance. Although area-efficient, the traditional 6T SRAM faces stability issues under low-voltage operation [13]. The limitations of standard SRAM cells led researchers to develop different modified SRAM architectures, improving stability, boosting static noise margin capabilities, and decreasing total power usage. SRAM cells require optimal transistor scaling as an essential step toward maintaining their operational stability. The static noise margin (SNM) and operational stability of the cell both directly result from proper adjustments of the cell ratio (CR) and pull-up ratio (PR) [14]. The 8T and 9T designs [14] add extra transistors for read isolation but still struggle with writeability at reduced voltages. The 10T designs proposed in [16, 21] introduce separate read/write paths but lack detailed fin dimension analysis. Furthermore, most existing solutions focus on planar CMOS technology or generic FinFET sizing without exploring geometric-level optimizations.

This study bridges the gap by introducing a FinFET optimized 10T cell with asymmetric fin distribution, providing superior RSNM and WSNM. Prior studies have not quantified the effect of CR and PR tuning on FinFET-based SRAM performance under sub-threshold operation. Designing SRAM systems requires selecting appropriate transistor dimensions since this choice ensures trustworthy operation in modern technology nodes. This study addresses a critical gap in the literature, the lack of geometrically optimized FinFET-based 10T SRAM designs that simultaneously enhance read and write SNMs in sub-threshold regimes. Most existing works do not fully utilize the fin dimension tunability offered by FinFETs to balance read and write performance. Therefore, we introduce a 10T SRAM cell with a fin allocation strategy tailored to optimize CR and PR, enabling robust operation under low-voltage conditions. The research introduces 6T [15] and 10T [16] SRAM cells through a design approach that optimises cell and pull-up ratios to enhance read and write stability. A stability is carried out for both SRAM cells at the 14nm technology level.

The goal of the research work is :

- To design a 10T SRAM cell with separate read/write paths using 14 nm FinFET technology.
- To apply geometric fin tuning to maximize RSNM and WSNM.
- To compare the proposed cell against conventional 6T and 10T designs regarding SNM, stability, and write-ability.

The novelty of this work lies in the explicit optimization of fin dimensions to achieve a high-performance 10T SRAM design in FinFET technology. The key contributions of the paper are:

- Fin Allocation Strategy for Enhanced Cell Stability: A central contribution of this work is demonstrating that the strategic allocation of fins among the transistors in a FinFET-based 10T SRAM cell can significantly improve

cell stability. By assigning more fins to the pull-down NMOS transistors than to the access transistors—thus adopting an asymmetric configuration—we ensure a higher cell ratio (CR), which directly enhances the pull-down strength during read operations. This results in a measurable improvement in the read Static Noise Margin (SNM). Simultaneously, by maintaining the pull-up ratio (PR) at or below unity, the write-ability of the cell remains unaffected. This approach allows optimized read and write margins through geometric fin-level tuning, a key advantage in FinFET-based SRAM design.

- Identification of Optimal CR and PR Ranges: We further establish the optimal design windows for achieving balanced performance by characterizing the relationship between transistor sizing and cell behavior. Our results show that a cell ratio of 1.5 to 3.0 and a pull-up ratio between 0.2 and 1.0 provide the most effective trade-off between read stability and write functionality. These ranges guide designers toward configurations that leverage FinFET structural advantages while meeting the stringent demands of modern SRAM architectures. This insight is a practical design reference for optimizing SRAM cells at advanced technology nodes.

2. SRAM Topology

2.1. 6T SRAM Cell

The six-transistor (6T) SRAM cell, as shown in Figure 1, is comprised of two cross-coupled inverters (formed by transistors M1–M4) and two access transistors (M5 and M6). These inverters store a single bit of data by maintaining a stable logic state, while the access transistors act as switches that connect the cell to the bit lines (BL and BLB) during read and write operations. The Word Line (WL) controls both access transistors, enabling or disabling interaction with the bit lines depending on the operation.

During a read operation, WL is activated (set to HIGH), turning on the access transistors and allowing the internal data of the cell to be sensed through the BL and BLB. The data on BL and BLB reflect the logic locked in the memory, with sense amplifiers used to interpret the small voltage difference between them. This process requires the cell to remain stable under read stress, without disturbing its content. In a write operation, the WL is again driven HIGH to provide access to the cell, while the bit lines are actively driven with complementary data values. One-bit is held HIGH and the other LOW, depending on the bit to be written.

This differential forces the internal nodes of the inverters to flip to the new value, effectively overwriting the stored data. For the write to succeed, the drivers on the bit lines must be strong enough to overpower the feedback from the cell's inverters, which can be particularly challenging as supply voltages scale down and cell stability becomes more sensitive.

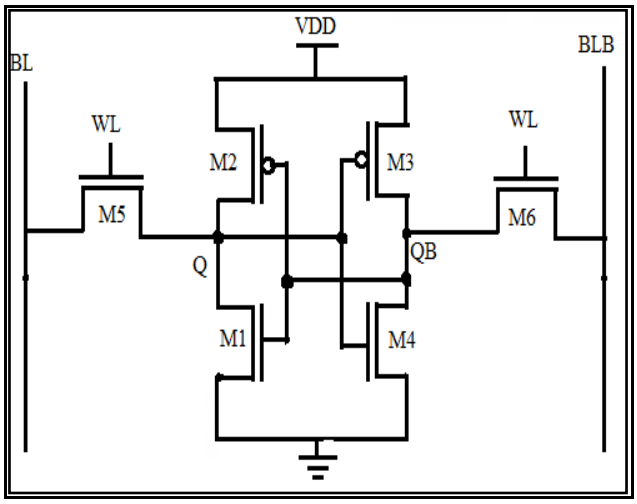

Fig. 1 6T SRAM Cell [15]

2.2. 10T SRAM Cell

Figure 2 presents a 10-transistor (10T) SRAM cell that employs dedicated transistors for read and write operations, allowing both to occur independently. In read mode, the Read Word Line (RWL) is set to a high logic level, activating the read access path, while the Write Word Line (WWL) remains low to prevent unintended write operations. Before reading begins, BL and BR are pre-charged to a HIGH level to prepare for sensing. Let us assume the cell stores a '0' at node VL and a '1' at node VR.

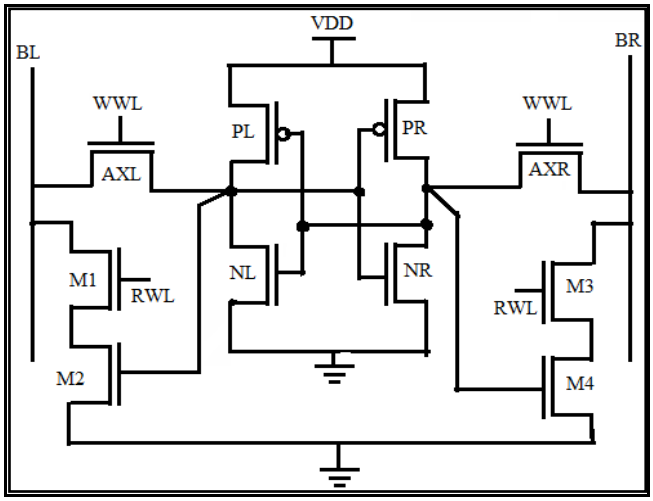

Fig. 2 10T SRAM Cell [16]

When the Read Word Line (RWL) is asserted high, the read access transistor associated with node VR is activated. Given that VR holds a high logic level, it, in turn, enables the bottom-right NMOS transistor to establish a conductive path to ground for the bit-line BR. This causes BR to discharge, indicating that a logical '1' is stored at VR. Conversely, if the node VL holds a logical '1', the BL will discharge through the bottom-left NMOS transistor connected to VL. This selective discharge mechanism enables the sense amplifiers to reliably

detect the stored data without altering the cell's contents, thus maintaining the read operation's integrity and stability. During SRAM cell write mode, the positioning of control signals operates in an opposite sequence to the read mode through the 10T cell. The 10-transistor (10T) SRAM cell uses Write Word Line (WWL) set in high logic state to activate write access transistors while keeping Read Word Line (RWL) in low condition for secure read path separation. During cell writing, the system drives strong electric signals through BL and BR bit-lines to apply the intended data content and its complementary value. The Write Word Line (WWL) must achieve a high logic state to write a logic '1' to node VL.

The write driver activates BL by setting it high while simultaneously driving BR low when it aims to set VR to a logic '0'. The bit-lines can establish a low-resistance path to internal storage nodes when the WWL function is turned on. Due to their drive strength, the write circuitry can control the bit-lines, which store previously stored values, so writing operations happen deterministically and reliably. BL forces VL to a high level, and BR pulls VR down to a low level.

Once the new values are written, WWL is deactivated to turn off the write access transistors, effectively isolating the cell and allowing it to hold the new data through the positive feedback loop formed by the cross-coupled inverters. This separation of read and write paths in the 10T SRAM design enables robust and non-interfering operations and improves the cell's stability, especially during low-voltage or noise-sensitive scenarios.

3. Methodology

3.1. Read Stability

The stability mechanism of SRAM cells directly affects both memory operation reliability and precision. Data storage stability in RAM cells indicates their capacity to preserve information while disregarding electrical disturbances and manufacturing uncertainties [17]. The progressive reduction in transistor dimensions in modern technology nodes makes it harder to protect data from corruption. Various factors, including lower supply voltage, increased leakage currents and enhanced variability, result in significant reductions of SRAM cell stability.

The Static Noise Margin (SNM) measures the stability of an SRAM cell by determining its tolerance to noise voltage until a data flip occurs [17, 19]. A visual and quantitative noise margin depiction is created through the butterfly curve technique by using the largest inscribed square from cross-coupled inverter VTC characteristics [20-23].

SRAM cell stability decreases because read operations increase its coupling with bit-lines, which causes additional stress on the cell. The SNM evaluation occurs by examining VTC curve modifications during read operations. The size of the inscribed square in the butterfly curve directly indicates how robust the cell is against noise during a read. This read SNM is commonly extracted through DC simulation techniques, providing valuable insight into the cell's performance under operational stress, as illustrated in Figure 3.

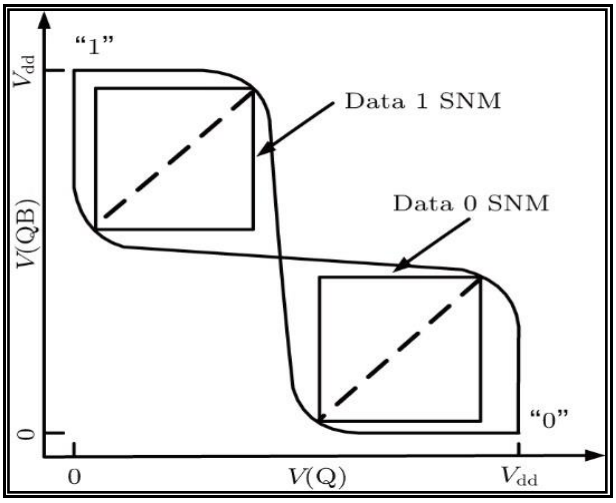

Fig. 3 SNM calculation using Butterfly curve [15]

3.2 Write Ability and WSNM Analysis

The SRAM cell's capability to accept new data through writing determines its reliability in memory operations at scales where technology sizes decrease. Reduced supply voltages and increased process variations result in increased difficulty with cell writing, thus making write ability assessment critical. WSNM is a measurement metric to determine the amount of static noise an SRAM cell can endure during writing before data loss occurs. Several techniques have been developed to estimate WSNM, including sweeping the word-line voltage [24, 25], bit-line voltage [26, 27], and using analytical methods that model the cell's behaviour [28, 29]. This study adopts the WL sweep method [26] to find the write noise margin.

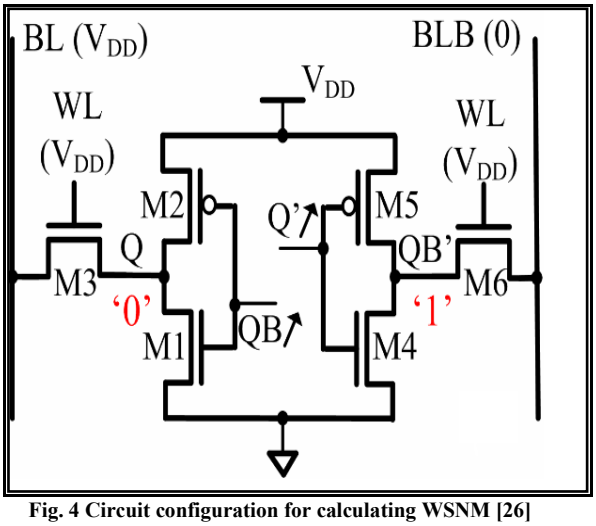

Fig. 4 Circuit configuration for calculating WSNM [26]

Figure 4 shows the write operation for a standard 6T SRAM cell, where a logic 'HIGH' state is successfully ported into the cell. This representation helps highlight how the cell responds during a write event and gives insight into its stability under real operating conditions.

4. Results and Discussion

SRAM cell architecture determines memory subsystems' overall performance, stability, and energy efficiency. Among the many design evolutions, the shift from the traditional 6-transistor (6T) cell to the more advanced 10-transistor (10T) cell represents a significant step toward enhanced static noise margin (SNM) performance, particularly when comparing CMOS and FinFET technologies. A defining feature of the 10T SRAM cell is its separate read and write ports, which fundamentally reconfigure how data is accessed and manipulated. This separation addresses critical limitations of conventional 6T SRAM cells, especially regarding read and write stability.

4.1. Design Considerations

The 10-transistor (10T) SRAM cell design uses 14 nm FinFET technology, which offers superior electrostatic control and reduced short-channel effects compared to traditional planar MOSFETs. Table 1 shows the environmental setup for simulating a 10T FinFET SRAM cell.

Table 1. The simulation environmental setup

Parameters	Setup
Transistor Device	FinFET
Technological Node(nm)	14
Temperature (°C)	27
Supply Voltage (V)	0.8

To achieve reliable operation, the number of fins in the FinFET devices is carefully optimized to regulate CR and PR. Both CR and PR are essential in ensuring the stability of the SRAM cell during read and write operations, particularly in preventing read disturbance and write failure.

The drive strength of each transistor in a FinFET-based circuit is directly influenced by the effective channel width, which in turn depends on the number of fins per device.

Unlike planar transistors, where the width can be continuously varied, the width in FinFETs is quantized and defined by the number of vertical fins. The effect of CR and PR on the performance of the SRAM cell is shown in Table 2.

Table 2. Effect of CR-PR on noise margin

6T SRAM Cell	RSNM	WSNM
(CR,PR) = (3,6)	115mV	66mV
(CR,PR) = (3,3)	106mV	100mV
(CR,PR) = (3,2)	97mV	127mV
(CR,PR) = (3,1)	78mV	189mV

Table 2 highlights the limitations of the 6T SRAM cell. The increased value of PR degrades the write performance and improves the read performance of the SRAM cell. The 10T SRAM cell has addressed the limitation with isolated read and write access transistors, enabling better read and write stability performance. The performance further improved using a FinFET-based SRAM cell by effectively sizing the fins of transistors. Due to its fin-based design, the FinFET-based SRAM cell allows a maximum transistor width in a smaller area. As shown in Table 2, CR, i.e effective width of pull-down transistor to width of access transistor, is maintained as 1.5 and PR, i.e effective width of pull-up transistor to access transistor, is maintained as 1. Thus, keeping CR=1.5 and PR=1 gives better performance than CMOS-based SRAM cells. This optimum value of CR and PR is to be maintained in the 6T SRAM cell due to common access transistors for read-write operations. In a 10T SRAM cell with separate read and write access transistors, maintaining the higher CR and lower PR independently strengthens the read and write performance. Thus, as shown in Table 3, in a 10T FinFET SRAM cell, CR =2 and PR=0.5 are maintained. The width is calculated using equation 1. Fin pitch denotes the effective width of the transistor.

Fin Thickness(WFin)=8nm;
Fin Height(HFin) = 40nm;
Fin pitch =40nm
W=2HFin+WFin

Table 3. Effective width of transistors in 6T SRAM cell

6T SRAM Cell	Pull Up Transistor	Pull Down Transistor	Access Transistors
Number of Fins	2	3	2
Width	176nm	264nm	176nm

Table 4. Effective width of transistors in 10T SRAM cell

10T SRAM Cell	Pull Up Transistor	Pull Down Transistor	Write Access Transistors	Read Access Transistors
Number of Fins	1	4	2	2
Width	88nm	352nm	176nm	176nm

Tables 3 and 4 show the effective width of transistors, as per equation 1, to maintain the cell and pull-up ratios to enable successful read and write operations.

4.2. Improved Read Stability and Write Capability

One of the primary limitations of the 6T SRAM cell lies in the vulnerability of its read operation. In 6T cells, the read process occurs through the same access path that connects to the storage nodes, which can disturb the stored data, especially under low-voltage conditions or process variation. Figure 5 shows the RSNM of a 10T SRAM cell, calculated using the butterfly curve method. The 10T SRAM architecture mitigates

this issue through dedicated read ports that decouple the read path from the storage node. As a result, the stored data is no longer directly exposed during a read operation, significantly improving the Read Static Noise Margin (RSNM).

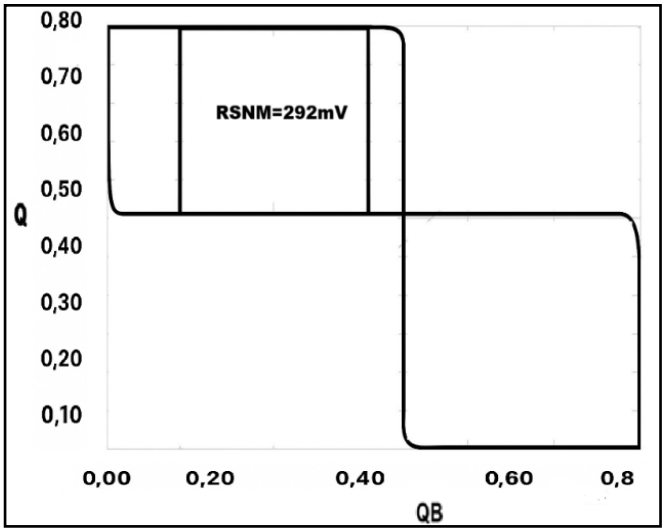

Fig. 5 RSNM of 10T SRAM cell (RSNM=292mV)

The WSNM is evaluated using the word line WLL sweep method. As stated in [26], word line WWL is swept from 0 to 0.8 V. As shown in Figure 6, the value of WWL where the node voltage drops to 50% is noted and, as per the methodology in [26], is subtracted from the supply voltage 0.8V. Thus, the value at which node voltage QB switched is 0.58V, and thus WSNM = 0.8 - 0.57 = 230mV.

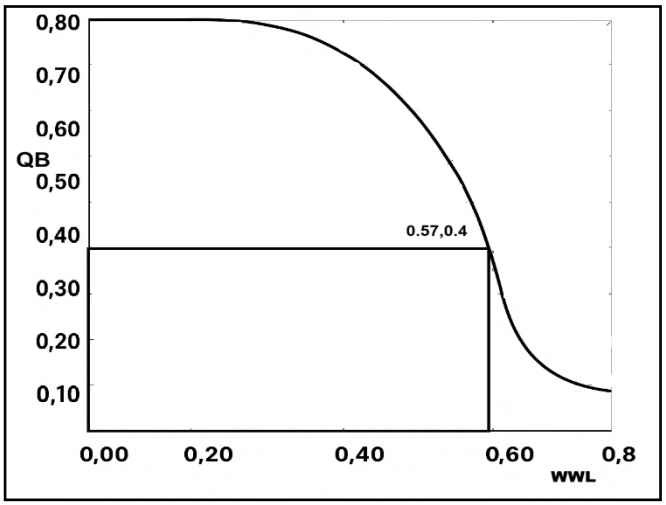

Fig. 6 WSNM of 10T SRAM cell (WSNM=230mV)

Table 5. Comparative performance analysis

Topology/ Parameter	RSNM(mV)		WSNM(mV)	
	CMOS	FINFET	CMOS	FINFET
6T	115	280	66	220
10T	176	292	227	230

Table 5 outlines the comparative performance of the 6T and 10T SRAM cells. Figure 7 shows the 10T SRAM cell improvement on RSNM and WSNM. In 10T SRAMs, the RSNM improves markedly from 176 mV in CMOS cells to 292 mV in 10T FinFET cells, representing a 65% enhancement. In FinFET technology, which inherently offers better electrostatic control, the RSNM increases from 280 mV in the 6T cell to 292 mV in the 10T cell, indicating that even with already high stability, the 10T design provides additional robustness.

This improvement reflects the architectural advantage of isolating critical operations, reducing data corruption risk and enhancing read reliability. The improved performance of the 10T SRAM cell with the proposed design parameters outperforms the conventional 6T SRAM cell.

Write stability is another crucial performance metric, and in 6T cells, it often suffers due to the contention between access transistors and the feedback loop that maintains data integrity. This makes the writing process particularly difficult, especially in CMOS designs operating at low power. The 10T SRAM's dedicated write ports enable a more direct and controlled write mechanism, easing this contention and significantly improving the Write Static Noise Margin (WSNM). Figure 6 shows the improvement of a 10T SRAM cell on RSNM and WSNM.

For CMOS technology, the WSNM sees an increase from 66 mV in the 6T design to 227 mV in the 10T configuration, indicating a 244% improvement. In FinFET-based SRAMs, the WSNM improves modestly from 220 mV to 230 mV, further reinforcing the value of the 10T cell even in advanced technologies. This enhancement is particularly beneficial for modern low-voltage applications where maintaining strong writability is often challenging.

A traditional 6T SRAM design has an inherent trade-off between read and write stability. Design optimisations that improve RSNM typically compromise WSNM, and vice versa. This constraint significantly limits the performance envelope of 6T cells.

The 10T SRAM design breaks this trade-off by decoupling the read and write operations. By introducing separate ports for each function, the design allows simultaneous optimization of both read and write stability metrics.

This decoupling enables a more flexible design strategy, which is particularly valuable in emerging technologies where variability and power constraints are more pronounced. As seen from the SNM values across both CMOS and FinFET technologies, the 10T cell demonstrates robust performance improvements in RSNM and WSNM, validating the architectural shift.

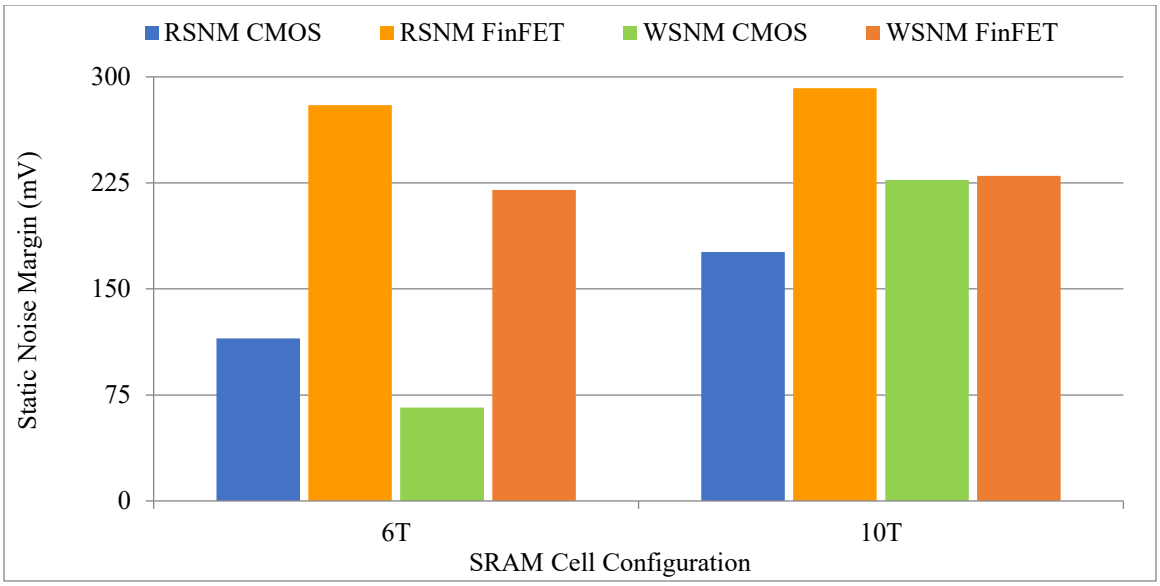

Fig. 7 Performance analysis of 6T and 10T SRAM cells using CMOS and FinFET technology

5. Conclusion

The research demonstrates that a 10-transistor (10T) SRAM cell with proposed design considerations establishes greater read and write operation stability than standard 6T versions in CMOS and FinFET technologies. Test results demonstrate that the 10T cell enhances Read Static Noise Margin (RSNM) by 65% compared to the 10T CMOS design, rising from 176 mV to 292 mV. The 10T architecture increases resistance by enhancing RSNM from 280 mV to 292 mV in devices based on FinFET technology, which features superior electrostatic control. Introducing 10T architecture increases CMOS WSNM levels by 244% from its original value of 66 mV in the 6T structure to 227 mV. Applying FinFET technology to the 10T cell design improves RSNM and WSNM by 4% over the standard 6T configuration. The 10T SRAM cell provides a powerful memory solution for upcoming memory systems because it works effectively in power-sensitive applications with low voltages, maintaining stability.

References

[1] Benton H. Calhoun, and Anantha P. Chandrakasan, "Static Noise Margin Variation for Sub-Threshold SRAM in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 7, pp. 1673-1679, 2006. [CrossRef] [Google Scholar] [Publisher Link]

[2] Seng Oon Toh et al., "Characterization of Dynamic SRAM Stability in 45nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 11, pp. 2702-2712, 2011. [CrossRef] [Google Scholar] [Publisher Link]

[3] Benton H.Calhoun, Alice Wang, and Anantha Chandrakasan, "Modeling and Sizing for Minimum Energy Operation in Subthreshold Circuits," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 9, pp. 1778-1786, 2005. [CrossRef] [Google Scholar] [Publisher Link]

[4] Akshay Bhaskar, "Design and Analysis of Low Power SRAM Cells," *2017 Innovations in Power and Advanced Computing Technologies (i-PACT)*, Vellore, India, pp. 1-5, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[5] Yu Cao et al., "The Predictive Technology Model in the Late Silicon Era and Beyond," *Foundations and Trends in Electronic Design Automation*, vol. 3, no. 4, pp. 305-401, 2008. [CrossRef] [Google Scholar] [Publisher Link]

[6] Mo Maggie Zhang, "Performance Comparison of SRAM Cells Implemented in 6, 7 and 8-Transistor Cell Topologies", *Electrical and Computer Engineering*, University of California, Davis, 2008. [Google Scholar] [Publisher Link]

[7] P. Upadhyay et al., "Read Stability and Power Analysis of a Proposed Novel 8 Transistor Static Random Access Memory Cell in 45 nm Technology," *Scientia Iranica: Transaction D*, vol. 21, no. 3, pp. 953-962, 2014. [Google Scholar] [Publisher Link]

[8] Rohit Lorenzo, and Saurabh Chaudhury A Novel 9T SRAM Architecture for Low Leakage and High Performance," *Analog Integrated Circuits and Signal Processing*, vol. 92, no. 2, pp. 315-325, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[9] Soumitra Pal et al., "Half-Select-Free Low-Power Dynamic Loop Cutting Write Assist SRAM Cell for Space Applications," *IEEE Transactions on Electronic Devices*, vol. 67, no. 1, pp. 80-89, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[10] Debajit Bhattacharya, and Niraj K. Jha, "FinFETs: From Devices to Architectures," *Advances in Electronics*, vol. 2014, no. 1, pp. 1-12, 2014. [CrossRef] [Google Scholar] [Publisher Link]

[11] Appikatla Phani Kumar, and Rohit Lorenzo, "Performance Analysis of DMG-GOS Junctionless FinFET with High-K Spacer," *2022 IEEE Silchar Subsection Conference (SILCON)*, Silchar, India, pp. 1-5, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[12] Mahmood Uddin Mohammed et al., "FinFET-Based SRAMs in Sub-10nm Domain," *Microelectronics Journal*, vol. 114, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[13] Gabriel Torrens et al., "A 65-nm Reliable 6T CMOS SRAM Cell with Minimum Size Transistors," *IEEE Transactions on Emerging Topics in Computing*, vol. 7, no. 3, pp. 447-455, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[14] Manpreet Kaur, and Ravi Kumar Sharma, "Comparative Parametric Analysis, For Stability of 6T and 8T SRAM Cell," *International Journal of Advances in Engineering & Technology*, vol. 5, no. 1, pp. 503-514, 2012. [Google Scholar] [Publisher Link]

[15] Shilpi Birla, R.K. Singh, and Manisha Pattnaik, "Static Noise Margin Analysis of Various SRAM Topologies," *IACSIT International Journal of Engineering and Technology*, vol. 3, no. 3, pp. 304-306, 2011. [CrossRef] [Google Scholar] [Publisher Link]

[16] Sayeed Ahmad, Naushad Alam, and Mohd. Hasan, "A Robust 10T SRAM Cell with Enhanced Read Operation," *International Journal of Computer Applications*, vol. 129, no. 2, pp. 7-12, 2015. [CrossRef] [Google Scholar] [Publisher Link]

[17] Aswathy A. Kumar, and Anu Chalil, "Performance Analysis of 6T SRAM Cell on Planar and FinFET Technology," *2019 International Conference on Communication and Signal Processing*, Chennai, India, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[18] Evert Seevinck et al., "Static-Noise Margin Analysis of MOS SRAM Cells," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 5, pp. 748-754, 1987. [CrossRef] [Google Scholar] [Publisher Link]

[19] Surbhi Bharti et al., "Performance Analysis of SRAM Cell Designed using MOS and Floating-Gate MOS for Ultralow Power Technology," *2019 4th International Conference on Internet of Things: Smart Innovation and Usages (IoT-SIU)*, Ghaziabad, India, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[20] Rohit Lorenzo, and Saurabh Chaudhury, "A Novel SRAM Cell Design with a Body-Bias Controller Circuit for Low Leakage, High Speed and Improved Stability," *Wireless Personal Communications*, vol. 94, no. 4, pp. 3513-3529, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[21] Himanshu Banga, and Dheeraj Agarwal, "Single bit-line 10T SRAM cell for low power and high SNM," *2017 International Conference on Recent Innovations in Signal Processing and Embedded Systems (RISE)*, Bhopal, India, pp. 433- 438, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[22] Evert Seevinck et al., "Static-Noise Margin Analysis of MOS SRAM Cells," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 5, pp. 748-754, 1987. [CrossRef] [Google Scholar] [Publisher Link]

[23] Chandrabhan Kushwah, and Santosh K. Vishvakarma, "Ultra-Low Power Sub-threshold SRAM Cell Design to Improve Read Static Noise Margin," *Progress in VLSI Design and Test*, Springer, Berlin, Heidelberg, vol. 7373, pp. 139-146, 2012. [CrossRef] [Google Scholar] [Publisher Link]

[24] Koichi Takeda et al., "Redefinition of Write Margin for Next-Generation SRAM and Write-Margin Monitoring Circuit," *2006 IEEE International Solid State Circuits Conference-Digest of Technical Papers*, San Francisco, CA, USA, pp. 2602-2611, 2006. [CrossRef] [Google Scholar] [Publisher Link]

[25] Nicolas Gierczynski et al., A New Combined Methodology for Write-Margin Extraction of Advanced SRAM," *2007 IEEE International Conference on Microelectronic Test Structures*, Bunkyo-ku, Japan, pp. 97-100, 2007. [CrossRef] [Google Scholar] [Publisher Link]

[26] Jiajing Wang et al., Analyzing Static and Dynamic Write Margin for Nanometer SRAMs," *Proceedings of the 2008 international symposium on Low Power Electronics & Design*, Bangalore India, pp. 129-134, 2008. [CrossRef] [Google Scholar] [Publisher Link]

[27] Kevin Zhang et al.: A 3-GHz70-mb SRAM in 65-nm CMOS Technology with Integrated Column-Based Dynamic Power Supply," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 1, pp. 146-151, 2005. [CrossRef] [Google Scholar] [Publisher Link]

[28] Ruchi, and Sudeb Dasgupta, "Compact Analytical Model to Extract Write Static Noise Margin (wsnm)for SRAM Cell at 45-nm and 65-nm Nodes," *IEEE Transactions on Semiconductor Manufacturing*, vol. 31, no. 1, pp. 136-143, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[29] Evert Seevinck, Frans J. List, and Jan Lohstroh, "Static-Noise Margin Analysis of MOS SRAM Cells," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 5, pp. 748-754, 1987. [CrossRef] [Google Scholar] [Publisher Link]