

Original Article

Power Quality Enhancement in Standalone DFIG-Based Wind Farms Using E²PLL-Controlled D-Statcom

M.Manohara¹, Y.N. Vijaya kumar², S. Sridhar³, T. Nageswara Prasad⁴, D Leela Rani⁵, B. Rajashekar⁶

¹Department of EEE, School of Engineering, Mohan Babu University, Andhra Pradesh, India.

²Department of EEE, Sri Venkateswara College of Engineering and Technology, Andhra Pradesh, India.

³Department of EEE, Geethanjali Institute of Science and Technology, Andhra Pradesh, India.

⁴Department of EEE, K.S.R.M. College of Engineering, Andhra Pradesh, India.

⁵Department of ECE, School of Engineering, Mohan Babu University, Andhra Pradesh, India.

⁶Management Trainee- Production, Meiden T&D Limited, Andhra Pradesh, India.

⁶Corresponding Author : krajashekar2002@gmail.com

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Abstract - Independent wind farms with Doubly Fed Induction Generators (DFIGs) often experience major overvoltage, harmonic distortion, and other power quality concerns, as well as transient disturbances [1]. This study implements a D-STATCOM system combined with Phase-Locked Loop (PLL) control to address voltage stability and enhance dynamic reactive power compensation [2]. The PLL-based control locks the system voltage, enabling synchronous operation and effective harmonic filtering [2]. A phase controller is incorporated within the D-STATCOM to further improve system response to increase damping against frequency variations and slow voltage magnitude changes. The created system is modeled in the MATLAB/Simulink platform, simulated, with the capability of DFIG-based wind farms to reduce power quality issues studied. Results demonstrate significant improvements in voltage stability, a marked reduction in harmonic content, and enhanced overall power quality performance [3]. These findings reinforce the potential of advanced D-STATCOM configurations in supporting reliable, high-quality power delivery from independent renewable energy sources [4].

Keywords - Doubly fed induction generators, Distribution static synchronous compensators, Phase-locked loop control, Reactive power compensation.

1. Introduction

Increased usage of wind energy is becoming vital to meet global energy demands, and the wind power is a major source, which is being affected by the intermittent character of the power output coupled with the changes in power conversions by power electronics, hence, introducing PQ issues such as the voltage distortion, harmonic current, and transient voltages at the PCC which are prospects of cost escalations and equipment failures as well as trip-outs [5].

These issues are even worse in open-loop Doubly Fed Induction Generator (DFIG) wind systems, given a bad network, and inefficiency of local compensation leading to poor voltage regulation, frequency drift and high Total Harmonic Distortion (THD) [6].

In addition to being fast-acting reactive power sources, voltage regulators, and harmonic dampers, Distribution Static Compensators (D-STATCOMs) also need synchronization methods. Standard synchronous schemes like Synchronous Reference Frame Phase-Locked Loop (SRF-PLL) and others

are ineffective with distorted or imbalanced voltages, while more recent techniques like Decoupled Double SRF (DDSRF), Second-Order Generalized Integrator (SOGI), and Enhanced PLL (EPLL) have limited capabilities when there are near-extreme perturbations and signal frequency variations [6]. Although synchronization plays a crucial role, there is a significant literature gap, with limited studies examining Enhanced PLL (E²PLL)-based control of D-STATCOMs in standalone microgrids under severe PQ conditions, as well as a general lack of comparative studies examining existing PLL techniques rather extensively.

To overcome this, this work presents and compares an E²PLL synchronized D-STATCOM controller to SRF, DDSRF, SOGI, and EPLL-based controllers over ideal PQ parameters of PCC voltage deviation, THD, negative-sequence components, DC-link ripple, and transient settling time, showing how the disturbance rejection stability and frequency tracking capabilities of E²PLL can enhance the performance of a standalone DFIG-based microgrid to improve power quality and stability of renewable-based systems [7].



2. D-Statcom-Based DFIG System

D-STATCOM is part of the system architecture depicted in Figure 1 below. This nonlinear, unbalanced demand is driven by a horizontal-axis, three-phase, Doubly-Fed Induction Generator (DFIG) connected to a star. A three-phase star-connected capacitor bank is proposed to be connected between the stator terminals of the DSTATCOM-based system to enable dynamic load regulation. The capacitor bank serves as a reactive power store, increasing the system's overall power support. The D-STATCOM interfaces with the incoming wire at the Point of Common Coupling (PCC). Besides offering system reactive power compensation and DFIG compensating, the D-STATCOM efficiently suppresses imbalances and nonlinearities. A Voltage Source Converter (VSC) using IGBTs, a three-phase coupling inductor (L_f) [8].

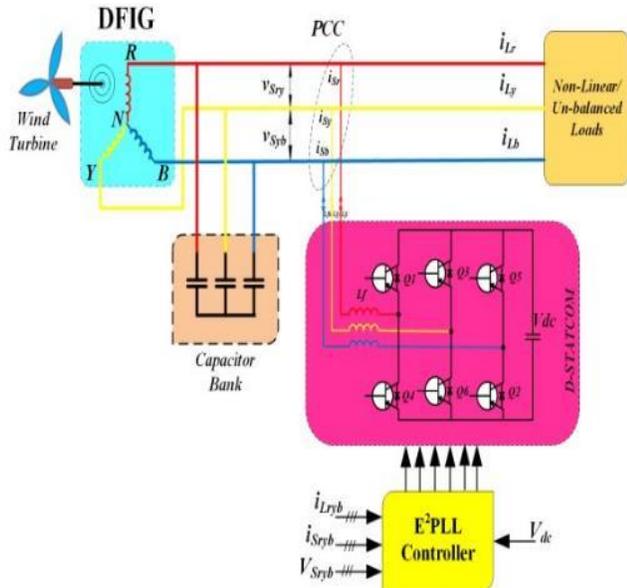


Fig. 1 Schematic of D-STATCOM-based DFIG system

3. E²PLL Control Technique

The implementation of power quality improvement starts when a control loop activates to detect and rectify PCC (Point of Common Coupling) faults. Real-time measurements of voltages alongside load currents detect all power quality anomalies, together with imbalanced reactive power and unstable voltages. Fundamental components are obtained from the load currents through an Enhanced Phase-Locked Loop (E²PLL) filtering before the D-STATCOM produces its necessary corrective outputs. The reference source currents are calculated according to the filtered values to achieve balanced operation and unity power factor while reducing distortion. The currents are then determined to prove useful in the active and reactive components' effective compensation.

To minimize power quality disturbances, a compensation current is fed to PCC, and switching pulses are produced at the drive voltage source convertors using the reference currents. The system would then use a measure of voltage stability and

the amount of Total Harmonic Distortion (THD) in evaluating power quality in an attempt to ensure that the standards of IEEE 519 or IEC 61000 are being maintained [9].

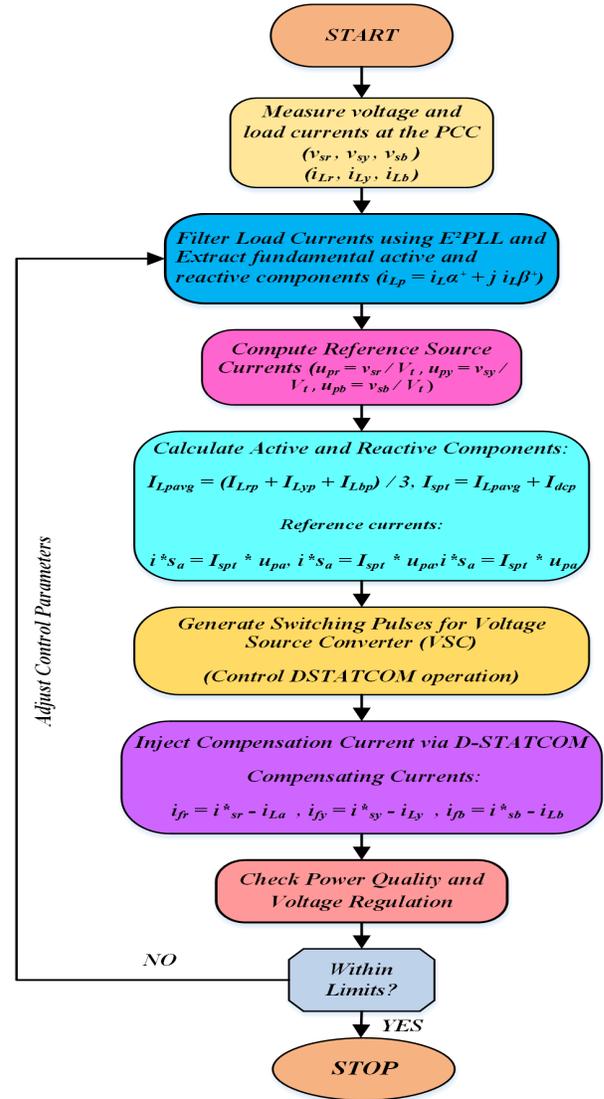


Fig. 2 Flowchart for control operation of E²PLL

3.1. E²PLL-Based Control Algorithm for DSTATCOM

The balanced E²PLL scheme is centered on oversampled two Modified Enhanced Phase-Locked Loops (MEPLLs) based capture. It is the optimistic reciprocal element of the oldest frequency and uses twin MEPLL. The MEPLL is purported to be implemented with a Phase Lock Loop (PLL) and a relative Adaptive Band-Pass Filter (ABPF) as shown in Figure 5 [10]. The filtering performance of the MEPLL gets improved through the implementation of a Moving Average Filter (MAF) into its error path ABPF [11]. Based on the filter output error signal, the PLL component acquires the frequency parameters and the phase characteristics of load currents. The MEPLL displays remarkable disturbance suppression capabilities relating to its internal frequency measurement

under changing frequencies [12]. The Positive Sequence Calculator (PSC) calculates Positive Sequence entries of the filtered currents. $i_{L\alpha}^+$ from $i_{L\alpha}$ and $i_{L\beta}^+$ from $i_{L\beta}$ Through its in-phase and quadrature-phase input terminals, as shown in Figure 4 [9]. The PSC unit processes data through the Instantaneous Symmetrical Components (ISC) technique, which can be explained as follows [13].

$$\begin{bmatrix} i_{L\alpha}^+ \\ i_{L\beta}^+ \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & j \\ -j & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_{L\alpha} \\ \hat{i}_{L\beta} \end{bmatrix} \quad (1)$$

A Moving Average Filter (MAF) is added into the QT1-PLL feedback loop, shown in Figure 3. Any of these can be used as a low-pass filter in the proper situation. The domain transfer function of this element is observed in reference [14].

$$\text{MAF}(s) = \frac{1 - e^{-T\omega s}}{T\omega s} \quad (2)$$

Where $T\omega$ is the span of the window of the MAF. In computer implementation using the z domain, we can have the z transfer function of the MAF given by

$$F(z) = \frac{1 - z^{-N}}{N(1 - z^{-1})} \quad (3)$$

Where f_s is the sampling rate and N is the quality of $f_s T\omega$. The MAF block diagram, Figure 6, can be generated by use of (3). It is clear that the MAF frame has a very simple structure, and this enhances its integration into the digital systems [14].

3.2. Controller for DSTATCOM

The control technique is illustrated in Figure 3 [15]. The most fundamental equations that relate the labels to each other are as follows: DC bus voltage (v_{dc}) and the reference source currents of DSTATCOM phases A, B and C can be decomposed into two groups according to supply voltages; in-phase (I_{Lp}) and quadrature (I_{Lq}).

$$v_{sr} = \frac{2v_{sry} + v_{syb}}{3} \quad (4)$$

$$v_{sy} = \frac{-v_{sry} + v_{syb}}{3} \quad (5)$$

$$v_{sb} = \frac{-v_{sry} - 2v_{syb}}{3} \quad (6)$$

The PCC voltages' peak value is calculated using the Equations (4), (5), and (6) as follows

$$V_t = \sqrt{\frac{2}{3}(v_{sr}^2 + v_{sy}^2 + v_{sb}^2)} \quad (7)$$

Equations (11),(12),(13) and (14) are utilized to create the in-phase unit magnitude voltage vectors as

$$u_{pr} = \frac{v_{sr}}{V_t} \quad u_{py} = \frac{v_{sy}}{V_t} \quad u_{pb} = \frac{v_{sb}}{V_t} \quad (8)$$

The quadrature unit voltage vectors have magnitudes of one.

$$u_{qr} = \frac{-u_{py} + u_{pb}}{\sqrt{3}} \quad (9)$$

$$u_{qy} = \frac{3u_{pr} + u_{py} - u_{pb}}{2\sqrt{3}} \quad (10)$$

$$u_{qb} = \frac{3u_{qr} + u_{qy} - u_{qb}}{2\sqrt{3}} \quad (11)$$

Approximation of low-order active (I_{lpr}) and reactive (I_{lqr}) load current components is determined using I_{lm} , u_{pr} , and u_{qr} elements, ZCD, and S&H circuit elements, as shown in Figure 3. The method used to obtain the rest of the active and reactive components remains consistent throughout this process [16].

3.3 Estimation of Essential Active Components

DC Bus Voltage (V_{dc}) of the rated voltage shall be properly controlled for D-STATCOM operation and operational reliability for any reference voltage value of (V_{dcref}). This must be under proper control through continuous monitoring and level comparison of the set point and actual DC buses.

The Proportional-Integral (PI) controller is the only controller that can provide fault compensation against anti-faulting since it senses the voltage, the difference of which is denoted [17].

Faulting is corrected in the system by PI controller regulation through the necessary active current (I_{dcp}). The mean value of fundamental active current (I_{lpavg}) may be calculated using Equation (12) and added to the PI-derived value of compensation current (I_{dcp}) generated in Equation (13) to provide the total active component of the reference current (I_{spt}). Suitable control of D-STATCOM enhances voltage stability in addition to enhancing power compensation efficiency [17].

$$I_{lpavg} = \frac{I_{Lrp} + I_{Lyp} + I_{Lbp}}{3} \quad (12)$$

$$I_{spt} = I_{lpavg} + I_{dcp} \quad (13)$$

Reference Current Nominal values of reference supply current in-phase component (i_{srp}^* , i_{syp}^* and i_{sbp}^*) are computed as

$$i_{srp}^* = I_{spt} u_{pr} \quad (14)$$

$$i_{syp}^* = I_{spt} u_{py} \quad (15)$$

$$i_{sbp}^* = I_{spt} u_{pb} \quad (16)$$

3.4. Estimation of Essential Reactive Components

Since the performance of the Double Fed Induction Generator (DFIG) depends on the output voltages that need to be kept at a steady pre-determined value (V_{tref}), then reactive power control would be necessary to make the Generator and the load demand commensurate. The difference between the reference voltage (V_{tref}) and the load voltage (V_t) yields a voltage error signal. A Proportional Integral (PI) controller,

which tracks the error online, is critical to determine the reactive current [17]. The total reactive reference current (I_{sq}) is obtained by the difference between the compensatory current and the compensatory current. The PI (I_{vtq}), as expressed in Equation (18), is calculated from the average load reactive current (I_{Lpavg}), as expressed in Equation (17). This approach guarantees proper voltage control and guarantees DFIG stability under different load conditions [19].

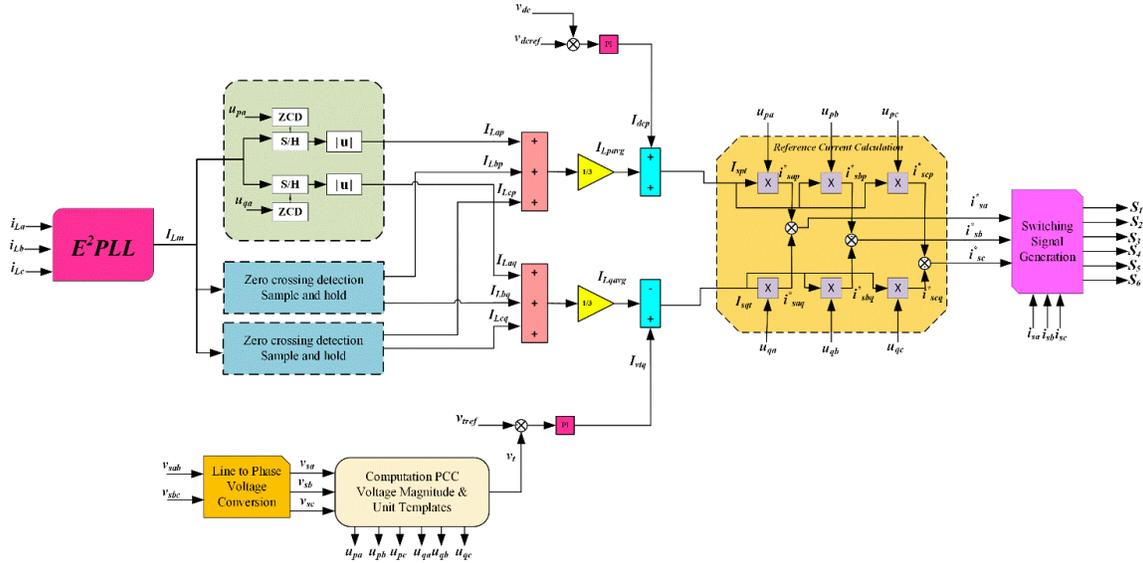


Fig. 3 E²PLL-based control technique for DSTATCOM

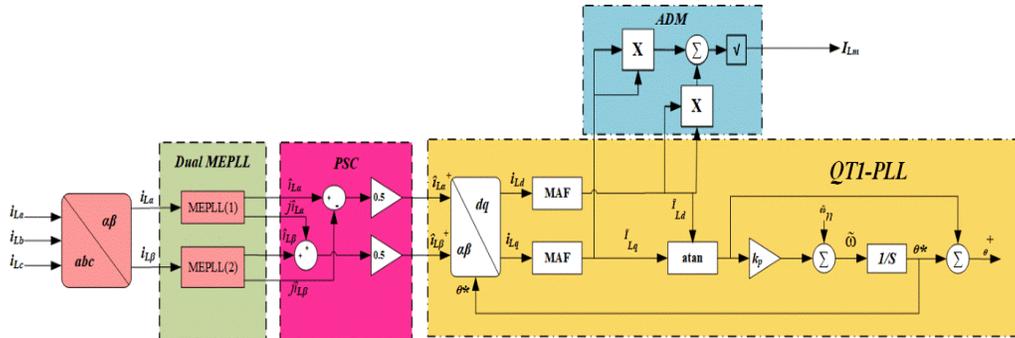


Fig. 4 Block diagram of E²PLL

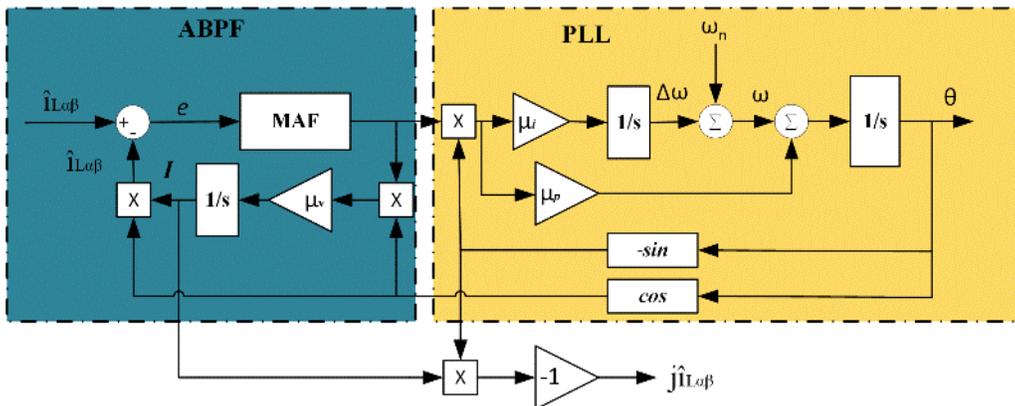


Fig. 5 Structure of MEPLLI

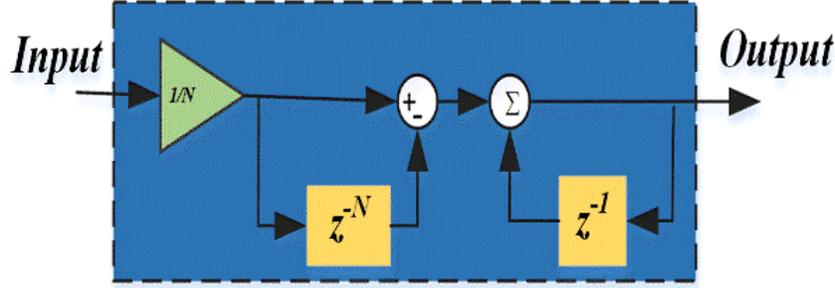


Fig. 6 Block diagram of MAF

$$I_{Lpavg} = \frac{I_{Lrp} + I_{Lyp} + I_{Lbp}}{3} \quad (17)$$

$$I_{sqt} = I_{vtq} - I_{Lqavg} \quad (18)$$

As shown in Equations (13)-(15), the reactive current component of each phase is determined by multiplying the Isqt value by the associated phase's quadrature unit templates [19].

$$i_{srq}^* = I_{sqt} u_{qr} \quad (19)$$

$$i_{syq}^* = I_{sqt} u_{qy} \quad (20)$$

$$i_{sbq}^* = I_{sqt} u_{qb} \quad (21)$$

The voltages of quadrature and supply reference current, as well as the amplitude of the in-phase supply reference current, are the results of the DC bus voltage PI controller.

The instantaneous reference currents (i_{sar}, i_{sbr} and i_{scr}) simple summation of in-phase supply reference currents (i_{srp}^*, i_{syp}^* and i_{sbp}^*) and quadrature supply reference currents (i_{srq}^*, i_{syq}^* and i_{sbq}^*).

Exchange values of its hysteresis supply source currents are also simultaneously shared with a carrier-less hysteresis PWM controller to give gate pulses to the IGBTs of DSTATCOM, reduced to a compact form after inputting supply current sensing values and instantaneous reference current values [15].

DSTATCOM control system regulates device currents, thereby ensuring supply currents stabilize within acceptable limits of the reference currents.

The hysteresis controller delivers adequate switching where six IGBTs are switched to operate the VSI [20].

3.5. Calculation of the Total Supply Current of References

To derive reference source currents, VSC adds to the control signal, producing active and reactive components of phase currents [21].

$$\begin{aligned} i_{sr}^* &= i_{srp}^* + i_{srq}^*; & i_{sy}^* &= i_{syp}^* + i_{syq}^*; \\ i_{sb}^* &= i_{sbp}^* + i_{sbq}^* \end{aligned} \quad (22)$$

Table 1. Comparison of different synchronizing methods for D-Statcom (Numerical scale (1 = Very Low, 5 = Very High))

Method	Harmonic Immunity	Unbalance Handling	Inter - harmonics	Frequency Drift	Dynamic Speed	Complexity	Typical Tuning
SRF -PLL	2-3	1-2	1-2	3	5	1-2	PI on q -axis loop, LPF
DDSRF - PLL	3	5	1-2	3	5	3	Two SRF loops + decoupling gains
SOGI -PLL (single/dual)	5	3-4	3	5	5	3	SOGI gain k, loop PI, optional dual chains
EPLL	5	3	3	5	4	3	Adaptation gains ? (amp/freq/phase)
E ² PLL (proposed)	5	5	5	5	5	4	Extended/adaptive gains + selective decoupling

4. Test Systems and Results

Modern power systems typically provide unbalanced and nonlinear loads. Nonlinear behaviour is found in a vast majority of equipment, ranging from industrial machines to domestic appliances. This section assesses the performance of the suggested E²PLL-based control algorithm when subjected to unbalanced and nonlinear loads. Table 2 outlines the parameters used for the DSTATCOM and DFIG.

Table 1 shows a comparison of the Total Harmonic Distortions (THD) for SEIG and DFIG machines, as well as the presence or absence of an E²PLL controller, under different load conditions.

Nonlinear loads give the THD of 6.06%, and unbalanced loads give the THD of 6.80% for the SEIG generator without the E²PLL controller. When the E²PLL controller is used, the THD rises to 8.92% for nonlinear loads, but decreases to 5.81% when it comes to unbalanced loads.

In comparison to this, the DFIG generator observes a reduction in THD with the use of the E²PLL controller. If the controller is not used, the THD for nonlinear loads is 50.45%, whereas it reduces to 27.41% with the use of the controller. In the case of unbalanced loads, THD without the controller is 20.07%, and it reduces tremendously to 2.97% with the controller.

Table 2. Parameters

DFIG Specifications	
Power	4 kW
Voltage	400 V
Phase resistance of stator	0.023 p.u
Phase inductance of stator	0.18 p.u
Rotor circuit resistance	0.016 p.u
Rotor circuit inductance	0.016 p.u
Coupling inductance	2.9 p.u
Frequency	50 Hz
Magnetic pole pairs	3
Excitation capacitor bank (Y-connected)	C = 60 μF
DSTATCOM Parameters	
Interfacing inductor (Lf)	5 mH
DC rail capacitor (C _{dc})	1500 μF
Carrier frequency	10 kHz
Controller Parameters	
PLL sampling frequency	0 kHz
MAF window length (T _ω)	20 ms
Gains of the PI controller for DC bus voltage (K _p)	0.8
K _i	50
PI controller gains for PCC voltage regulation(K _p)	0.6
K _i	40
Reference DC voltage (V _{dcRef})	700 V
Reference PCC voltage (V _{tref})	400 V

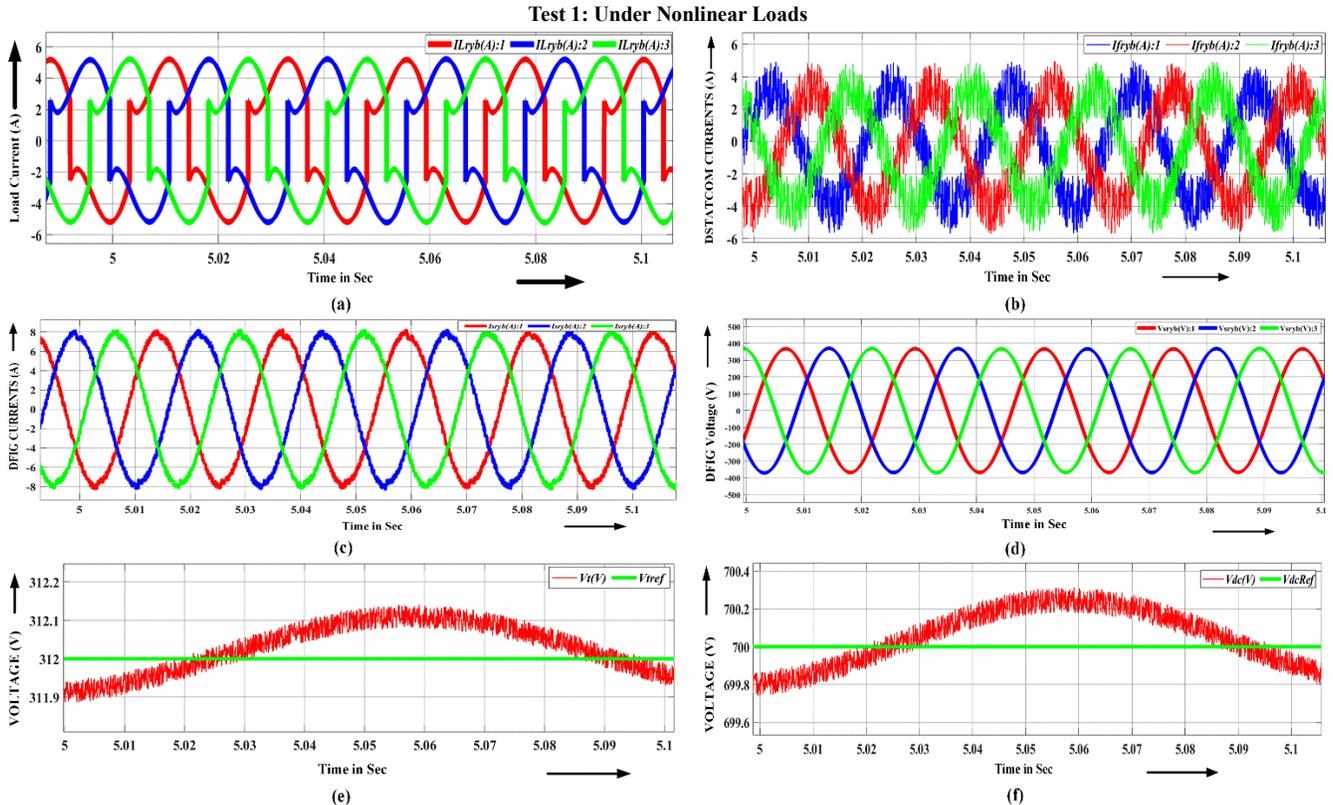


Fig. 7 E²PLL-based DSTATCOM control method performance nonlinear load: (a)Load currents, (b)DSTATCOM currents, (c)DFIG currents, (d)DFIG terminal voltages (e)Amplitude of DFIG voltages, and (f)DC bus voltage.

This analysis makes it evident how effective the E2PLL controller is in alleviating harmonic distortion, particularly in systems where the loads are unbalanced. The following two test circumstances are taken into consideration. Test Condition 1: The unbalanced loads inherently swing the harmonic currents out of line due to nonlinearity. A three-phase diode rectifier has been employed as a nonlinear load to challenge the proposed controller strategy across the terminals of the DFIG. Test Condition 2: Like nonlinear loads, imbalanced loads are commonly found in energy systems. An imbalanced load bank with 35Ω, 40Ω, and 50Ω resistive loads is connected to the PCC. The system load currents (iLryb), DSTATCOM currents (ifryb), DFIG currents (isryb), and DFIG terminal voltages (vry, vyb, vby) for nonlinear load conditions are displayed in Figures 7, respectively, using the E²PLL-based control method.

Nonlinear load disturbances in the current caused harm to the Doubly-Fed Induction Generator (DFIG) performance. The disruptive behaviours were mitigated through both D-STATCOM and E²PLL-based control systems. The D-STATCOM achieves stability by adding compensatory currents, which make the DFIG terminal and current sinusoidal and balanced (Ifryb). The E²PLL-based The control algorithm improves voltage regulation by correctly measuring reactive power consumption, followed by setting DFIG terminal voltage(vt) to its reference value(vdcref). The control approach controls the D-STATCOM dynamics to keep the DC bus voltage (vdc) stable, manage the system load currents (iLryb), D-STATCOM currents (ifryb), DFIG currents (isryb) and DFIG terminal voltages (vry, vyb, vby) for Unbalanced load conditions are displayed in Figure 8, respectively, using the E²PLL-based control method.

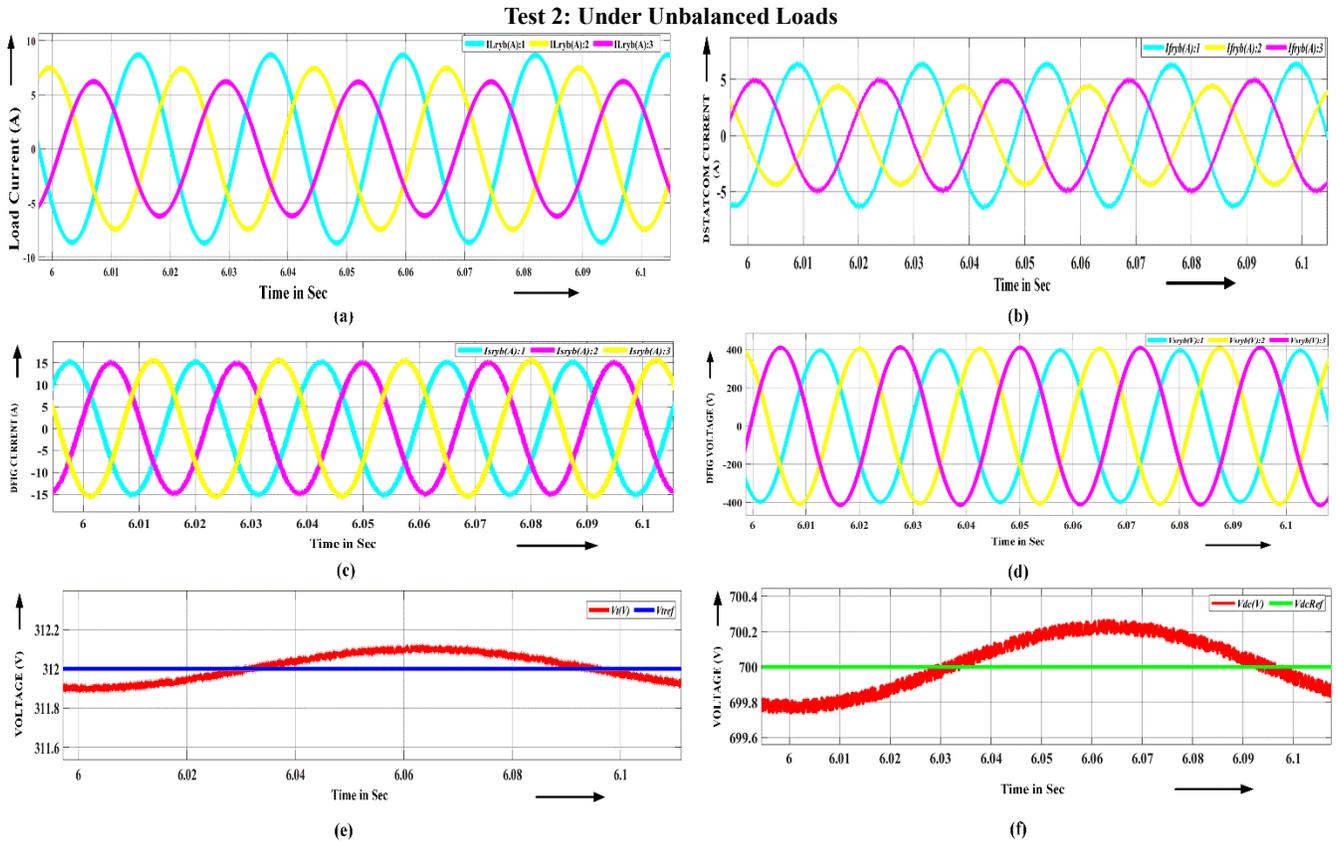


Fig. 8 E²PLL-based DSTATCOM control method performance under unbalanced load (a)Load currents, (b)DSTATCOM currents, (c)DFIG currents, (d)DFIG terminal voltages, (e)Amplitude of DFIG voltages, and (f)DC bus voltage.

Figures 8(c) and 8(d) indicate the balanced DFIG currents and voltages that result due to the compensatory currents (Figure 8(b)) injected by DSTATCOM for this purpose, even if there is minimal fluctuation in the DC bus voltage.

5. Conclusion

A new control method on the E²PLL basis is suggested in the paper that will significantly enhance the D-STATCOM

systems. The technique can be implemented for nonlinearly loaded systems and unbalanced systems, as they can relatively well calculate the phase angle of load and total load current amplitude, and the sinusoidal source currents are generated with more accuracy in calculation. Based on simulation investigations Figures 9-12, it is seen that inclusion of the E²PLL compromises the dynamic performance and stability of the D-STATCOM when subjected to low-frequency

disturbances, offering improved control over grid voltages and control over the overall system. Experimental results and Table 3 further confirm such developments with a THD reducing significantly to 50.45% and then 27.41%; unbalanced loads 20.07% and then 2.97%, respectively, evidence improved harmonic filtering and improved power quality. It is of particular significance in remote wind-diesel microgrids in regions of low system strength (like Tamil Nadu and Gujarat), where PQ issues have been acute as a result of fluctuating standalone wind generation. Post-fault, the fault voltage imbalance of more than 12 percent and harmonics

over IEEE-519 are common after a fault, initiate voltage instability, and spoil sensitive loads until blackout. This forces unnecessary application of backup diesel generator sets, resulting in high fuel cost, emissions, and joint genset wear due to frequent cycling. With low-loss D-STATCOMs and high synchronization- as with E²PLL control, PQ could be enhanced significantly, which would decrease the dependence on diesel generators, and, therefore, would increase the reliability and sustainability of wind-diesel microgrids in remote regions of India.

THD's under nonlinear and unbalanced loads

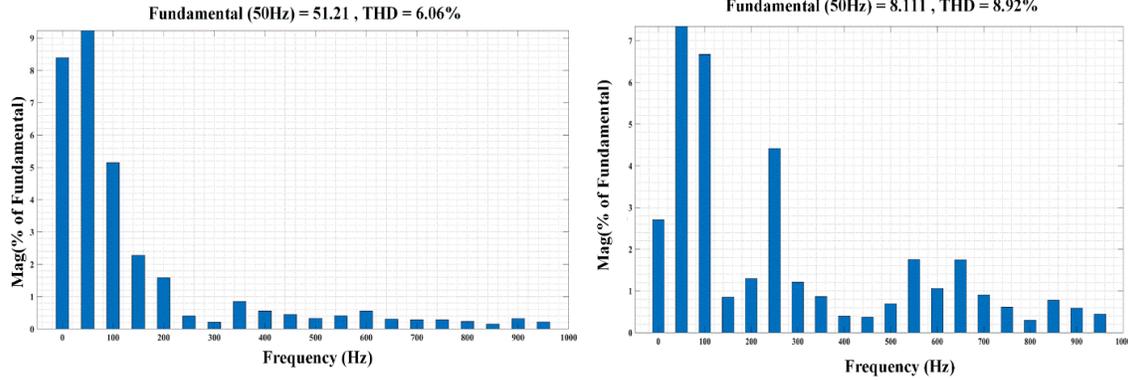


Fig. 9 THD's of SEIG- E²PLL controller in the absence as well as presence of nonlinear loads

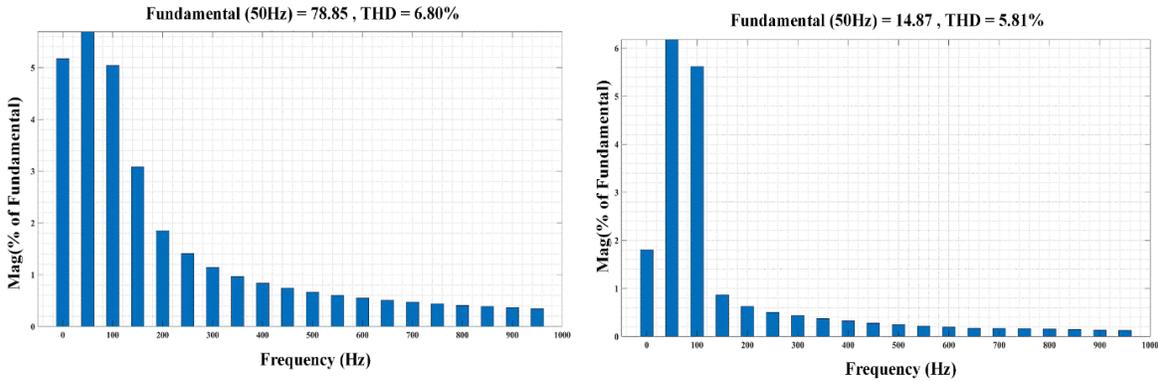


Fig. 10 SEIG output THD's with and without E²PLL controller under unbalanced loads

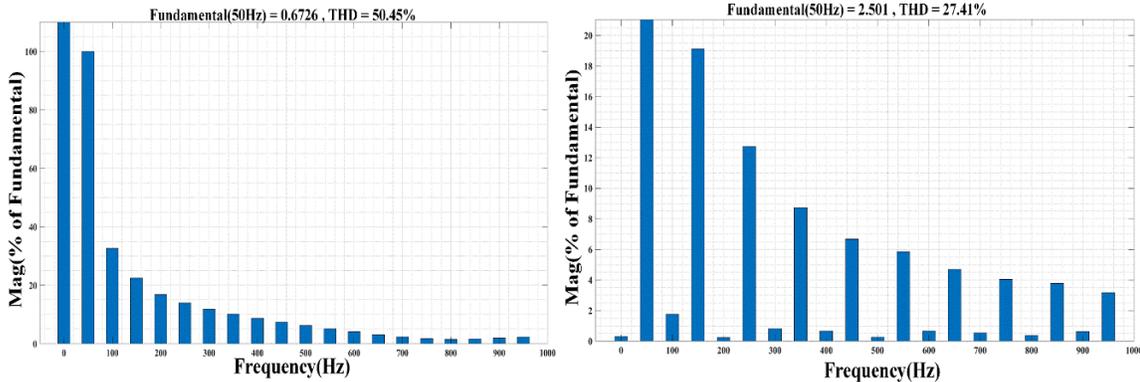


Fig. 11 THD's of DFIG with and without E²PLL controller under nonlinear loads

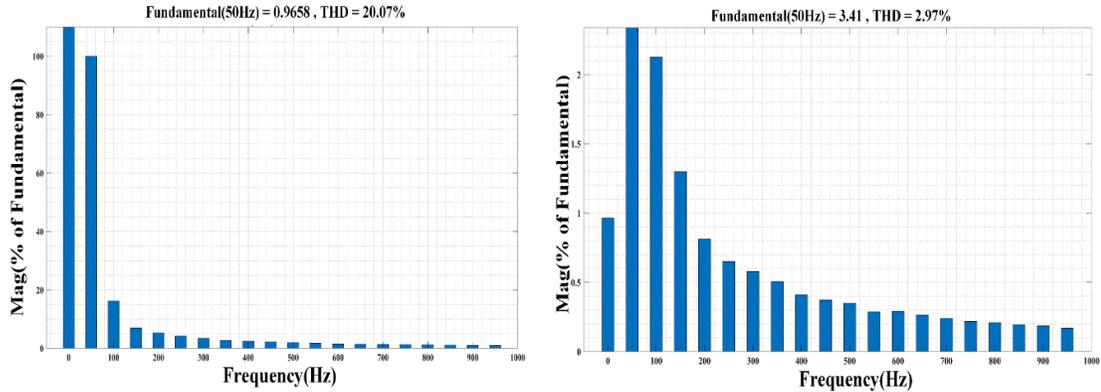


Fig. 12 THDs of DFIG with and without E²PLL controller under unbalanced loads

5.1. Glossary (Key Terms)

- DFIG: Doubly Fed Induction Generator
- D-STATCOM: Distribution Static Compensator, provides voltage support and harmonic filtering.
- PLL: Phase-Locked Loop, synchronizes signal phase/frequency with the grid.
- E²PLL: Enhanced PLL, improved disturbance rejection under distorted/unbalanced voltages.
- MEPLL: Modified E²PLL, uses adaptive filters for better harmonic suppression.
- PCC: Point of Common Coupling; connection point between wind farm and grid.
- THD: Total Harmonic Distortion
- VSC: Voltage Source Converter; converts DC to AC and injects compensation currents.
- Reactive Power Compensation: Maintains voltage and power factor by supplying/absorbing VARs.
- MAF: Moving Average Filter; extracts fundamental signals, suppresses noise.

- Positive Sequence Components: Balanced 3-phase components used for synchronization.
- IEEE-519: Standard defining harmonic limits for power systems.

5.2. Future Scope

- An experimental prototype, a hardware prototype, or a Real-Time Digital Simulation room (RTDS) is also used to verify the scalability of a new control mode.
- Optimization of PI controller in terms of algorithm intelligent optimization (e.g., PSO, GA) as applied to varying grid conditions in the process of adapting tuning to the various conditions.
- Integration of a hybrid renewable (PV, fuel cells) into a multi-source microgrid stability.
- Investigation of E²PLL behaviour at the extreme grid disturbance, such as a voltage sag/swell or a grid frequency departure.

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