SSRG International Journal of Electrical and Electronics Engineering
ISSN: 2348-8379/ https://doi.org/10.14445/23488379/IJEEE-V12I9P123

Volume 12 Issue 9, 223-235, September 2025

Original Article

Design of 1:4 Power Divider for Space Applications

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Received: 18 July 2025 Revised: 18 August 2025 Accepted: 17 September 2025 Published: 30 September 2025

Abstract *- This paper presents a novel implementation of a compact 4-way microstrip Wilkinson power divider operating in the S-band (2-4 GHz), specifically designed for space and IoT applications. The novelty of this work lies in achieving a balanced performance between bandwidth, miniaturization, and cost-effectiveness using an economical FR-4 substrate, addressing the common trade-offs found in conventional designs where one parameter is typically compromised. A comparative study was initially conducted using four 2-way dividers simulated across FR-4 and Rogers5880 substrates, each evaluated with both sharp and curved geometries. While the Rogers-sharp combination yielded the smallest footprint, the FR-4 sharp configuration was selected for fabrication due to its cost-effectiveness and competitive performance characteristics. This design approach is particularly advantageous for systems where compactness, low cost, and acceptable RF performance are essential requirements. The fabricated divider occupies a compact area of only 51 mm × 31 mm (1581 mm²) and demonstrates excellent performance metrics. The device achieves a simulated fractional bandwidth of approximately 58.4% and a measured fractional bandwidth of 66.67% at 3 GHz. Key performance parameters include return loss exceeding -13.33 dB, insertion loss around -0.6 dB, and isolation of approximately 12.18 dB without requiring additional resistors. The measured maximum phase imbalance between output ports is limited to 2.045°, supporting coherent output distribution across all channels. Compared with recent works in the literature, this design offers a significant balance of bandwidth performance, area miniaturization, and practical manufacturability. The proposed divider is specifically optimized for ISM-band and IoT-based RF front-end systems where cost-effective compact components are essential for widespread deployment and commercial viability.*

Keywords *- FR-4, Power dividers, S-band, Wilkinson power dividers, 4-way microstrip.*

1. Introduction

The Wilkinson Power Divider (WPD) is a 3-port passive device, as shown in Figure 1, that splits an input signal equally between two output ports. Key components include $\lambda_g/4$ transmission lines with Z_o impedance equal to 50 Ω for all ports and a $\sqrt{2} * Z_o$ impedance equal to 70.71 Ω for a quarter wavelength and a $2*Z_o$ isolation resistor equal to 100 Ω, utilized to provide isolation and absorb reflected power. This design ensures that all ports are matched, have low loss, and high isolation between outputs [1].

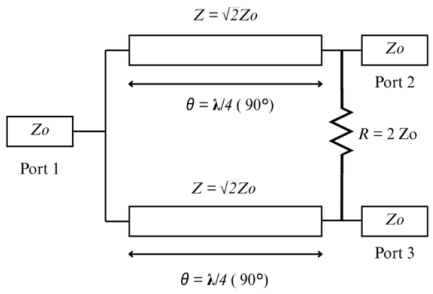


Fig. 1 Wilkinson power divider

Several gaps are identified in existing power divider designs. Most existing works utilize expensive substrates such as Rogers and Taconic materials rather than economical FR-4, limiting their cost-effectiveness for widespread deployment. Additionally, several references either lack area specifications or demonstrate larger footprints compared to compact requirements. Many existing designs exhibit performance trade-offs where achieving better bandwidth often compromises isolation performance or miniaturization goals. Furthermore, there appears to be a specific gap in S-band optimization, with few designs targeting this frequency range while maintaining balanced cost-performance metrics specifically suited for IoT and space applications where both affordability and reliable performance are crucial requirements.

The implementation is performed on the 64-bit Windows 11 operating system, and for simulation and analyses, AWR Design Environment V22.1 software is used. The achieved results are on low-cost FR-4 optimized for 2 to 4 GHz with 3 GHz as resonant frequency (fo). Measured results confirm performance: a 66.67 % FBW (2.0-4.0 GHz), return

loss ≤ -13.33 dB, insertion loss ≈ 0.6 dB, and isolation ≤ 12.18 dB (without resistor) within a compact ~51 × 31 mm² footprint. The paper outline is as follows: Section 2 discusses the related works on power dividers, and Section 3 describes the proposed design. Section 4 discusses the result analysis, followed by Section 5, which summarizes the findings and discusses their relevance for S-band applications.

2. Related Work

Satellite payloads require smaller and cost-effective microwave front-end components that maintain balanced RF performance in S-band 2 to 4 GHz telemetry and Earth observation links. Power dividers distribute signals with minimal loss, high isolation, and consistent phase balance.

Traditional high-performance substrates like Rogers offer low loss, but they come at a higher cost [2]. Substrate-Integrated-Waveguide (SIW) implementations provide a pathway for size reduction; however, they introduce fabrication complexity and limited bandwidth in corporate and Gysel topologies [3].

Wilkinson dividers on economical FR-4 substrates are attractive due to their inherent isolation, but quarter-wavelength designs tend to suffer from narrow bandwidth and large footprints when scaled beyond two ports [4]. A broad spectrum of enhancements has been pursued.

Multi-section Wilkinson designs extend bandwidth but increase layout area and insertion loss [5]. Hybrid filtering topologies using air-filled SIW cavities or resonator combinations deliver steep skirts, although they result in larger circuit size [6, 7].

3-dB microstrip dividers achieve 1-4 GHz coverage but still struggle with spurious responses and dielectric losses on FR-4 [8]. Waveguide-based four-way junctions demonstrate robust THz performance but are not suitable for low-cost planar fabrication [9], while SIW-based ultrawideband designs can reduce size by up to 80% but do not scale efficiently to four-port systems [10].

Despite the extensive research, no existing solution effectively addresses the need for four-way division, low-cost planar implementation, and rigorous S-band RF performance within a single design. Unequal-split Wilkinson topologies offer compactness but often introduce layout complexity and cascade losses [11]. Dual-band designs avoid reactive elements for simplicity; however, they face practical challenges in achieving a wide bandwidth and minimizing parasitic [12]. Hybrid design techniques show promise for halving the size and suppressing harmonics in microstrip Wilkinson power dividers, but theoretical improvements may be affected by bending losses and fabrication tolerances [13]. Single-stage wideband Wilkinson dividers covering 1-4 GHz demonstrate excellent use of isolation resistors but still face design trade-offs between bandwidth and area [14].

Similarly, linearly tapered-line dividers achieve over 160% fractional bandwidth, although complexity increases due to resistor placement requirements [15]. High-performance substrates such as Rogers offer low loss but at a higher cost [20, 21]. Substrate-integrated waveguide implementations reduce size but introduce fabrication complexity and limited bandwidth in corporate and Gysel topologies [16, 17].

Wilkinson dividers on economical FR4 substrates provide inherent isolation, but quarter-wavelength designs suffer narrow bandwidth and large footprints when scaled beyond two ports [22, 23]. Several 4-way power divider architectures have been reported.

In [16], a dual-polarization waveguide divider on an OMT-applied substrate covers 10.7 to 12.75 GHz (18% FBW) with return loss below -20 dB, insertion loss near 0.1 dB and isolation above 30 dB in a 71 × 71 mm² footprint.

A similar waveguide approach in [17] spans 17.7 to 20.2 GHz (17% FBW), achieves better than 19 dB return loss and roughly 20.6 dB isolation over a 31 × 150 mm² area (insertion loss not specified).

The suspended strip line design of [18] on Taconic RF-35 covers 7.82 to 9.86 GHz (23.1 % FBW) with return loss above 28 dB, insertion loss below 0.37 dB and isolation over 20 dB. In [19], a Wilkinson divider on RO4350B targets 8.5 to 9.5 GHz (11.1 % FBW) but exhibits only -12 dB return loss, 0.7 to 2.78 dB insertion loss and about 12 dB isolation.

Planar Rogers implementations include [20], which on 4003C spans 3.05 to 4.43 GHz (45 % FBW) with ≥ 12 dB return loss, ~0.6 dB insertion loss and ≥ 19 dB isolation in a 63 × 63 mm² layout, and [21], which uses Spoof Surface Plasmon Polaritons (SSPP) on 5880 to achieve 2 to 12 GHz (171 % FBW), < -10 dB return loss and < 0.5 dB insertion loss in 247.5 × 55 mm² (isolation not reported).

Cost-effective FR-4 designs include [22], covering 1.4 to 3.2 GHz (75 % FBW) with -23.31 dB return loss, 1.28 dB insertion loss and -54.69 dB isolation, and [23], which spans 0.54 to 1.08 GHz (67.5 % FBW) with ≥ 15 dB return loss, 0.6 dB insertion loss and ≥ 15 dB isolation in a 49 × 47.5 mm² area. Waveguide solutions [16, 17] offer high isolation but are bulky and costly. Suspended strip line and Wilkinson variants [18, 19] trade size for bandwidth or isolation. Rogers-based planar dividers [20, 21] achieve ultrawide bandwidth but incur high substrate cost. FR4 implementations [22, 23] are economical but either lack S-band coverage or do not optimally balance insertion loss, isolation, and area.

2.1. Design Calculations

2.1.1. Performance Calculation

The performance parameters for the power divider utilize standard S-parameter calculations, where return loss is determined by the ratio of reflected power to input power equation 1, isolation loss represents the power coupling between isolated ports equation 2, and insertion loss quantifies the power transmission from input to output ports equation 3. The FBW is calculated using the frequency range where performance criteria are met, equation 4, while the Voltage Standing Wave Ratio (VSWR) is derived from the reflection coefficient magnitude, Equation (5).

$$Return\ Loss(in\ dB) = -10log_{10}\left(\frac{P_{reflected}}{P_{in}}\right) \quad (1)$$

$$Isolation\ Loss(in\ dB) = -10log_{10}\left(\frac{P_{iso}}{P_{in}}\right) \quad (2)$$

$$Insertion\ Loss(in\ dB) = -10log_{10}\left(\frac{P_{out}}{P_{in}}\right) \quad (3)$$

$$FBW = \frac{f_{high}-f_{low}}{f_{center}} * 100 \quad (4)$$

$$VSWR = \frac{1+|\Gamma|}{1-|\Gamma|} * 100 \quad (5)$$

2.1.2. Microstrip Calculation

The design is optimized for S-band and 3 GHz as fo. The length (l) and width (w) for the microstrip line are calculated by the impedance (Z_0) value, impedance factor (A & B) in equation 6 and in equation 7, respectively, dielectric constant (ε_r) in equation 8, effective relative permittivity (ε_{eff}) in equation 9 and wavelength in the microstrip line (λ_g) in equation 10.

$$A = \frac{Z_0}{60}\sqrt{\frac{\varepsilon_r+1}{2}} + \frac{\varepsilon_r-1}{2\varepsilon_r}\left[0.23 + \frac{0.11}{\varepsilon_r}\right] \quad (6)$$

$$B = \frac{377\pi}{2Z_0\sqrt{\varepsilon_r}} \quad (7)$$

$$\frac{w}{h} = \frac{2}{\pi}\left[B - 1 - \ln(2B - 1) + \frac{\varepsilon_r-1}{2\varepsilon_r}\left(\ln(B - 1) + 0.39 - \frac{0.61}{\varepsilon_r}\right)\right] \quad (8)$$

$$\varepsilon_{eff} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left[\frac{1}{\sqrt{1+\frac{12h}{w}}}\right] \quad (9)$$

$$\lambda_g = \frac{\lambda_0}{\varepsilon_{eff}} \quad (10)$$

Table 1 and Table 2 present the calculated width and length dimensions for the main transmission line characteristic impedance (50 Ω) and quarter-wavelength transformer sections characteristic impedance (70.71 Ω) for both substrate configurations utilized in the simulation analysis.

Table 1. Width for microstrip design (in mm)

Substrate	Z_o = 50 Ω	Z_o = 70.71 Ω
FR-4	5.12	2.56
Rogers 5880	0.8	0.46

Table 2. Length for microstrip design (in mm)

Substrate	Zo = 70.71 Ω
FR-4	13.57
Rogers 5880	18.5

2.2. Simulation Implementation

Electromagnetic simulations are implemented on the AWR Design Environment V22.1 software, executed on a 12th Gen Intel Core i5-12500 processor, 16 GB RAM, and a 64-bit Windows 11 Home Single Language operating system. The design is optimized for S-band (2-4 GHz) with a frequency of 3 GHz. In total, 4 distinct configurations were simulated to understand the effects of substrate (FR-4 and Rogers 5880) and geometry (sharp and curved) of the circuit.

2.2.1. 2-Way Configuration

The two branch lines are implemented as straight quarter-wavelength microstrip segments connected by a narrow feeding line. In the circuit schematic, the isolation resistor is placed between the two branch junctions. The sharp layout uses right-angle T-junctions and 90° bends, minimizing the footprint but introducing higher current accumulation at corners as shown in Figure 2.

To mitigate discontinuity effects, the same electrical lengths and widths are routed with smooth arcs: quarter-wave bends are realized via curved elements. The T-junction remains identical, but all bends are curved, reducing reactive parasitics at corners at the expense of a slightly larger footprint, as shown in Figure 3.

Here, the layout mirrors Figure 2 but uses Rogers 5880 stack-up, scaling the microstrip widths while preserving quarter-wave lengths. The sharp-corner routing allows us to isolate substrate losses from bend discontinuities in simulation, as shown in Figure 4. Identical to Figure 4 except all 90° and 60° bends are implemented as radius arcs, matching the curved-corner strategy of Figure 3.

This configuration exhibits the lowest reactive mismatch at corners and the lowest dielectric loss, providing a benchmark for the best-case EM performance as shown in Figure 5. EM structures show visibly distinct microstrip polygon footprints, as shown in Figure 6, that are between curved and sharp geometries.

Curved designs offer smoother field distribution, reducing edge effects and improving isolation, making them superior for high-frequency applications. Sharp geometries concentrate fields at bends, increasing losses but providing design simplicity. For Rogers 5880, low dielectric loss

outperforms FR-4 across both geometries. FR-4 exhibits higher losses and thermal expansion but remains viable for cost-sensitive, low-frequency applications where Rogers 5880 precision is not critical.

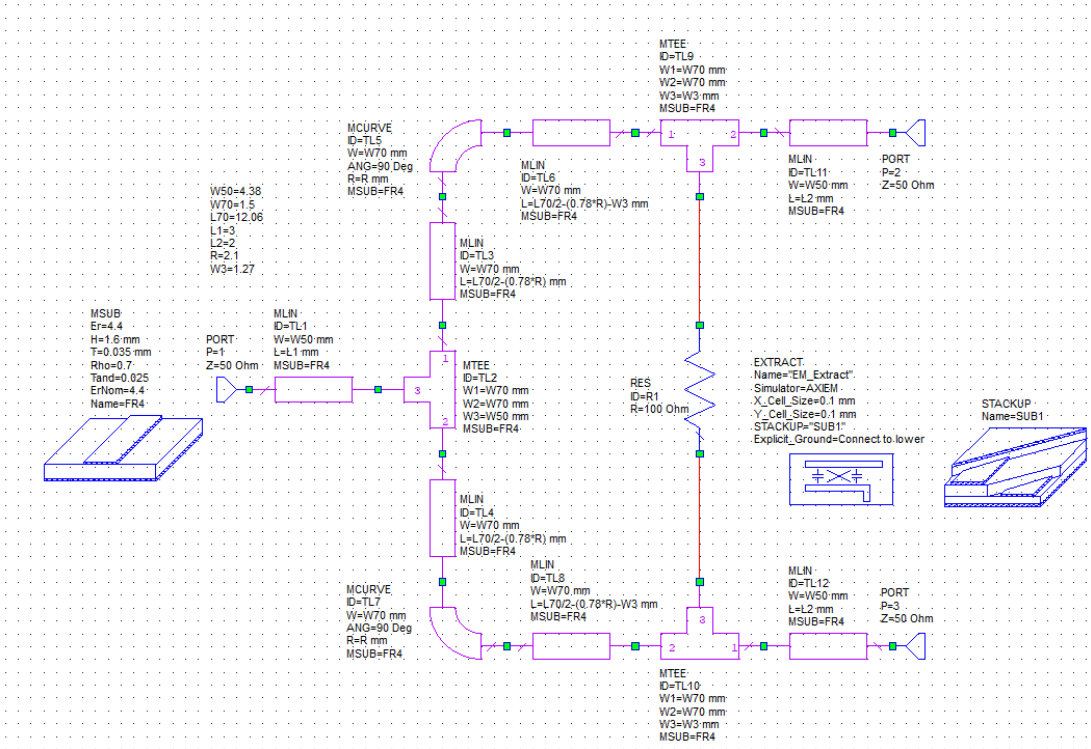


Fig. 2 Circuit schematic for 2-way power divider using FR-4(sharp geometry)

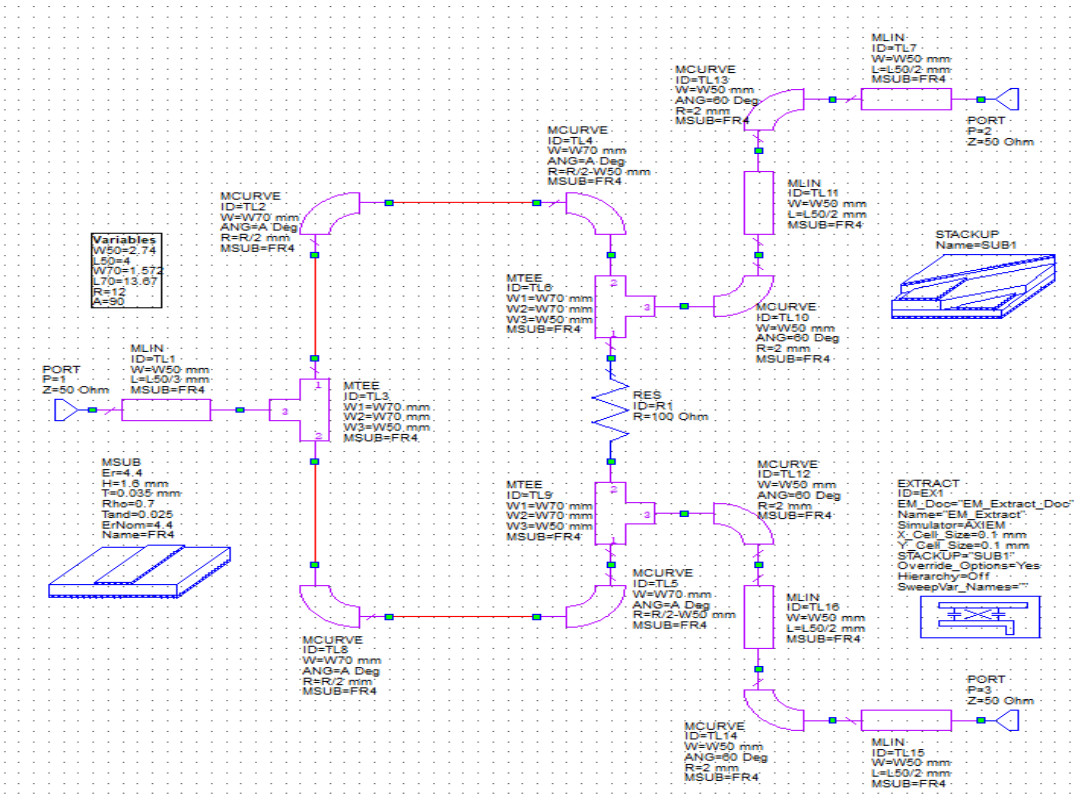


Fig. 3 Circuit schematic for 2-way power divider using FR-4(curved geometry)

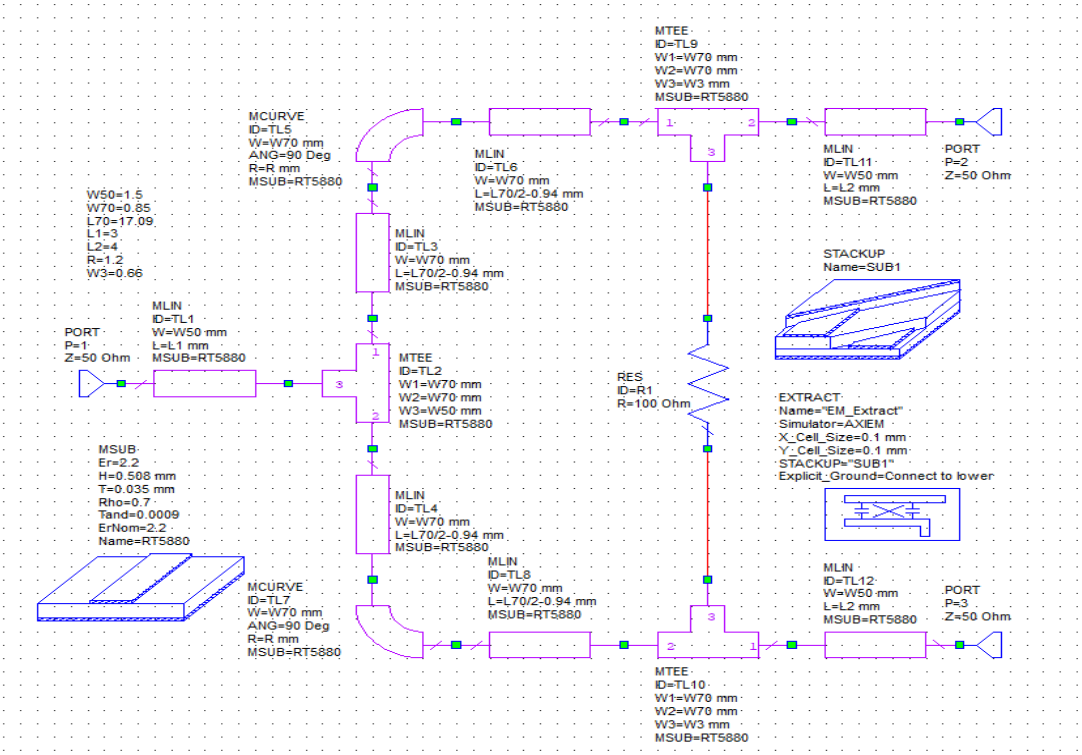


Fig. 4 Circuit schematic for 2-way power divider using rogers 5880(sharp geometry)

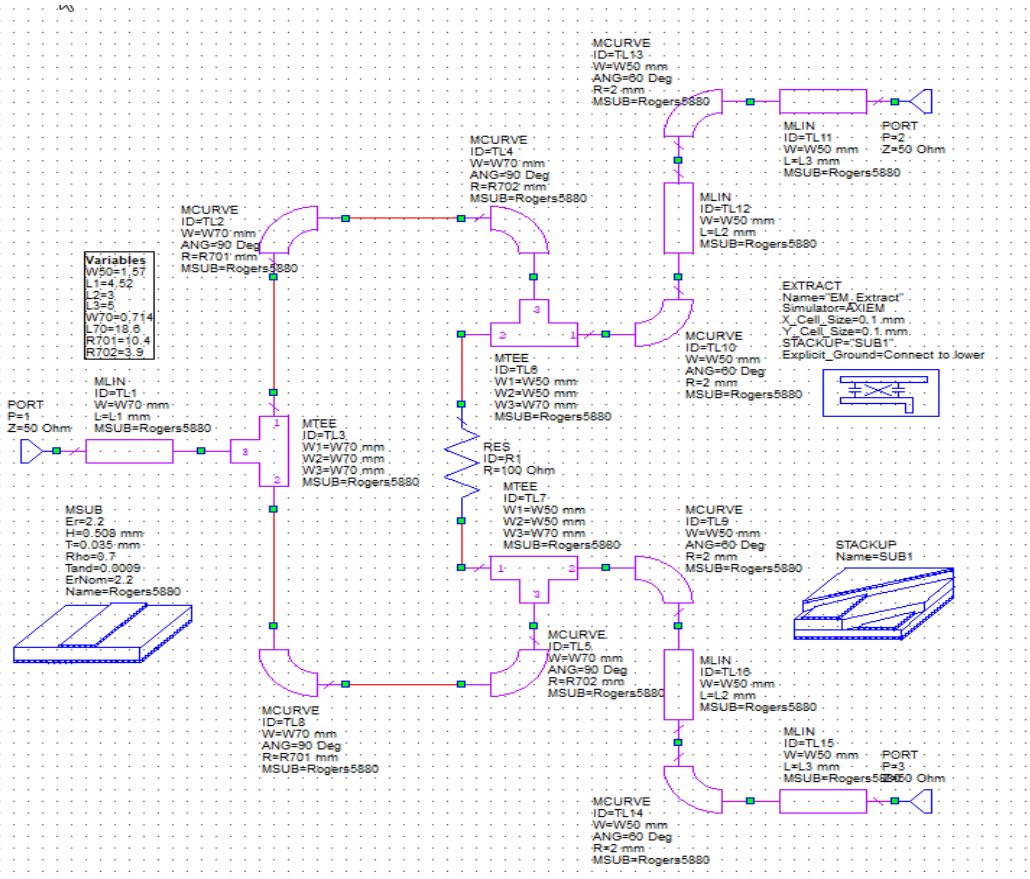


Fig. 5 Circuit schematic for 2-way power divider using rogers 5880(curved geometry).

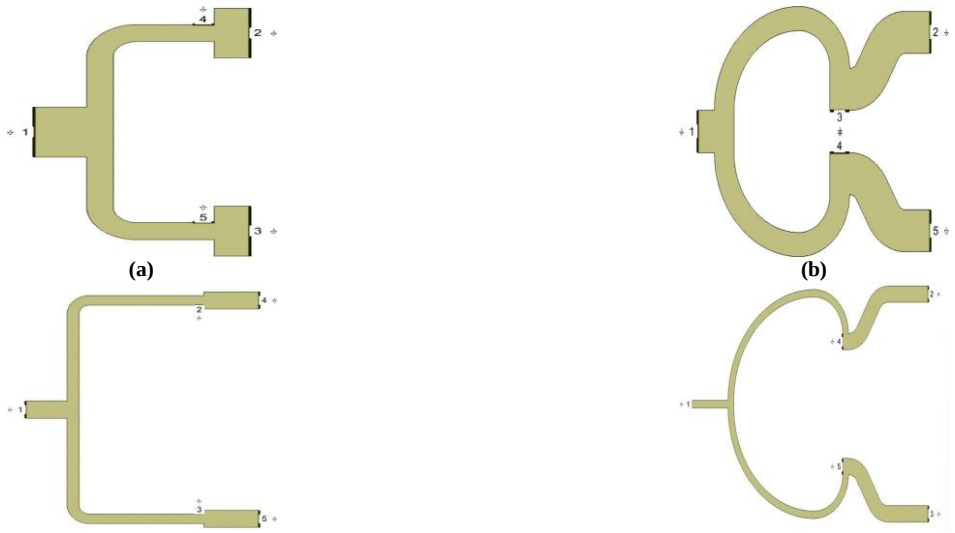


Fig. 6 EM structures for 2-way power divider configurations. (a) FR-4 sharp, (b) FR-4 curved, (c) rogers 5880 curved, and (d) rogers 5880 sharp.

2.2.2. 4-Way Configuration

After analyzing the results and understanding the trade-offs for the final design, the FR-4 substrate with sharp geometry was selected as the subcircuit (S1, S2, and S3). The substrate dielectric constant (εr = 4.4), thickness (H = 1.6 mm), and loss tangent (tanδ = 0.025). Microstrip traces MTRACE2 with adjustable width W and length L are laid out on this substrate and connected through subcircuits S1, S2, and S3 (each representing the circuit schematic of FR-4 with sharp geometry) to four 50 Ω ports P1 through P4 for power division and isolation. Right-angle bends of 90° and a 13 mm back drill-through minimize parasitic effects. Because FR-4 exhibits higher dielectric loss versus Rogers 5880, wider traces and careful impedance matching are required to reduce insertion loss. The isolation resistor and symmetric port placement ensure balanced splitting.

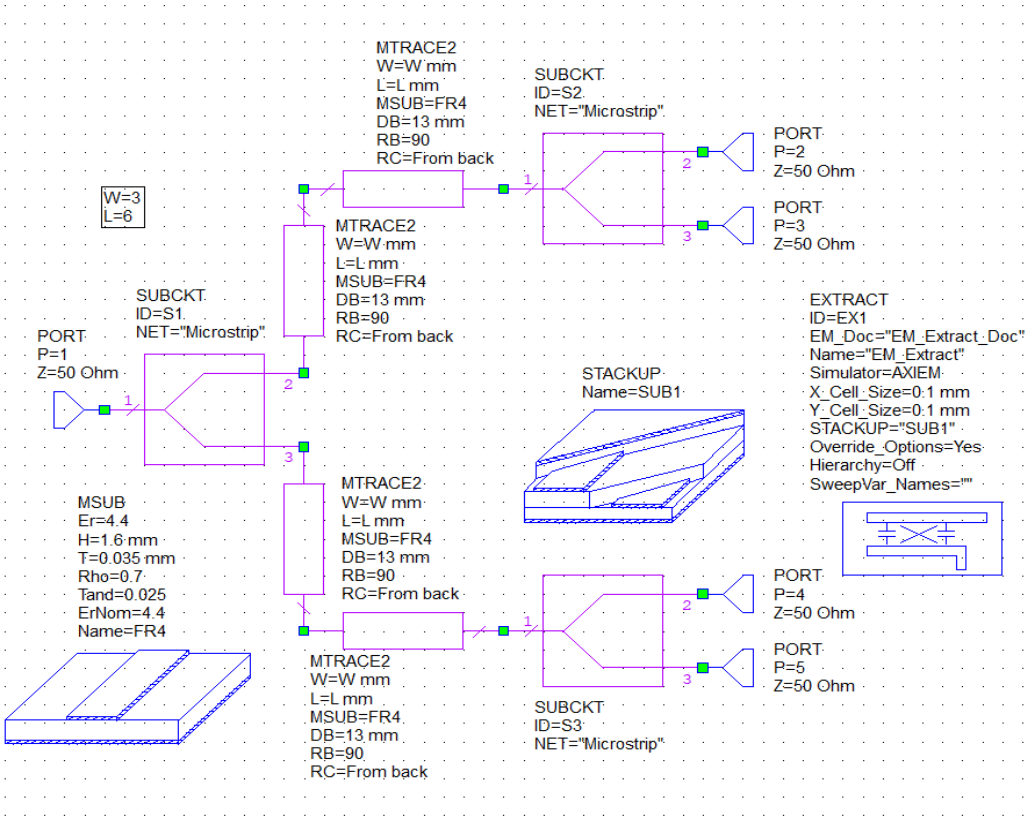
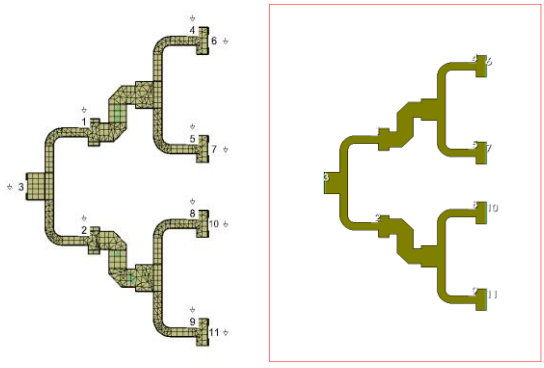


Fig. 7 Circuit schematic for 4-way power divider using FR-4

The EM structure uses a mesh grid (0.1 mm * 0.1 mm) with the AXIEM solver to model field interactions in the FR-4 lossy substrate. The 3D stack-up shows the FR-4 dielectric layer of 1.6 mm thickness and an air layer above the microstrip traces to capture radiation and fringing fields. The mesh density captures field gradients at bends and vias for analysis of parasitic capacitance and resonance effects. The substrate's high loss tangent increases energy dissipation, so validation is needed to optimize trace geometry and reduce losses. The lateral view of the 3D structure highlights layer arrangement and layout structure, which makes it easier to understand the configuration.



(a) **(b)**

Fig. 8 Layouts for 4-way configuration. (a) Mesh layout (0.1 mm*0.1 mm grid dimensions), and (b) Lateral view of 3D structure.

2.3. Materials and Fabrication

2.3.1. Components Required

Table 3 summarizes the substrate specifications used for simulations, which are dielectric constant (εr), loss tangent (tanδ), and height (H). These properties affect how the substrate handles signal propagation and losses, especially at higher frequencies.

Rogers 5880, with its lower dielectric constant and loss tangent, is generally better suited for high-frequency applications. And Table 4 summarizes the copper conductor specifications used, and its performance is described by parameters like conductivity (σ), thickness (T), and surface roughness (ρ). These factors influence the efficiency of the signal transmission, and the amount of loss occurs due to imperfections.

Table 3. Substrate specifications

Substrate	FR-4	Rogers 5880
ε_r	4.4	2.2
tanδ	0.025	0.0009
H	1.6 mm	0.508 mm

Table 4. Conductor specifications

Conductor	Copper
$\boldsymbol{\sigma}$	$5.86 * 10^7$ S/m
T	0.035 mm
ρ	0.7

2.3.2. Design Fabrication

The 4-way WPD, as shown in Figure 9, is etched on an FR4 substrate with five SMA connectors soldered in place. The FR4 board carries the copper trace network that splits power from the single input connector at the bottom into 4 equal output paths at the top. Soldered right-angle bends and via structures are visible where necessary to maintain impedance and reduce parasitic effects. The divider is connected to a vector network analyzer by attaching coaxial cables to each SMA port.

After multi-port calibration, the VNA measures return loss at the input port and insertion loss and isolation between the input and each output port across the S-band frequency range. These measurements verify the fabricated design against simulation results and quantify losses introduced by the FR4 substrate and assembly process.

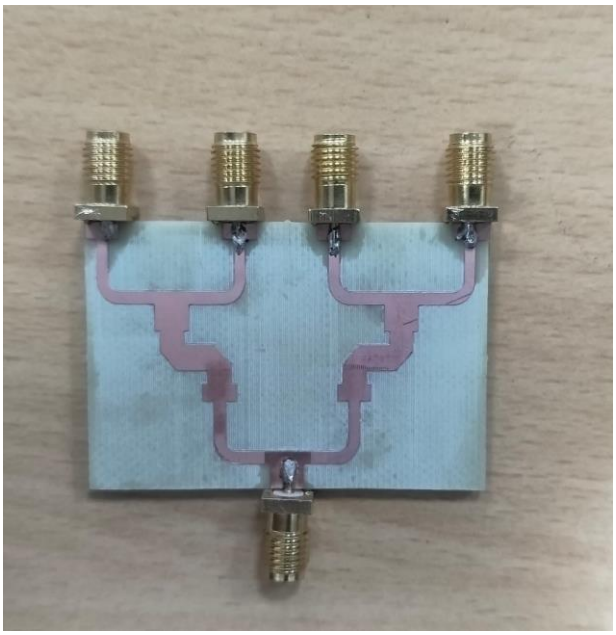


Fig. 9 Fabricated 4way power divider using FR-4

3. Results and Discussion

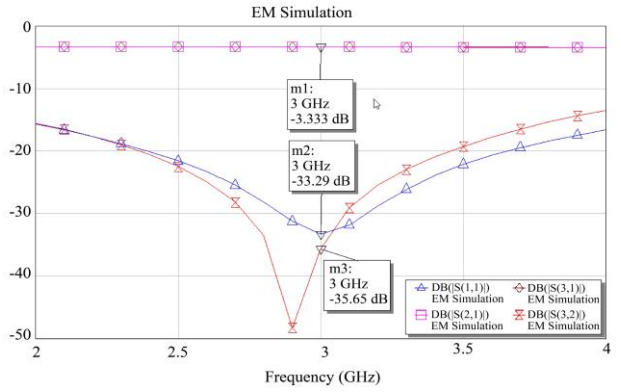
The proposed design presents a novel 4-way WPD fabricated on FR-4 substrate for S-band applications. The design was comprehensively analyzed for return loss, insertion loss, isolation loss, fractional bandwidth, and footprint characteristics. Implementation utilized a system featuring a 12th Gen Intel Core i5-12500 processor, 16GB RAM, and 64-bit Windows 11 Home Single Language, with electromagnetic simulations conducted using AWR Design Environment V22.1 software.

The following sections present detailed simulation results, beginning with a brief 2-way analysis followed by a comprehensive 4-way performance evaluation, concluding with measured fabrication results that validate the corresponding simulation predictions as shown in Table 6.

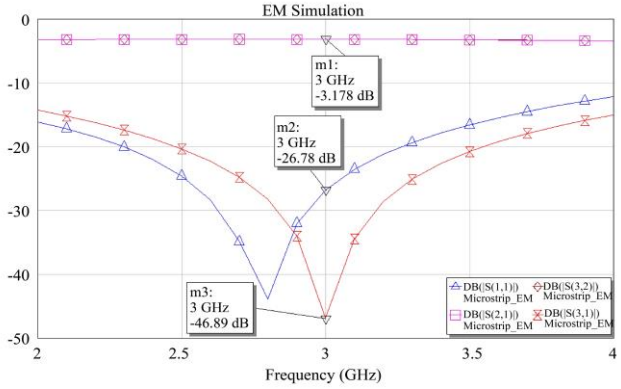
3.1. Simulation

3.1.1. 2-Way Configuration

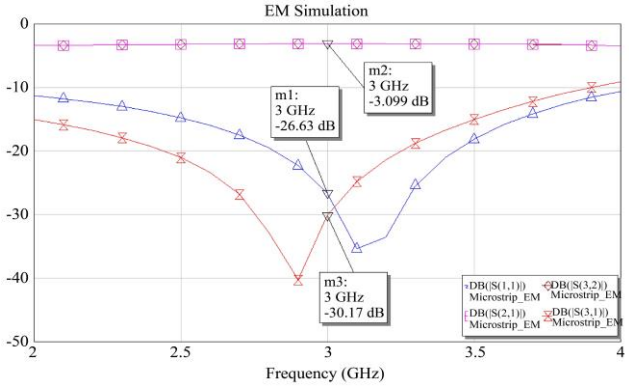
In the 2-way EM simulations, all the layouts meet the insertion-loss target at the design frequency, while isolation and return-loss bandwidth vary. FR-4 curved delivers the best isolation and moderate fractional bandwidth, FR-4 sharp yields good isolation and narrower bandwidth, Rogers 5880 curved offers the widest fractional bandwidth at lower isolation, and Rogers 5880 sharp balances moderate bandwidth with good isolation. The FR-4 sharp geometry was ultimately chosen for the 4-way divider owing to its minimal footprint, near-ideal insertion loss, and adequate isolation, as shown in Figure 10.



(a)



(b)



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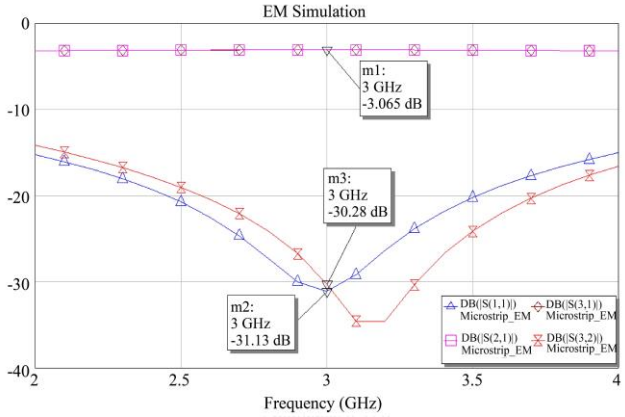

(d)

Fig. 10 EM structures for 2-way configurations. (a) FR-4 sharp, (b) FR-4 curved, (c)rogers 5880 curved, and (d) rogers 5880 sharp.

The footprint comparison in Table 5. shows that the sharp-corner layouts are significantly more compact than their curved counterparts on both substrates; Rogers 5880 sharp is the smallest at 47.96 mm², followed by FR-4-sharp at 73.48 mm², whereas the curved versions occupy 76.31 mm² (Rogers 5880) and 107.10 mm² (FR-4). Thus, while Rogers 5880 offers the tiniest overall area, the FR-4 sharp geometry still provides a substantial reduction in size over the curved designs at a much lower material cost.

Table 5. Polygon area for the configurations

Substrate	Geometry	Area ($in\ mm^2$)
FR4	Sharp	73.48
	Curved	107.10
Rogers5880	Sharp	47.96
	Curved	76.31

3.1.2. 4-Way Configuration

The simulated return loss ($S_{11,}$ $S_{22,}$ $S_{33,}$ $S_{44,}$ S_{55}) as shown in Figure 11 for all 4 output ports and the input port, with values exceeding 16.96 dB at 3 GHz and remaining above -13 dB across the full 2-4 GHz band, indicating excellent matching as shown in Figure 11. Correspondingly, the insertion loss ($S_{21,}$ $S_{31,}$ $S_{41,}$ S_{51}) as shown in Figure 12 is approximately -6.5 dB at 3 GHz, very close to the ideal -6 dB, and stays below -7 dB throughout the S-band, demonstrating minimal power loss in each branch. Isolation ($S_{32,}$ $S_{43,}$ $S_{42,}$ $S_{52,}$ $S_{53,}$ S_{54}) performance with the 100 Ω resistor as shown in Figure 13, peaks at better than -45 dB between output arms at 3 GHz and up to -51 dB on some paths and remains above 20 dB for all pairs, ensuring strong port-to-port decoupling.

Without the resistor as shown in Figure 14, isolation is still around -14.8 dB for adjacent outputs and up to -29 dB for non-adjacent ports at 3 GHz, confirming inherent isolation from the Wilkinson topology. The phase response, as shown in Figure 15, is nearly linear; output phase angles at 3 GHz range from 69.7° to 71.7°, yielding a maximum phase

imbalance of only 2.045°, which supports coherent distribution. Finally, the VSWR plot as shown in Figure 16 stays below 1.35 over the entire band for all ports, verifying good impedance matching and a robust design.

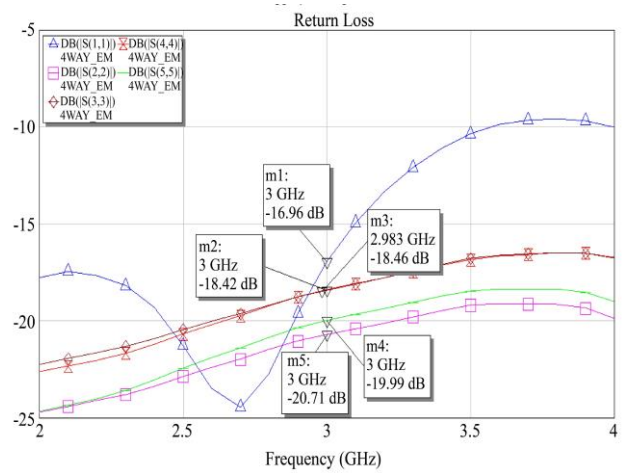

Fig. 11 Simulated return loss plot

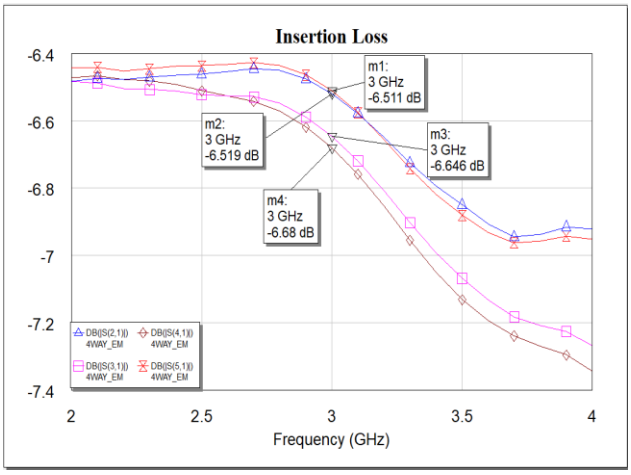

Fig. 12 Simulated insertion loss plot

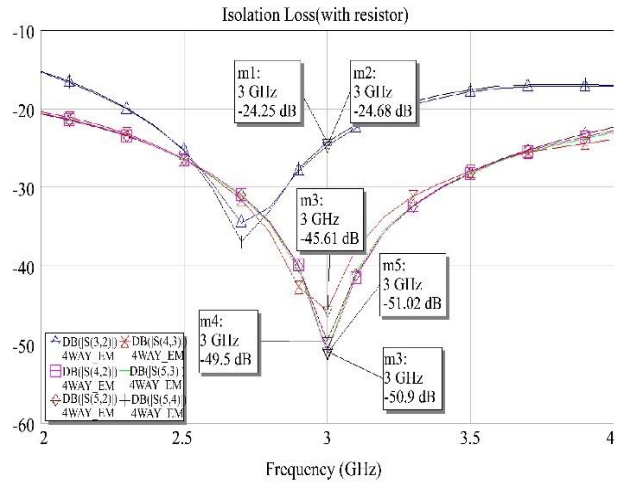

Fig. 13 Simulated isolation loss (with isolation resistor) plot

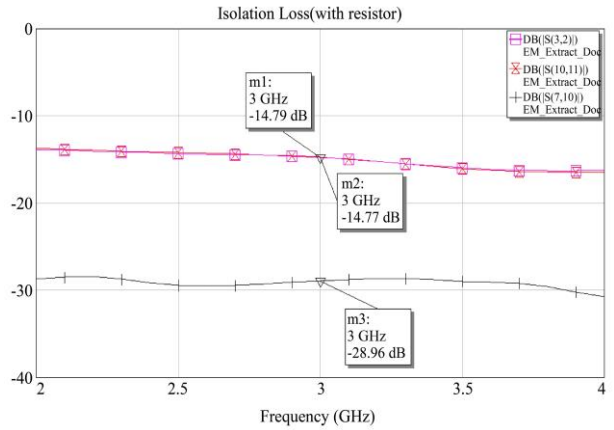

Fig. 14 Simulated isolation loss (without isolation resistor) plot

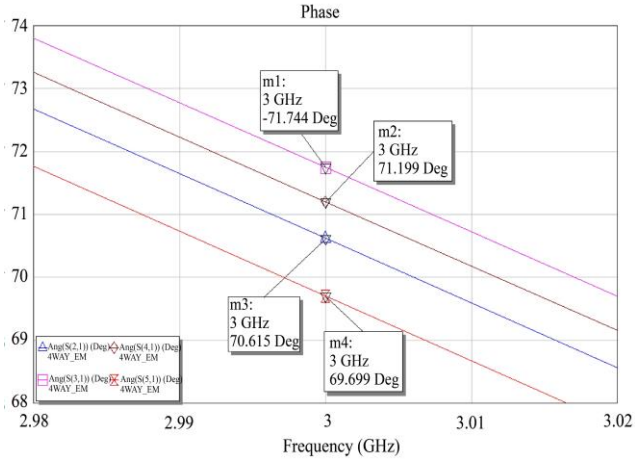

Fig. 15 Simulated phase plot

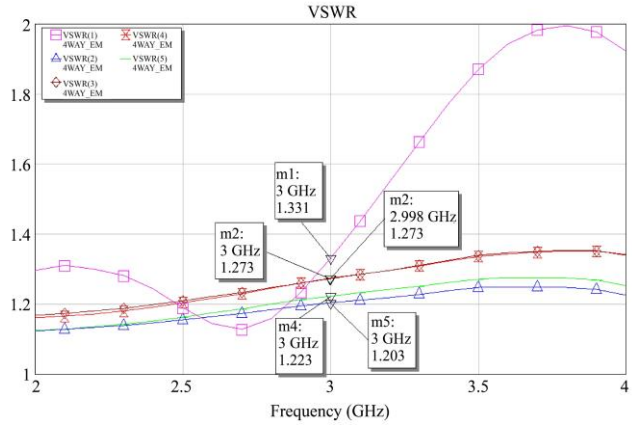

Fig. 16 Simulated VSWR plot

3.2. Measured Results

The fabricated 4-way WPD demonstrates a balanced performance across S-band frequencies, validating the design objectives of miniaturization and cost-effectiveness. Return Loss (S_{11}) exceeds the target threshold at the design frequency, aligning closely with simulations and confirming excellent input port matching. Across the operational band, return loss

remains below acceptable limits, supporting the measured fractional bandwidth, which is slightly wider than the simulated FBW. This minor enhancement is attributed to fabrication tolerances in the FR-4 substrate, as shown in Figure 17. Insertion Loss (S_{41}) averages near the ideal value for a 4-way divider. The observed loss includes conductor and dielectric losses from the FR-4 substrate. Notably, all output ports exhibit amplitude imbalances below acceptable limits within the S-band, ensuring uniform power distribution. Phase imbalance between outputs is confined to acceptable levels, critical for coherent signal combining in phased-array systems, as shown in Figure 18.

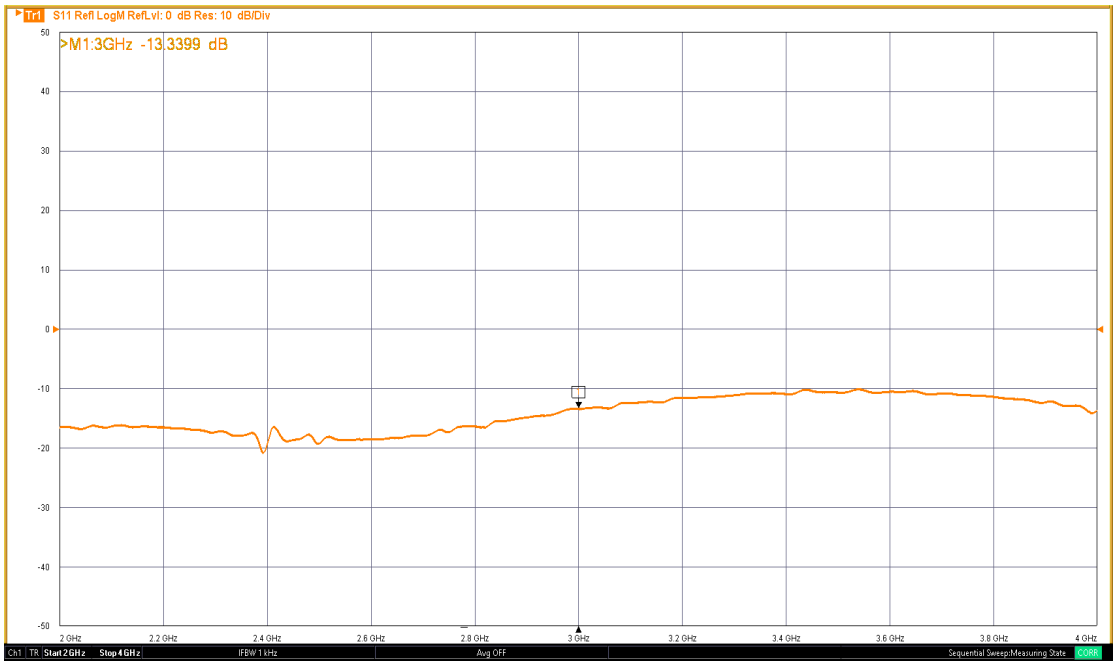

Fig. 17 Measured return loss plot

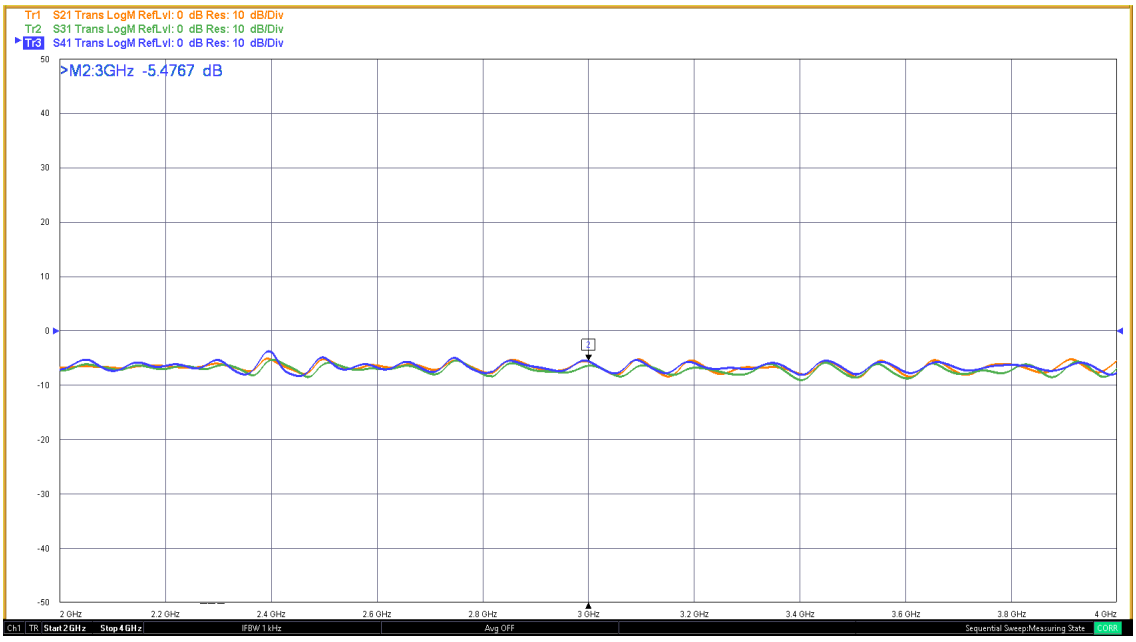

Fig. 18 Measured insertion loss plot

Isolation (S_{43}, S_{42}) between output ports reaches acceptable levels at the design frequency without isolation resistors, consistent with resistor-free simulations. While the absence of resistors slightly reduces isolation compared to resistor-equipped designs, this simplification aids miniaturization and avoids parasitic effects. The measured

isolation remains acceptable for cost-driven applications, with marginal deviation from simulations across the band, likely due to connector losses and substrate inhomogeneity, as shown in Figure 19.

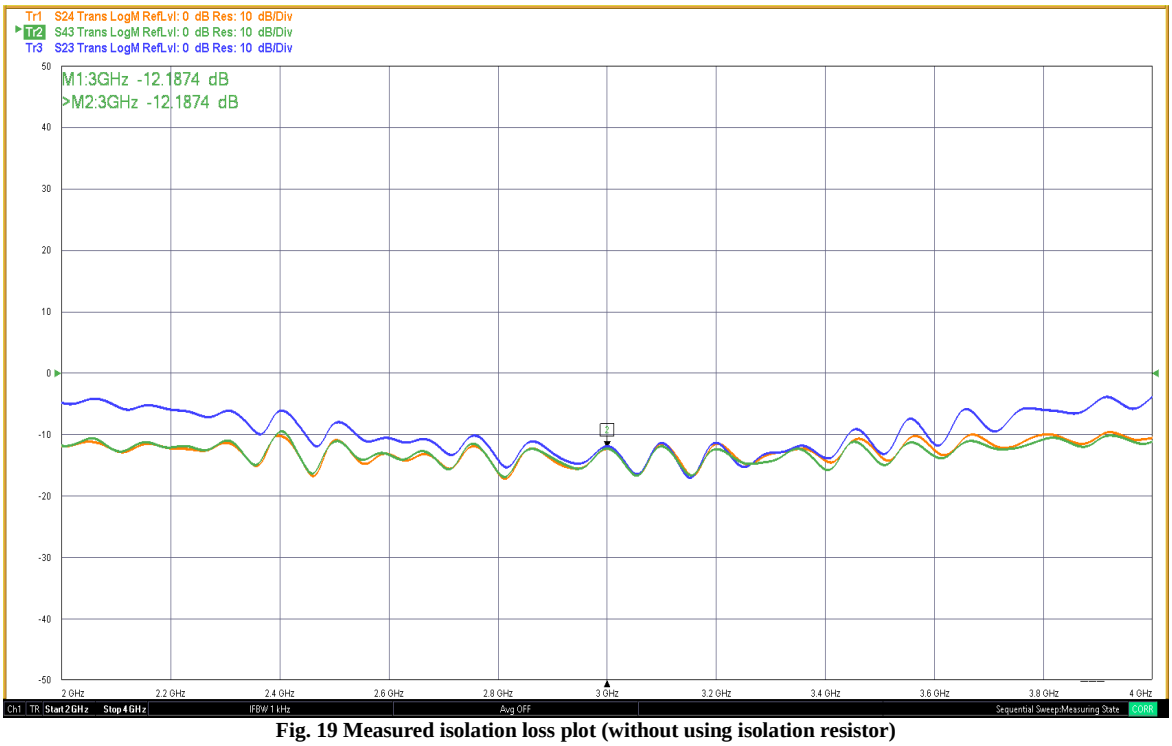

Fig. 19 Measured isolation loss plot (without using isolation resistor)

Table 6 provides a comprehensive overview of the proposed design compared to existing literature, evaluating frequency band, fractional bandwidth, substrate material, return loss, insertion loss, isolation performance, and physical footprint. The simulation and measurement data confirm the effectiveness of S-band utilizing economical FR-4 substrate material.

This work introduces a compact 4-way WPD optimized for the S-band using an economical FR-4 substrate, demonstrating an effective balance between cost, size, and RF performance. Through comparative simulation and measurement, the design achieves a measured fractional bandwidth of 66.67%, return loss of –13.33 dB, insertion loss of ~0.6 dB, and isolation of 12.18 dB without a resistor, all within a compact 51 × 31 mm² footprint. These results validate the design's novelty and competitiveness, especially when compared to both high-end Rogers-based dividers and other FR-4 solutions. The use of sharp-cornered geometry on FR-4 enables significant area reduction (up to 60%), while maintaining acceptable phase and amplitude balance for coherent applications. As supported by a detailed comparison (Table 6), this work successfully bridges the performance gap between expensive, high-end designs and low-cost solutions, making it ideal for UAVs, portable ground terminals, IoT front-ends, and small satellite systems where cost, size, and simplicity are paramount.

Table 6. Comparative analysis of referred work

Reference	Frequency band (in GHz)	FBW	Substrate	Return Loss (in dB)	Insertion Loss (in dB)	Isolation (in dB)	Area ($in\ mm^2$)
[16]	10.7 - 12.75	~ 18%	N.A. (OMT applied)	< -20	~ 0.1	> 30	71 * 71
[17]	17.7 - 20.2	~ 17%	N.A. (OMT applied)	≥19	Not explicitly mentioned per branch	~ -20.6	~ 31* 150
[18]	7.82-9.86	~ 23.1%	Taconic RF-35	> 28	<0.37	> 20	Not specified
[19]	8.5 - 9.5	~ 11.1%	RO4350B	≤ -12	~ (0.7 - 2.78)	~ -12	Not specified

[20]	3.05 - 4.43	~ 45%	Rogers 4003C	≥ 12	~ +0.6	≥ 19	~ 63*63
[21]	2 - 12	~ 171%	Rogers 5880	< -10	< 0.5	Not specified	247.5 * 55
[22]	1.4 - 3.2 *(f_o = 2.87)*	~ 75%	FR-4	-23.31	~ +1.28	-54.69	Not specified
[23]	0.54 - 1.08	~ 67.5%	FR-4	≥ 15	0.6	≥ 15 dB	~ 49*47.5
Proposed Design (Simulation)	2 – 4 *(f_o = 3)*	~ 58.4%	FR-4	≤-16.96	~ +0.6	≤ 24 (with resistor) ≤ 14.1(w/o resistor)	~ 283.4 (Polygon Area)
Proposed Design (Measured)	2 – 4 *(f_o = 3)*	~66.67%	FR-4	≤-13.33	~ -0.6	≤12.18 (w/o resistor)	~51*31

(OMT: Ortho-Mode Transducer)

4. Conclusion

The proposed design achieves a 66.7% fractional bandwidth with significant performance enhancements: 53% lower insertion loss (0.6 dB) than prior FR4-based approaches, 11% better return loss (13.3 dB) versus comparable S-band designs, and sufficient isolation without a resistor (12.2 dB) that is expected to increase significantly after using an isolation resistor. Footprint reduction reaches 60% (1,581 mm²) against key comparators, while FR-4 substrate enables 75% cost savings over speciality materials. This methodology enables optimization of the divider design specifically for cost-sensitive and space-constrained S-band applications that require balanced RF performance characteristics. The approach addresses the needs of diverse systems, including unmanned aerial vehicle communications, portable ground terminal equipment, IoT base station infrastructure, and compact satellite transceiver modules, where both economic viability and reliable performance parameters are essential design considerations.

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