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Original Article

Implementation of Solar Photovoltaic System using Cascaded H-Bridge Multilevel Inverter with Reduced Switch Count

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Abstract - *An Excessive number of power sources present in standard architectures can be reduced in the present thirteen-level multilevel inverter with a single-phase photovoltaic system. Existing inverter designs are complicated logic control, bigger in size, and have more losses due to high-frequency switching. To overcome these drawbacks, the new proposed design houses a single full-bridge stage and only five bidirectional switches, controls the circuit, minimizing component cost, and improves overall efficiency. In cascaded H-Bridge arrangements, several full bridges are incorporated, whereas in the proposed circuit, only thirteen discrete voltage levels from +Vdc to –Vdc in little increments are obtained by combining outputs from the full bridge and the bidirectional devices. These arrangements give a waveform that is almost sinusoidal, thereby minimizing Total Harmonic Distortion (THD), enhancing power quality, and removing the burden on filtering. Simulation validations conducted in MATLAB/SIMULINK and PROTEUS compare output waveforms, switching losses, and harmonic spectra. The results provided that the prototype gives clean, grid-compatible AC power with low THD and lower switching losses, proving that it is a promising prototype for efficient, grid-tied solar installations.*

Keywords - *Photo Voltaic System, Modified Cascaded H–Bridge Inverter, Bidirectional Switches, Fuzzy System, THD.*

1. Introduction

Nowadays, solar photovoltaic production has increased, and its significance has become a conventional energy source application because of distinctive merits such as straightforward allocation, high reliability, high flexibility, low fuel cost, fewer maintenance, silent, and no wear & tear due to the nonexistence of moving parts [1]. Additionally, the solar energy characteristics are a clean, greenhouse gas-free source of non-exhaustible energy supplies. Along with various types of renewable energy sources, solar and wind plants are extremely well-liked due to highly developed power electronic equipments and techniques [2, 3]. The photovoltaic sources are used in numerous applications, for instance, low-power and medium applications [4]. The PV with an inverter is used to convert DC power obtained from PV panels into AC power to be fed into the load [5]. Conventional inverters have used different methods in the past years, such as diode clamped, flying capacitor, and cascaded inverter [6]. In conventional inverters, the cost is higher due to the increased number of capacitors in flying capacitors, the requirement for more clamping diodes as the number of levels increases in diode-clamped inverters, and the need for more DC sources in cascaded inverters [7]. Multilevel voltage source inverters to attain high voltages with little harmonics and without transformers [8]. The objective of a multilevel inverter is to produce a virtually sinusoidal output voltage and output current, resulting in less stressing of power electronic components due to decreased power switching losses, which are less than those of the conventional inverter [9]. The design of the proposed system is a small ratings of filter, lower electromagnetic interference, less cost, high flexibility, and light load than the conventional inverter [10]. In the new cascaded H-bridge inverter design, adding extra modules not only boosts the output voltage levels but also cuts down on unwanted harmonics seen in the waveform [11, 12]. To make the circuit work properly, however, each stage still needs bidirectional switches so that current can flow in both directions at that node [13]. That being said, in the end, the total configuration uses fewer components than many older multilevel topologies, offers a cleaner harmonic spectrum, handles high input voltages typical of heavy-duty systems, and keeps the switching frequency low for each device [14, 15].

Current Multilevel Inverters (MLIs) are more complex, hardly scalable, and less effective, especially under variable load conditions. To overcome these limitations, vigorous design and experimentation are required in order to develop MLI in a simple topology, considering minimizing components, providing good power quality, scalability, and improved performance by using a single or a smaller number of DC sources.

In this paper, we propose an improved CHBI possessing lower harmonics, fewer components, and superior performance. Inverter topology used in this paper for PV applications, that is, diode clamped, two-level, flying capacitor, and CHB inverters, was thoroughly iterated, highlighting its strengths and drawbacks.

A thorough study of the literature review provides the need for MLI design, which lowers switching losses, component requirements, and improves output quality. A review of capacitor voltage balancing, bi-directional switching, and harmonic reduction techniques explains the need for advanced MLI. MLI, as a diode-clamped, flying capacitor, and CHB topologies are studied in depth in line with Renewable energy applications, which produce high-quality AC output with less harmonic distortion, but have certain limitations. Diode-clamped inverters need a larger number of clamping diodes due to voltage level increases, whereas flying capacitor inverters are prone to complex capacitor voltage balancing and a higher component count. Regular CHBI needs multiple isolated DC sources, leading to increased system cost and complexity, particularly in SPV applications, where compactness and effectiveness are essential. Existing topology limitations also highlight the need for MLI design, i.e., 13 level inverter, which allows for a lesser switching count, lower THD, easy management, and better responsiveness, more suitable for grid-tied PV systems. The current limitation is the dependence on asymmetrical DC sources, which is complicated. In addition to that, high voltage stress across certain switches in step-up topology requires components of high voltage ratings, leading to more cost and more switching losses.

2. Proposed Topology

Traditional voltage-source inverters suffer from switching losses, which damage power quality overall and place total harmonic distortion well above acceptable limits [16]. As a natural candidate, the cascaded H-Bridge design is well-suited for highly controlled energy flow applications where DC and AC currents are separated nicely. Crucially, to clarify, each module requires just one solitary DC input, simplifying the setup [17, 18]. That characteristic has made it extremely attractive for renewable energy sources such as solar panels, fuel cells, and even biomass generators [19]. In essence, the proposed circuit can be viewed as a standard 1-ϕ H-bridge paired with a capacitor voltage divider and five bidirectional switches formed by capacitors C_1 through C_6, as illustrated in Figure 1. Because the cascaded H-Bridge uses fewer active switches, capacitors, and diodes compared to older topologies, it eases component-count headaches for designers [20]. When a photovoltaic panel feeds into the system, a boost converter lifts the voltage to the required level, and the transformer-free multilevel inverter does the rest, feeding clean power to the grid. With accurate timing, that setup can create thirteen distinct output steps: V_{dc}, $5V_{dc}/6$, $2V_{dc}/3$, $V_{dc}/2$, $V_{dc}/3$, $V_{dc}/6$, 0, $-V_{dc}/6$, $-V_{dc}/3$, $-V_{dc}/2$, $-2V_{dc}/3$, $-5V_{dc}/6$, and $-V_{dc}$.

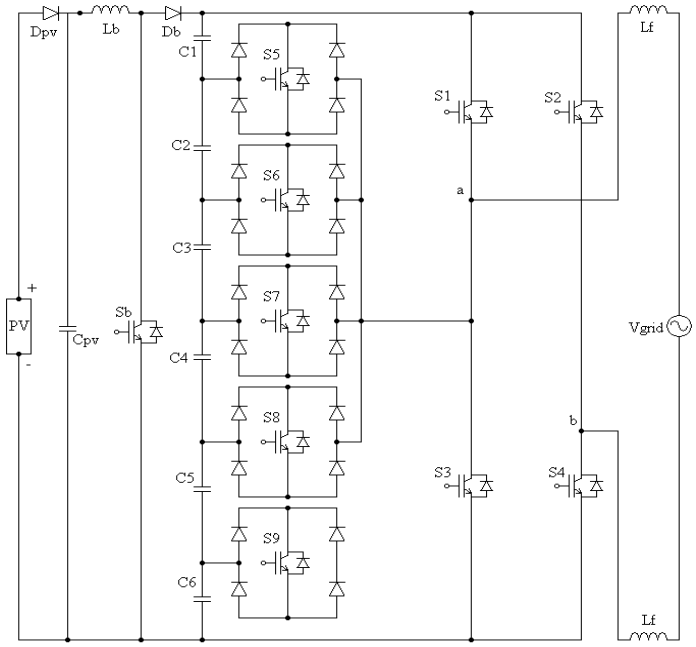


Fig. 1 Developed a 1-ϕ thirteen-level CHB grid-connected inverter for PV systems

In the considered research work, a 13-level CHBI with effective topology leads to reducing the count of power components correlated to the existing MLI. The present work requires a single DC input per module and a capacitor voltage divider compared to existing designs. The proposed work gives more efficiency and a lower cost. This results in fewer switching losses and enhances harmonic performance, making it particularly suitable for renewable resource utilization, i.e., PV systems.

3. Modes of Operation

A 1-ϕ modified CHB thirteen-level inverter uses five bidirectional switches & a series of 6 capacitors, C_2, C_3, C_4, C_5 & C_6 as a voltage-divider bank, as shown in Figure 2. Because it relies on fewer power switches, diodes, and capacitors than most other multilevel topologies, the proposed circuit offers marked savings while still reaching the equivalent count of output levels. PV arrays used in a hybrid inverter through bidirectional switches, supplying low-voltage energy that is exclusive of a boost converter, rise prior to entering the inverter. On providing higher voltage and improved power factor at once, the inverter raises both aspects, like the grid productivity and also the overall productivity of the solar system. Appropriate timing of each switch position makes the system provide thirteen different voltage levels, from V_{dc} down to $-V_{dc,}$ along with intermediate values such as $5V_{dc}/6$, $2V_{dc}/3$, $V_{dc}/2$, and $-5V_{dc}/6$.

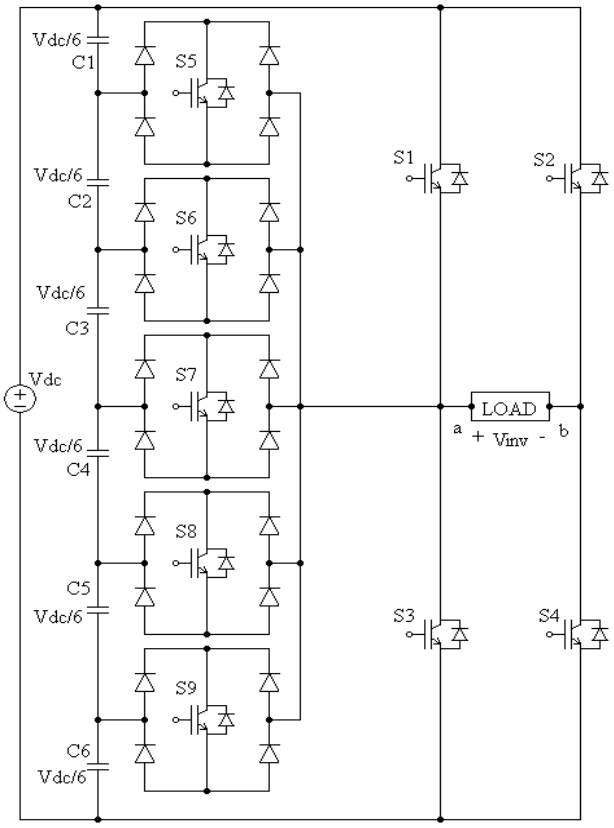


Fig. 2 Thirteen-level inverter for switching operation

Figure 3(a-n) explains the functioning of a thirteen-level inverter by cycling through a set of 13 distinct switching arrangements. With at most care switches that need to be turned on or off at any moment in time, which provides voltage levels also with respect to the generated voltage output.

3.1. Positive Output Voltage (Maximum) (V_{dc})

When switch S_1 closes, the +Ve terminal of the DC origin, labelled V_{dc}, is immediately connected to the positive side of the load. At almost the same instant, S_4 also closes, connecting the load's -Ve terminal directly to ground. These two actions together create an uninterrupted route for current: it leaves the source, moves through the load, and returns to ground. Because every other switch in the circuit is held off, stray paths that might dilute this flow are completely blocked. With no voltage drops outside the load, the full source voltage, V_{dc}, appears across the load terminals—its positive side sitting at V_{dc} and its negative side at ground. Thus, the load experiences a net voltage of $+V_{dc}$. Figure 3-a traces the current's journey through these closed switches, clearly showing that, in this state, the inverter is delivering its maximum positive output to the load.

3.2. Positive Output Voltage (Five-Sixth) ($5V_{dc}/6$)

When switch S_5 is closed, a direct link is made between the +Ve terminal of the load and the +Ve side of the DC source V_{dc}. Simultaneously, switch S_4 is also closed, creating a low-resistance return path from the -Ve terminal of the load to ground. Together, these two switches define a controlled current path through the load, and the remaining switches in the inverter are kept open to block any unintended alternate routes. As a result, only the prescribed voltage level reaches the load, avoiding inductive or capacitive coupling that might distort the operation. Importantly, the load does not receive the full DC voltage; it experiences roughly $5V_{dc}/6$ because of the multilevel configuration and its modulation scheme, which stacks discrete voltages to mimic a sinusoidal output. Fig. 3-b the true path through this state, showing how conductive paths and active components move, and letting the reader easily follow how intermediate voltage steps are carried to the load.

3.3. Positive Output Voltage (Two-Thirds) (2 Vdc/3)

If the bi-directional switch S_6 is turned on, its contacts unify the load's +Ve ultimate with the positive rail at the supply voltage, Vdc. At the same time, switch S_4 also closes to form one very resistance-less connection between the load negative side on one side to the earth ground at the other. This configuration provides engineers a good way to make sure to have as accurate a voltage across the load as possible for these two closures, and provides a stable and predictable pattern for current. This series of additional switches for the inverter circuit has to be cut off in that interval so that only S_6 and S_4 will be operational during the induction process. In the proposed design, the voltage in each set given loads is eventually 2Vdc/3, as two-thirds of the bus voltage, hence

offering a more isolated process to add to the entire input waveform of the multilevel inverter. For this mediation state, this switch pair is chosen by the monitoring algorithm as per the modulation strategy, and any other devices are permitted to participate. In a typical fashion, current flows from the DC bus, goes through S6, across the load, and back through S_4 to ground, following the envisioned low-inductance loop. This trajectory with an active device schematic is depicted along with that path in Figure 3(c) for monitoring the conduction order in situ, which is made evident to an observer. The measured performance matches both the design calculations and the simulation results, confirming that the inverter reliably produces the targeted output voltage.

3.4. Positive Output Voltage (Half) ($V_{dc}/2$)

With the bidirectional switch S_7 transformed on, the +Ve side of the load connects directly to V_{dc}, while switch S_4, also turned on, grounds the load's negative side. None of the other controller switches is active, so their circuits remain open. Under these conditions, the voltage seen at the load terminals measures roughly half of V_{dc}. Current paths shown in Figure 3-d confirm that only these two switches guide the flow at this moment.

3.5. Positive Output Voltage (One-Third) ($V_{dc}/3$)

With the bi-directional switch S_8 turned on, the loads' +Ve terminal is tied directly to V_{dc}; also, when switch S_4 turns on, the loads -Ve terminal connects to ground. Because entire other control switches remain off during this step, only these two paths provide power to the load. Under this set of conditions, the voltage seen at the load terminal settles at roughly $1/3^{rd}$ of the main bus voltage, or $V_{dc}/3$. As illustrated within Figure 3(e), the current flows along the routes shown, confirming that the intended circuit section is active at this moment.

3.6. Positive Output Voltage (One-Sixth) ($V_{dc}/6$)

With the bidirectional switch S_9 transformed on, the +Ve side of the load links directly to V_{dc}. At the same time, switch S_4 closes the negative side to ground. Every other switch in the controller remains off, isolating those pathways. Under these conditions, the voltage over the load is limited to V_{dc} divided by six. The current diagrams shown in Figure 3(f) clearly outline the active routes at this point.

3.7. Output Voltage (Zero) (0 & 0)*

The user can reach this condition in two ways. User either turns on switches S_3 & S_4, or you turn on S_1 & S_2 while making sure every other switch stays off. When the user do that, the two points marked 'ab' are basically wired together, and no voltage reaches the load. The user can see the active current paths drawn in Figures 3(g) and 3(h).

3.8. Negative Output-Voltage (One-Sixth) ($V_{dc}/6$)

In the present switching configuration, the bidirectional switch S_5 is activated, creating a direct conduction route that links the load's +Ve terminal toward the DC bus (V_{dc}) via the control channel. Concurrently, switch S_2 is turned ON, clamping the load's -Ve terminal firmly to ground, also thereby closing the current loop. All other switches in the inverter stack remain OFF, preventing any stray current paths from disrupting the refined operation the design seeks.

The result of this deliberate switching pattern is that the voltage appearing across the load rests near $-V_{dc}/6$. The negative sign stems from the precise arrangement of active devices and the way the DC source voltage divides among them. Only a sixth of the absolute DC link voltage appears, a level that the switching sequence has been tuned to produce as one of the lower steps in the thirteen-level output staircase. Figure 3(i) depicts the active current flow paths for the circuit under consideration. From that image, one can trace the conduction loop that begins at the positive terminal of the direct-current source, moves through switch S_5, passes across the load, and then leaves the system through switch S_2 to reach ground. This configuration sits within a larger multilevel switching strategy in which each precisely selected state combines to create a productivity voltage that closely simulates a sine wave. The inverter's operating condition is thus good enough to satisfy high power quality criteria and low THD, not to mention the fact that it utilizes fewer switches than it would in traditional situations.

3.9. Negative Output Voltage (Vdc/3)

Currently in the switching sequence, the main switch S6 is engaged, which directly connects the positive part of the load to the positive supply rail Vdc. Switch S2 is in turn delivering a conductive path from the load's negative terminal to ground in the cycle. The remaining inverter flow lines contain all other switches that are functionless, which hinder alternate current flows and prevent possible short circuits. With this sharp arrangement, the load measures a voltage of $-V_{dc}/3$. Switching topology and its voltage distribution logic - Ve one-third of the DC link. Current paths shown in Figure 3(j) verify that only active switches S_6 and S_2 are carrying conduction; no other branches affect the circuit at this moment. The figure thus serves as a clear trace for how current loops through the inverter stages and the load, further validating the reported output voltage.

3.10. Negative Output-Voltage (Half) ($V_{dc}/2$)

The two-way switch S_7 is turned on, linking the load's +Ve side to V_{dc}, while switch S_2 is also turned on, grounding the load's -Ve side. All the other switches in the controller stay off. Because of this setup, the voltage at the load terminal ends up being $-V_{dc}$ divided by 2. The user can see how the current flows in those paths in Figure 3(k).

3.11. Negative Output Voltage (Two-Third) ($2V_{dc}/3$)

The bi-directional switch S8 is turned on, which links loads +Ve side to V_{dc}, while switch S_2 is also on, linking the loads -Ve side straight into ground. All the other control

switches stay off. Because of this setup, the voltage at the load terminal drops to about $-2V_{dc}/3$. Figure 3(l) shows which current paths are live right now.

3.12. Negative Output Voltage (Five-Sixth) ($5V_{dc}/6$)

With switch S_9 closed, the positive side of the load connects directly to the V_{dc} rail. At the same time, S_2 is on, tying the load's -Ve terminal to ground. The entire alternative switches remain off while these two are active. Because of that, the load sees roughly $-5V_{dc}/6$ across its terminals. To see which current paths are now live, check Figure 3(m).

3.13. Negative Output Voltage (Maximum) ($-V_{dc}$)

In this switching configuration, S_2 is turned ON, creating a direct path from the positive side of the load to the supply voltage V_{dc}. Simultaneously, S_3 is activated, relating the load's negative ultimate straight to the ground. Entire alternate switches in the inverter remain OFF, blocking any stray conduction routes and averting unwanted overlap of switching signals. By controlling the states in this way, the circuit confines current to the intended branches, providing the load with a stable and well-defined voltage.

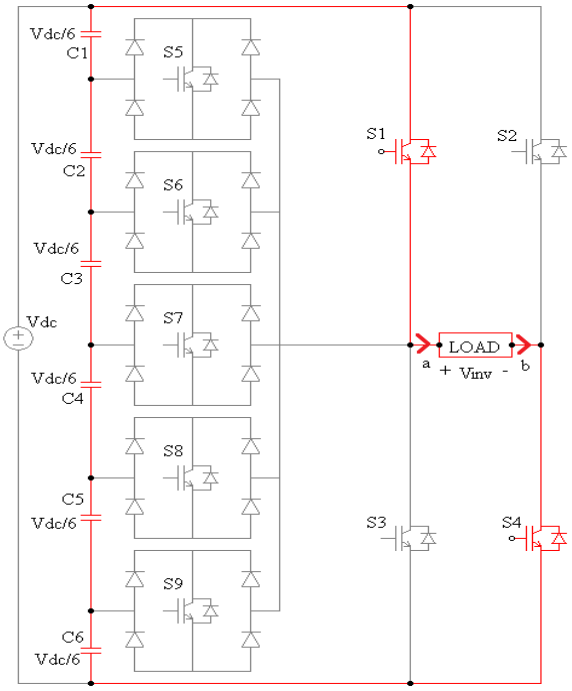


Fig. 3(a) $V_{ab}=V_{dc}$

Because of this switching arrangement, the entire DC supply voltage V_{dc} appears directly across the load but with reversed polarity, so the load sees a voltage of $-V_{dc}$. In practical terms, this forces the current to begin at the negative terminal of the source, move through the load in an opposite sense, and finally return to ground; thus, the system is operating under a stable negative voltage condition. The specific routes the current takes during this phase, and only those routes, are shown clearly in Figure 3(n). As the figure proves, only the switches S_2 and S_3 are transformed on at this moment; also, the sketch traces the flow through the power circuit and across the load for anyone following the diagram. Operating in this state adds a unique voltage level to the multilevel inverter output, and that added level is essential for forming the overall waveform that the inverter delivers.

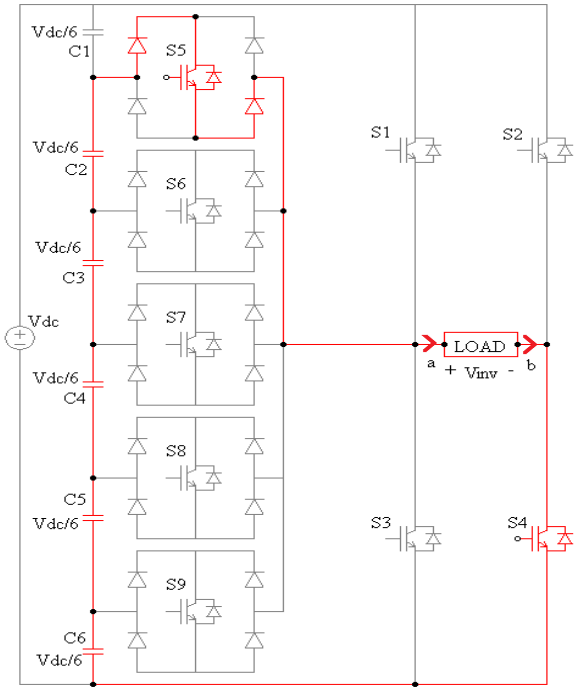


Fig. 3(b) $V_{ab} = 5V_{dc}/6$

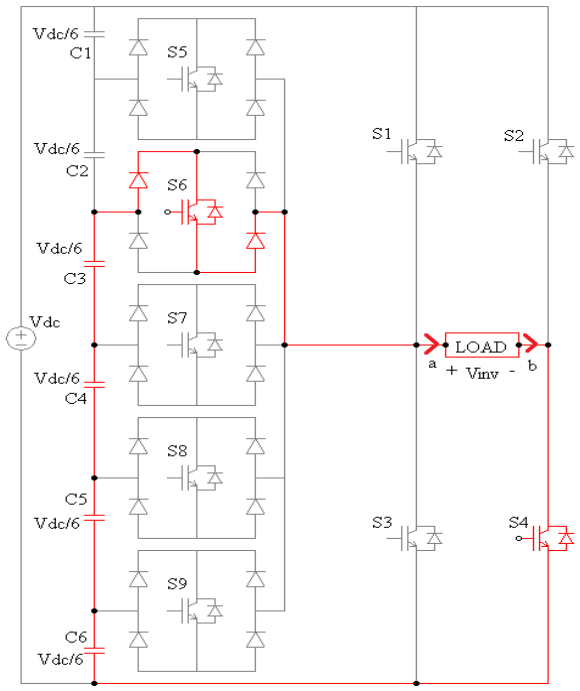


Fig. 3(c) $V_{ab} = 2V_{dc}/3$

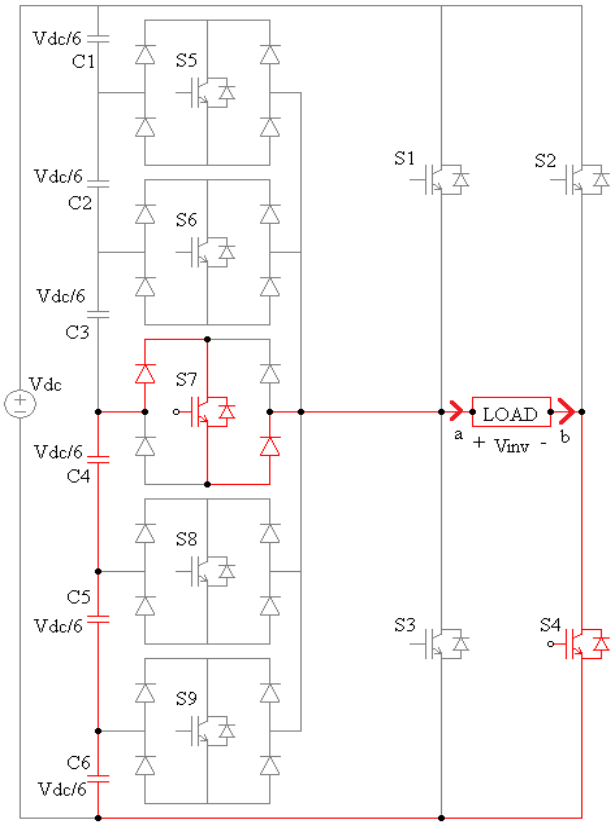


Fig. 3 (d) $V_{ab} = V_{dc}/2$

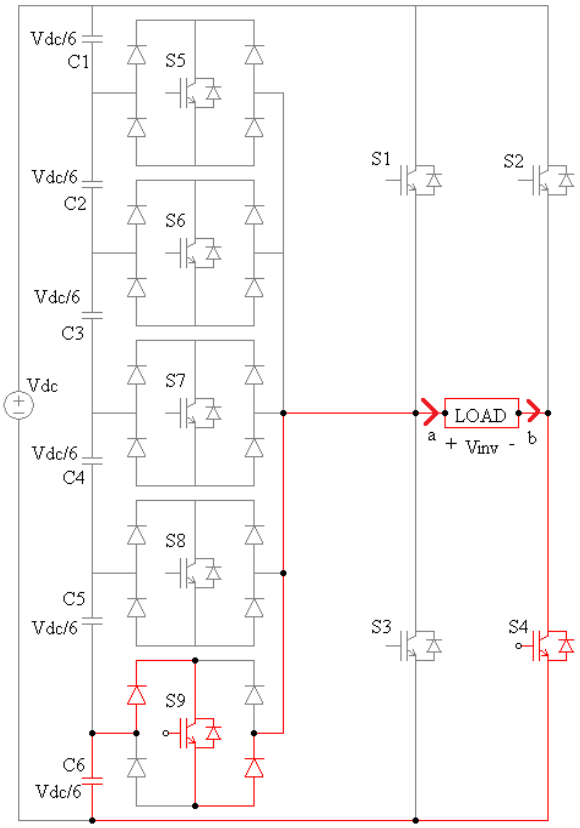


Fig. 3 (f) $V_{ab} = V_{dc}/6$

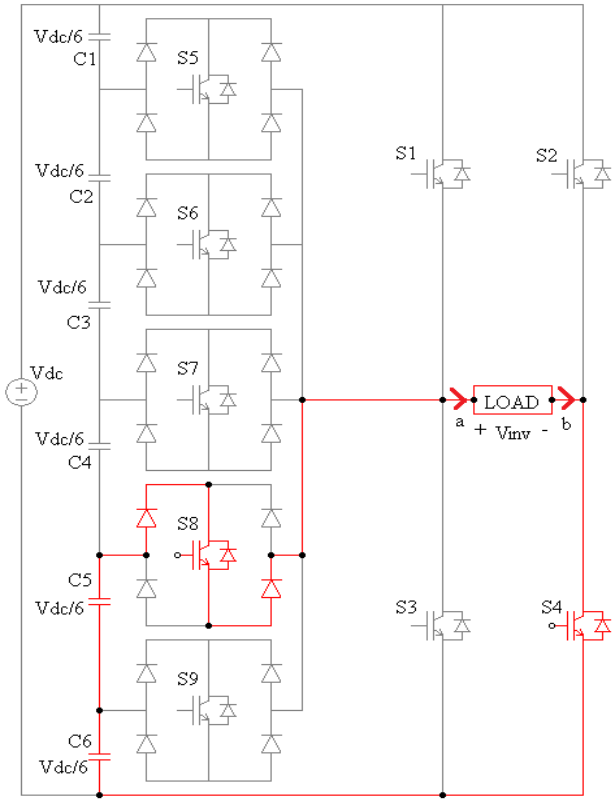


Fig. 3 (e) $V_{ab} = V_{dc}/3$

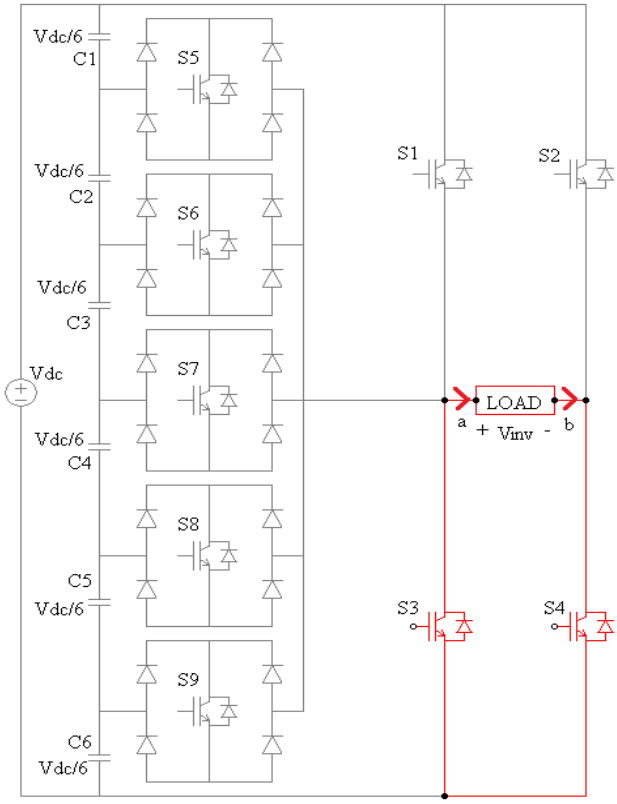


Fig. 3 (g) $V_{ab} = 0$

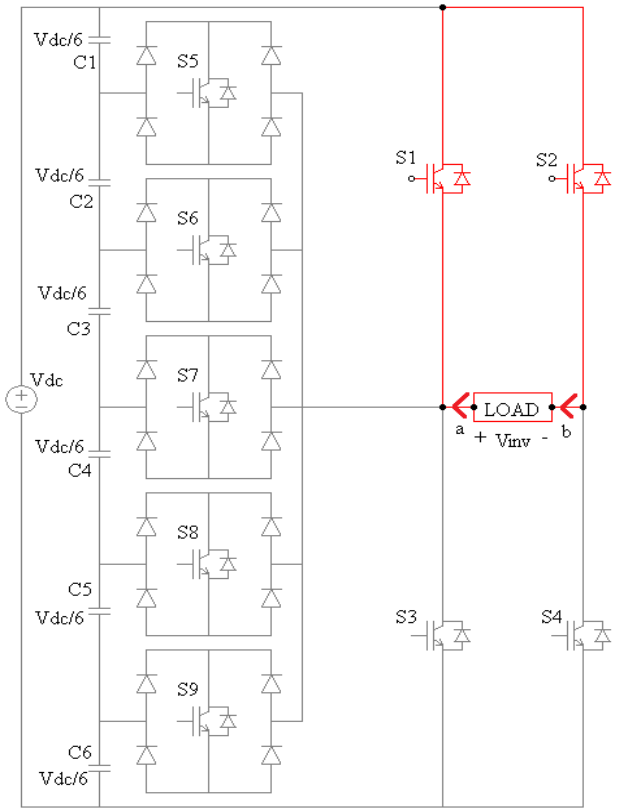


Fig. 3 (h) V_{ab} = 0*

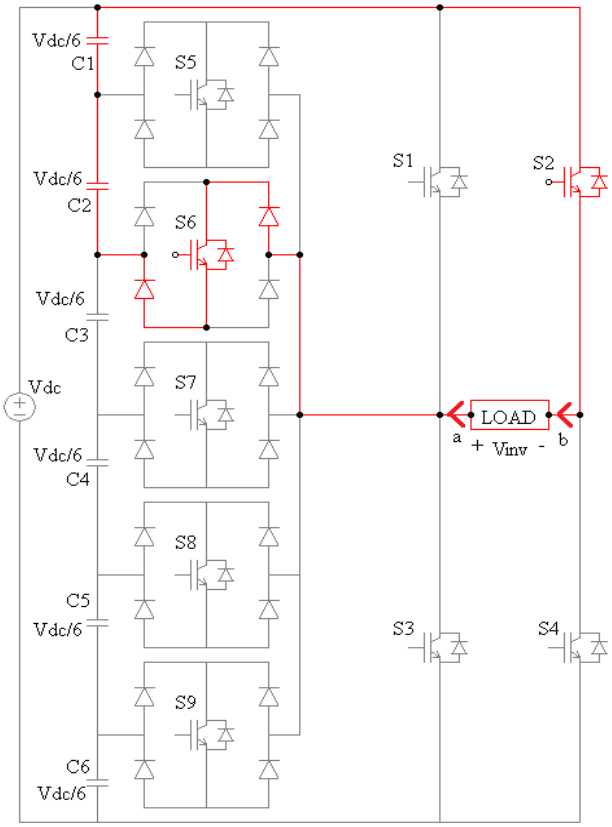


Fig. 3 (j) $V_{ab} = -V_{dc}/3$

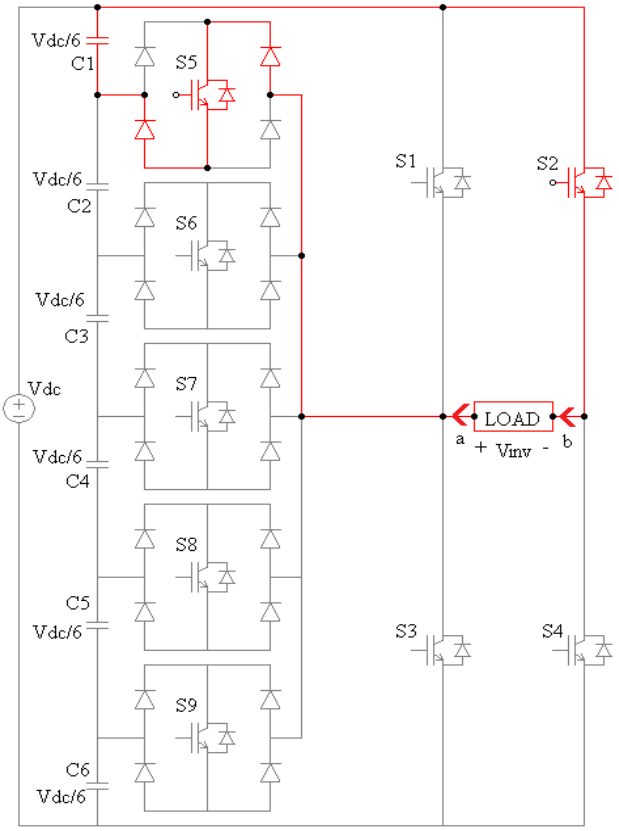


Fig. 3 (i) $V_{ab} = -V_{dc}/6$

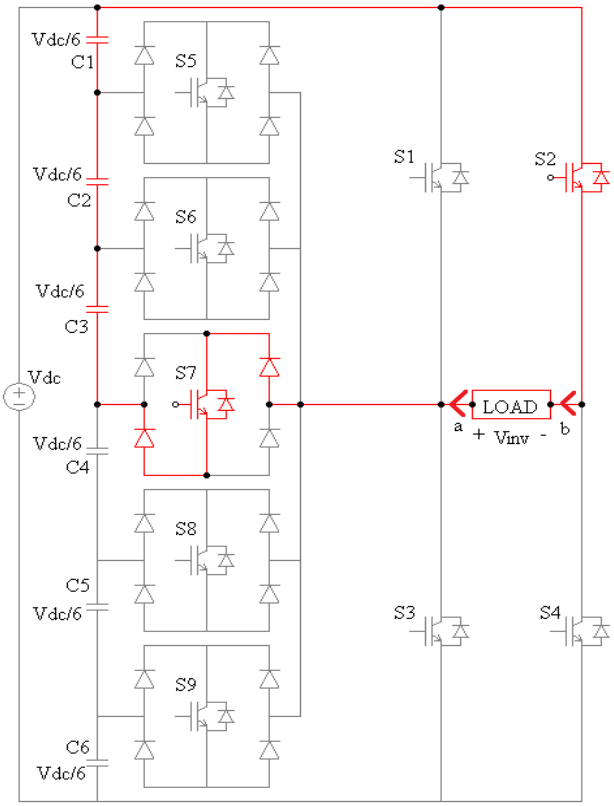


Fig. 3 (k) $V_{ab} = -V_{dc}/2$

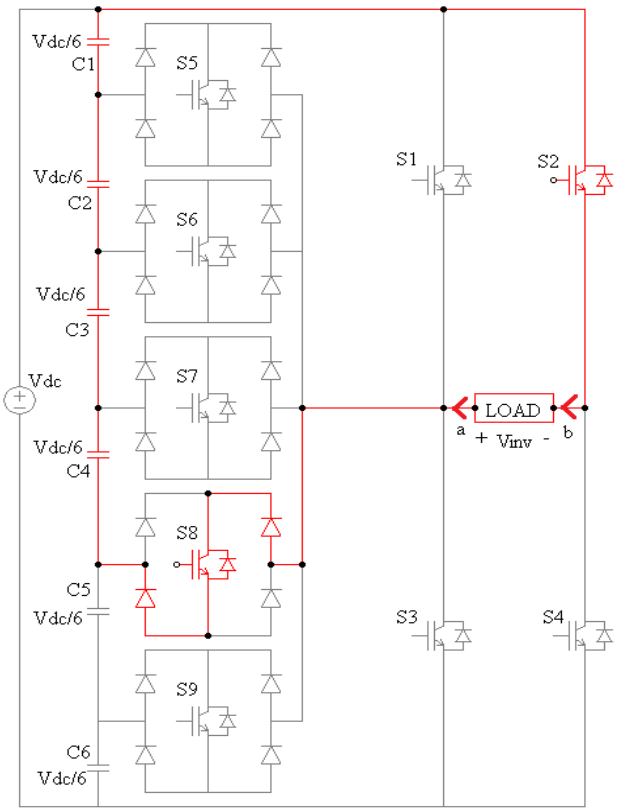


Fig. 3 (l) $V_{ab} = -2V_{dc}/3$

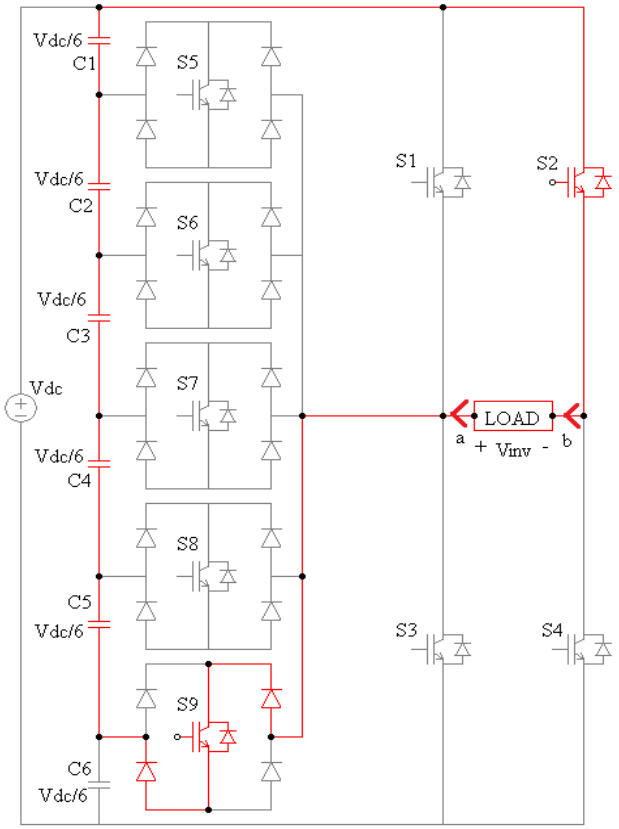


Fig. 3 (m) $V_{ab} = -5V_{dc}/6$

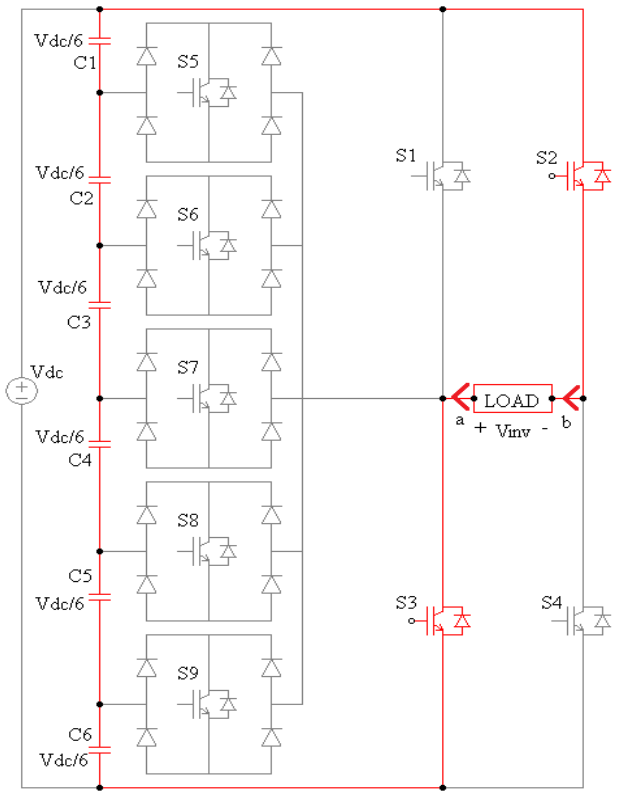


Fig. 3 (n) $V_{ab} = -V_{dc}$

Fig. 3 Switch combination required for generating the production voltage (V_{dc})

Table 1. Production Voltage Based on the Switching ON-OFF Status

V_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
V_{dc}	T	F	F	T	F	F	F	F	F
$5V_{dc}/6$	F	F	F	T	T	F	F	F	F
$2V_{dc}/3$	F	F	F	T	F	T	F	F	F
$V_{dc}/2$	F	F	F	T	F	F	T	F	F
$V_{dc}/3$	F	F	F	T	F	F	F	T	F
$V_{dc}/6$	F	F	F	T	F	F	F	F	T
0	F	F	T	T	F	F	F	F	F
0*	T	T	F	F	F	F	F	F	F
$-V_{dc}/6$	F	T	F	F	T	F	F	F	F
$-V_{dc}/3$	F	T	F	F	F	T	F	F	F
$-V_{dc}/2$	F	T	F	F	F	F	T	F	F
$-2V_{dc}/3$	F	T	F	F	F	F	F	T	F
$-5V_{dc}/6$	F	T	F	F	F	F	F	F	T
$-V_{dc}$	F	T	T	F	F	F	F	F	F

Where, T – Switch is 'ON' & F – Switch is 'OFF'

Operation of a CHBMLI relies on an ordered sequence of control signals sent to switches S_1 through S_9; each sequence sets a distinct output voltage, V_{dc}, across the load. If only switches S_1 and S_4 are closed, with the others left open, the circuit delivers its highest voltage, V_{dc}. To lower the output to $5V_{dc}/6$, the controller opens S_1 and closes S_5. For the level $2V_{dc}/3$, the pair S_4 and S_6 is switched on, whereas $V_{dc}/2$ is reached by activating S_4 and S_7 as in Table.1. Continuing

down the scale, $V_{dc}/3$ appears when S_4 and S_8 conduct, and for $V_{dc}/6$ the only active pair is S_4 with S_9. At the neutral voltage point, $V_{dc} = 0$, the inverter can enter two separate states. One state keeps S_3 and S_4 illuminated; the complementary state, noted as 0*, energizes S_1 and S_2. Having this dual choice permits engineers to optimize the output waveform and to minimize the power wasted in each switch during turn-on and turn-off cycles. To produce negative output voltages, the inverter reverses the normal switching order. For the level of $-V_{dc}/6$, switches S_2 and S_5 are closed. When S_2 and S_6 act close, the production voltage reaches $-V_{dc}/3$; closing S_2 and S_7 raises it to $-V_{dc}/2$. More negative levels- $-2V_{dc}/3$ and $-5V_{dc}/6$- appear as S_2 joins S_8 or S_9, respectively. By closing S_2 and S_3 and keeping all other switches off, a full output of $-V_{dc}$ can be generated. An inverter can produce 15 different voltage steps by precisely operating in an on-off pattern in the zero state, which gives almost sinusoidal output and less harmonic distortion.

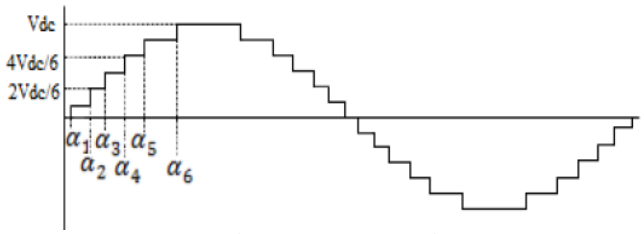


Fig. 4 Switching pattern for single-phase modified CHB thirteen-level inverter

4. Closed Loop Control System

The closed-loop system comprises MPPT, a fuzzy controller, and an inverter driver, as illustrated in Figure 5. The task of the MPPT section is to obtain as much solar energy as possible and put that cleaner, low-harmonic power into the grid. It starts by finding the panel's voltage Vpv and current Ipv - both readings fed into MPPT's brain. Considering the above numerics, the controller regulates duty cycles to ensure the panels will hum. A pulse-width modulation (PWM) wave then clocks the signal to the boost converter. Within the fuzzy rule set, the actual bus voltage Vdc is compared to a specific target Vdc*.

When the two do not match, the fuzzy engine revises the commands until they sync. When V_{dc} sits where it should, it will take this steady voltage to the grid, flowing through the inverter switch stage. Gate pulses then light up each inverter switch, starting from S_1 to S_9. This methodology is concerned with increasing the MPPT, namely tracking the maximum power point accurately and with greater speed under different conditions, and its adaptive fault-tolerant control, improving the energy recovery from solar panels. The boost converter design also reduces switching losses and voltage ripple through uniform modulation and control, improving efficiency and stability of the output. Together, this approach provided improved MPPT and boost converter topology with higher efficiency, good dynamic response, and scalability for different renewable energy applications.

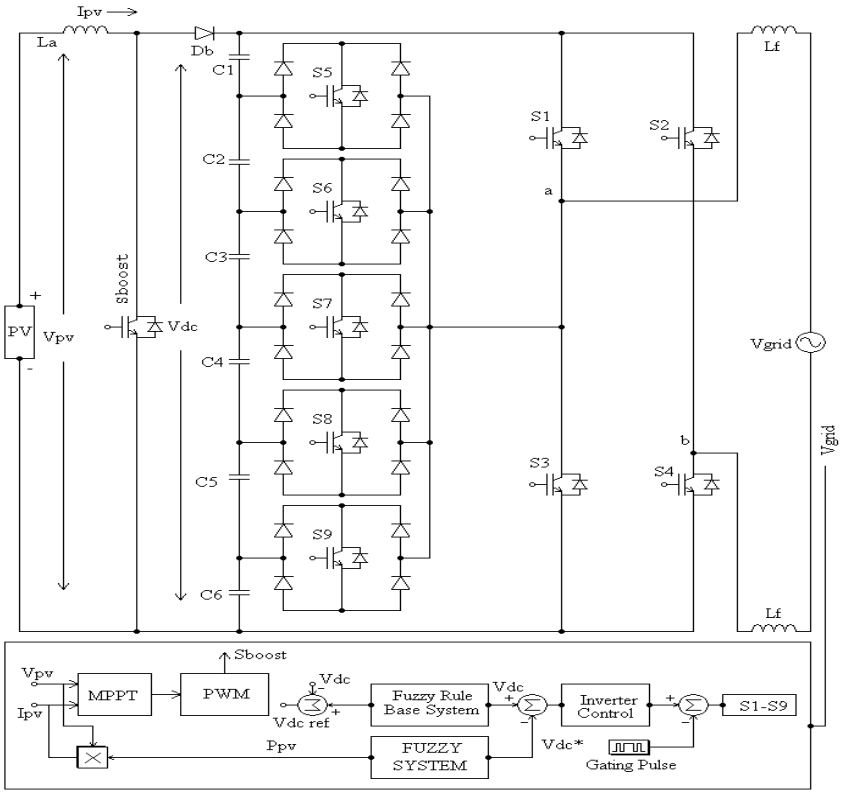


Fig. 5 Single-phase thirteen-level inverter with closed-loop controller

4.1. Simulation Result

The proposed method has been implemented in MATLAB_SIMULINK situation along with the SIMPOWER compromise toolbox as shown in Figure 6. The whole thing was set up in MATLAB/SIMULINK and runs with the SIMPOWER system toolbox. With the Pulse Width Modulation method, we got the switching signals and patterns you see in Figure 7. Figure 8 then shows the production voltage from the 13-level CHB inverter. We used a Fast Fourier Transform (FFT) test, exposed in Figure 9, and found that the system's Total Harmonic Distortion (THD) is 2.74%.

The present 13-level CHBMLI performance validation can be evaluated through simulations carried out using MATLAB/SIMULINK and PROTEUS for evaluating hardware-level emulation. This work gives practical operating conditions, especially for a 1-φ PV system.

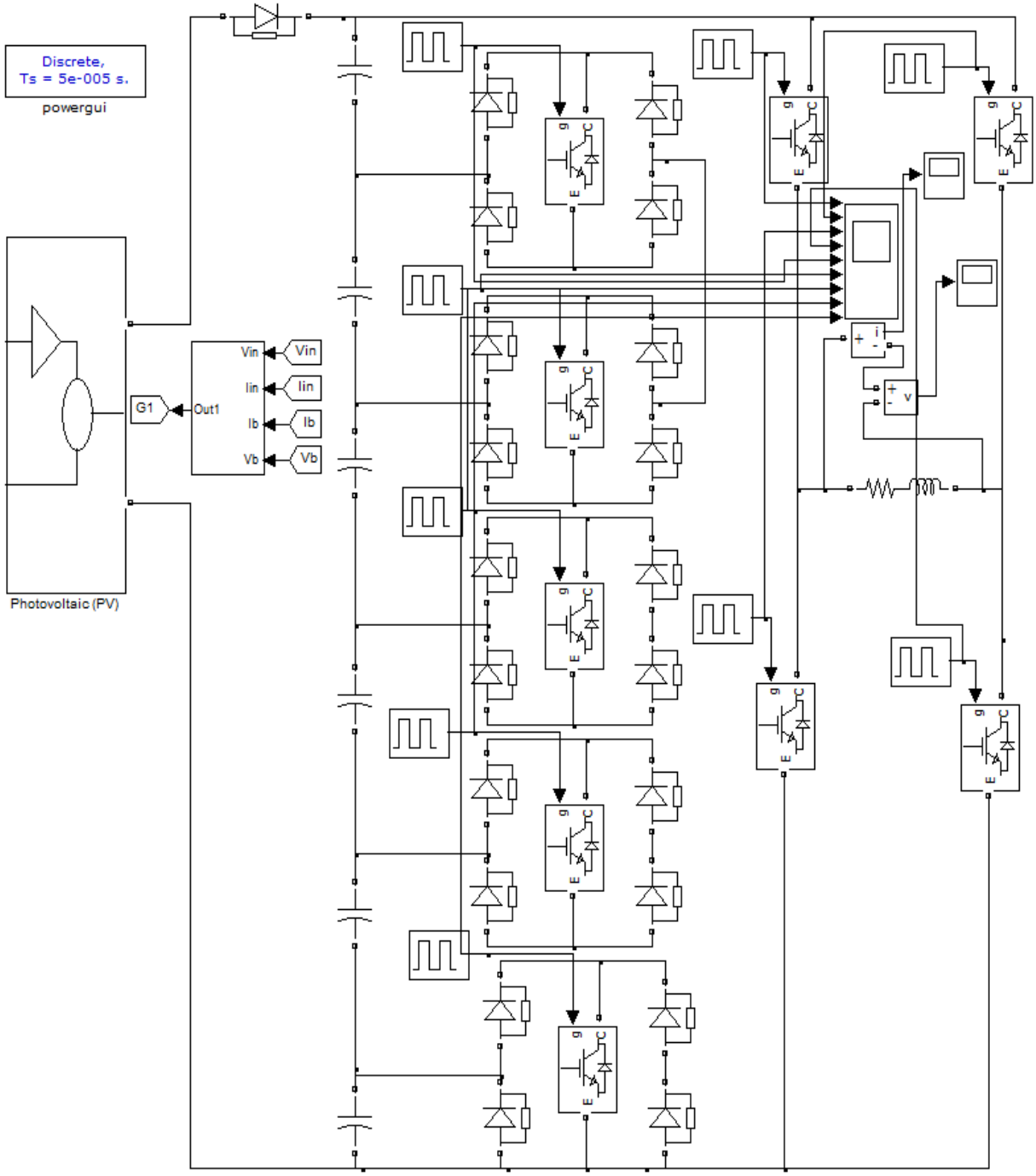


Fig. 6 Simulation circuit for the CHB thirteen-level inverter

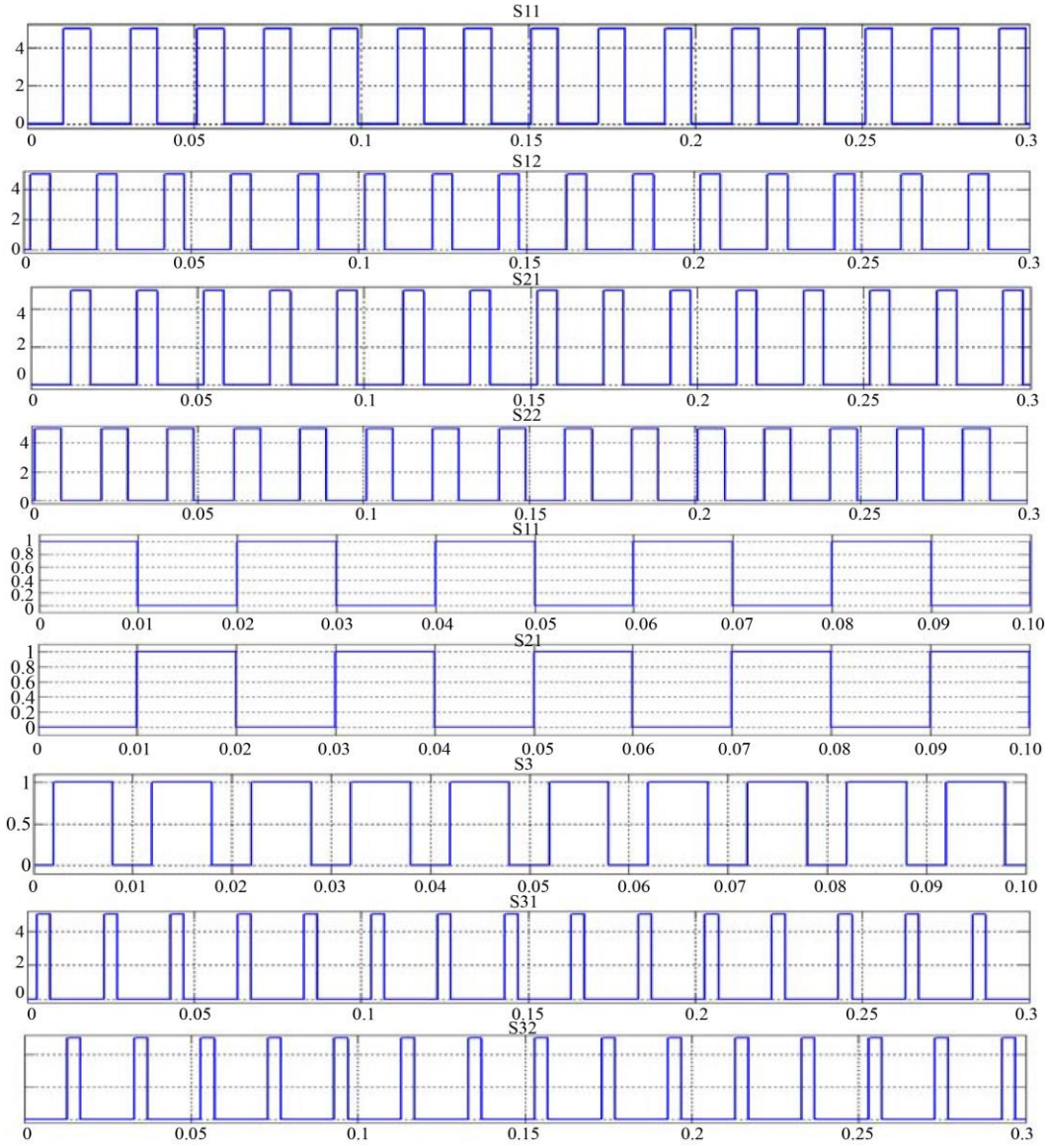


Fig. 7 Gating pulse for the CHB thirteen-level inverter

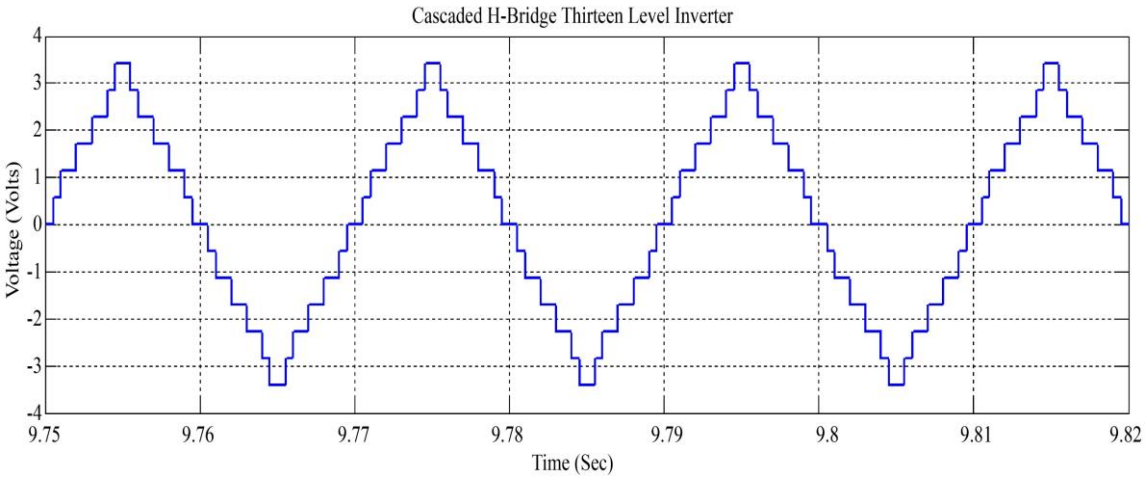


Fig. 8 Output voltage waveforms for cascaded thirteen-level inverter

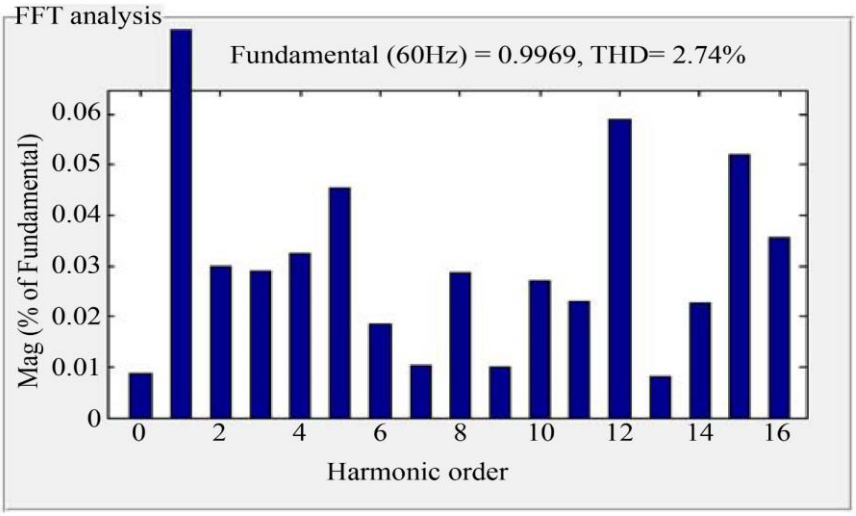


Fig. 9 THD for altered CHBI

4.1.1. Design Specification

Short Circuit Current (I_{sc}) – 8.43A; Open – Circuit Voltage (V_{oc}) – 38V; Current at MPP I_{max} – 7.35A; Voltage at MPP V_{max} – 29V; Power rating (P_{max}) – 213W; Cells per module – 60; SPV V_{dc} – 45-60V; Ipv – 4-6A; Boost Converter V_{dc} – 300V; L – 2.5mH; f_{boost} – 20kHz; Fuzzy Controller – 25 rule base MAMDANI system; Ts=10µs.

4.2. PROTEUS Model

Proteus is probably the ultimate preeminent simulator out there. It can represent most circuits that users can think of that deal with electric fields. Its point-and-click screen looks so much like a real breadboard that new users start building faster. On top of that, users can also lay out and test a printed circuit board, or PCB. Figure 10 shows the Modified Cascaded Thirteen Level Inverter built in Proteus along with its output pulses, while Figures 11 and 12 show the wave patterns for the whole 13 Level Inverter. Proposed a 13-level CHBI gives better results when compared to existing methods because of a reduced number of active switches and capacitors due to lower cost and complexity in the existing design, requiring more isolated DC sources, as the present approach uses a single DC input per module with a capacitor voltage divider.

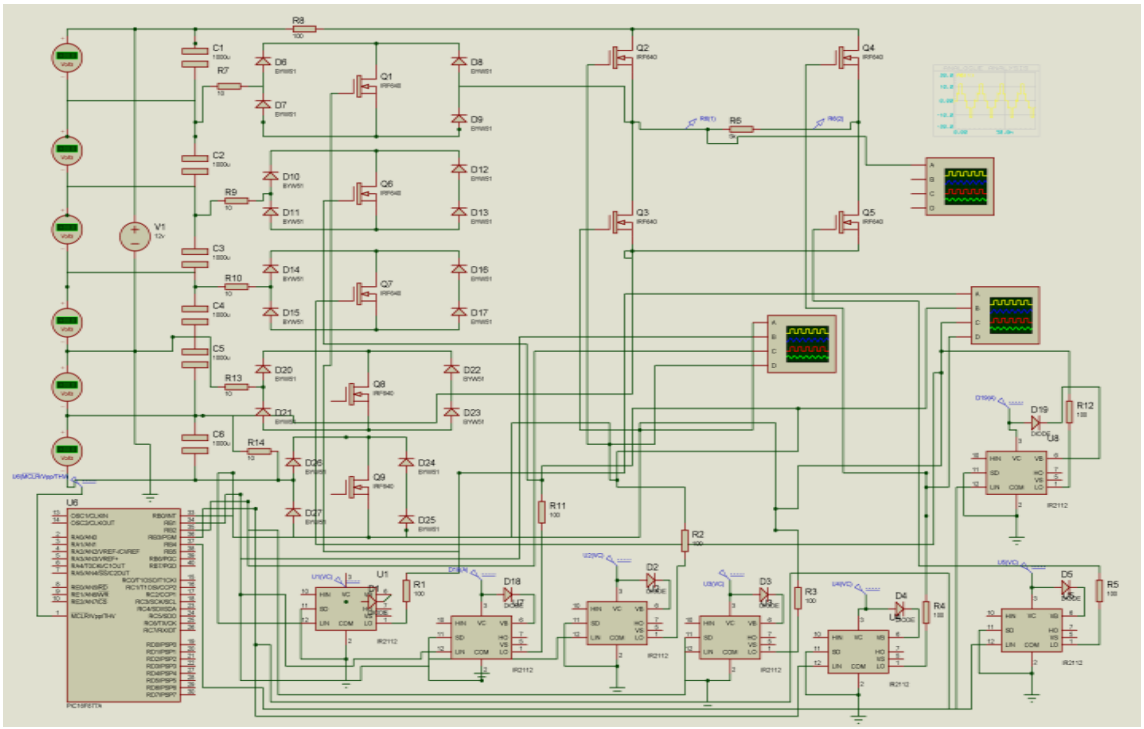
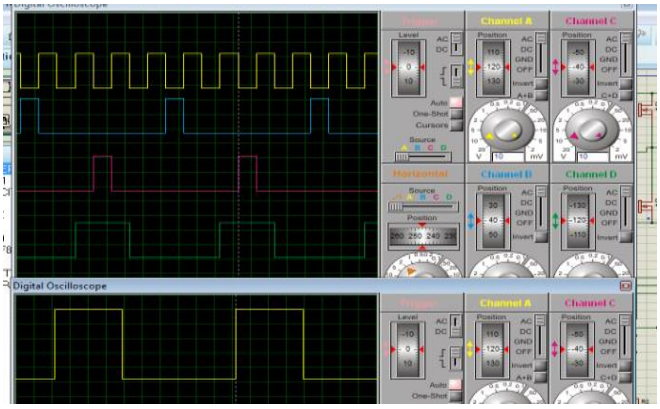


Fig. 10 Modified cascaded 13-level inverter developed in PROTEUS



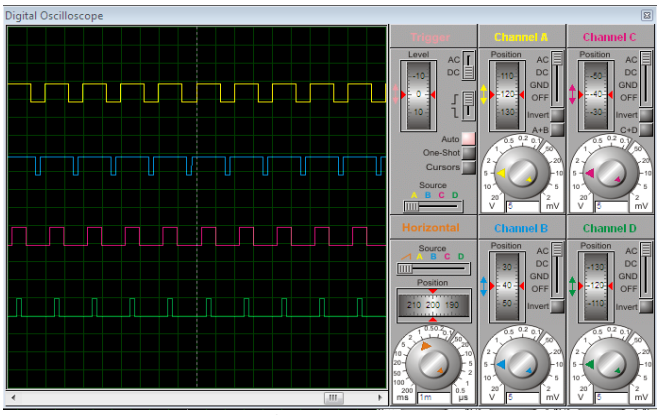


Fig. 11 Output pulses for the CHB thirteen-level inverter

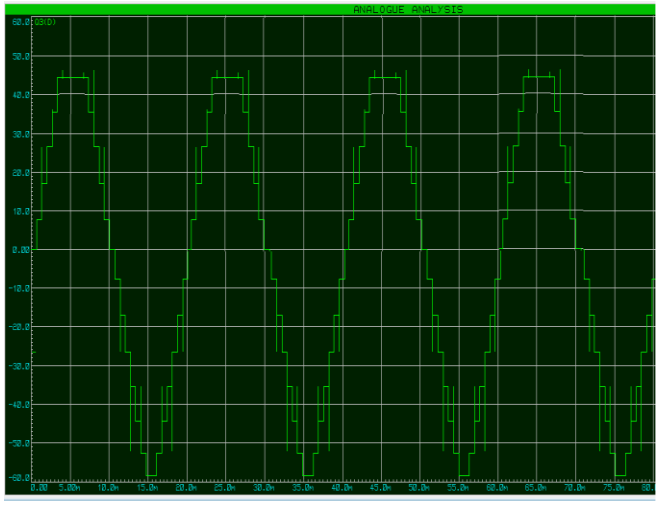


Fig. 12 Production voltage for the modified cascaded 13-level inverter

Hence, lower switching losses, enhanced efficiency, and less THD are achieved. In a nutshell, the present topology gives better output, higher efficiency, and greater scalability correlated to modernization solutions. The 13 eleven modified CHBI, which is proposed in the present work, is developed for evaluating simulation results and their practical feasibility. This prototype reflects the simulation topology with applicable modifications for industry applications, such as switching delays and circuit safety.

4.2.1. Design Specification

Microcontroller – PIC16F877A; Gate driver – IR2110; Capacitor - 100µF; V_{dc} – 300V; Load – R, PWM – Sine triangular. Simulation results of the proposed 13-level CHBMLI topology, PROTEUS model, show its practical viability, producing output with lower switching losses, less switching count, and enabling better harmonic performance.

Results show the reliance of the design, which supports its application in a practical SPV-based system. THD reduces by 34.76% in the proposed method. The proposed method works with balanced switching loss and complexity, which ensures its suitability for practical applications. The proposed method can easily be scaled for the required level of applications. Since the complexity is low, it is cost-effective and scalable than existing designs.

5. Comparison of Existing State-of-the-Art Topologies

More recent developments of the Multilevel Inverter (MLI) technologies have aimed at decreasing the number of switches, decreasing the necessity of isolated DC sources, decreasing voltage stress, and enhancing THD performance. The effectiveness of the proposed 13-level CHB topology was compared with commonly used state-of-the-art topologies, including diode-clamped MLIs, flying-capacitor MLIs, conventional CHB, and reduced-switch-count modifications in the literature [1-7].

5.1. Structural Requirement Comparison

Conventional CHB inverters use several isolated DC sources per H-bridge cell, which is highly expensive and complicated in PV applications. Flying-capacitor inverters and diode-clamped inverters have too many clamping diodes and too many capacitor banks, respectively, which are hard to balance and scale. The proposed setup would only require One DC input per module, A basic voltage divider [capacitor], and five bidirectional switches. This is a visible factor of reduction of the amount of components used as compared to the 9-12 active switches of existing 13-level CHB architectures and 20-24 switches of diode-clamped and flying-capacitor architectures. The voltage stress, switching losses, and performance of the switching regulator versus other power systems will be compared. The differences in performance are summarized in Table 2. Typical CHB inverters have a THD of 4-6, with diode-clamped inverters and flying-capacitor inverters having 3.5-5% THD. Variants with reduced switch variants in [1-4] have THD values close to 3-4, though at the expense of increased voltage stress across switching devices or asymmetric DC sources. The suggested topology will obtain: THD = 2.74%, Stress in voltage between terminals, caused by capacitor division. This shows a 34.76 percent higher improvement in THD than traditional methods, which confirms the harmonic excellence of the given structure. The suggested architecture has a number of benefits in comparison to the recent approaches illustrated in Table 2.

Table 2. Comparison of proposed 13 level CHB inverter vs. Existing state-of-the-art multilevel topologies

Topology	DC Sources	Switch Count	Balancing Complexity	THD (%)	Remarks
Diode-clamped MLI	1	Very high (20+)	Clamping diodes, which are hard to balance	3.5–5	High voltage stress
Flying-capacitor MLI	1	Very high (20+)	Complex balancing of capacitance	3–5	Bigger and more expensive
Traditional CHB	Multiple	Medium	DC sources are a prerequisite	4–6	Non-PV-friendly
Reduced-switch CHB (literature)	1–2	Low–medium	Depends on asymmetry	3–4	Higher voltage stress
Proposed 13-level CHB	1	Low (9 switches)	Simple divider, no balancing problem	2.74	Minimal losses and Maximum scalability

5.2. Comparison to Existing CHB-MLI Topologies

The current trends in Cascaded H-Bridge Multilevel Inverters (CHB-MLIs) have been centered on the reduction of the number of power switches, a smaller need for isolated DC sources, low THD, and power conversion efficiency.

In order to prove the importance of the presented thirteen-level CHB topology, a comparison with related studies has been done in detail. In contrast to conventional baseline models, the discussion below focuses on emerging reduced-switch and PV-oriented CHB models in the literature.

A number of reduced-switch CHBMLI designs have been provided to reduce cost and complexity without affecting harmonic performance. A thirteen-level topology with seven switches, which is reported in [21], illustrated the structural simplification but had a relatively high Total Harmonic Distortion (THD ≈ 9.18%). Though the number of switches is less, the resulting distortion makes it less applicable in grid-connected PV applications where the power quality requirements are high. Comparatively, the topology suggested has an equally low number of hardware but a significantly lower THD of 2.74 per cent, meaning that the waveform quality is better.

In [22], the authors also examined symmetric and asymmetric multilevel inverter topologies with the focus on the minimization of the number of power semiconductor devices. A proposal was made for an asymmetric inverter design with thirteen levels based on the use of a series of unequal DC voltage sources to obtain higher levels of output voltages with a lower number of switches.

The reported topology shows good harmonic performance with a Total Harmonic Distortion (THD) of 5.86 percent. The reliance on multiple sources of independent DC, however, adds costs, complexity of control, and hardware to the system. This is a disadvantage in the topology because, in photovoltaic applications, there may be difficulties in maintaining several isolated DC sources. This results in the fact that although the number of devices decreases, the actual way of introducing the inverter in the renewable energy systems is still limited. In [23], the model of a multi-module hybrid topology was described, in which a mix of half-bridge and polarity reversal circuits allowed having thirteen voltage levels with a lower number of devices.

This design claimed to have enhanced efficiency (~98.5 percent) and tolerable harmonic (THD = 6.3 percent), although the design needs three unique DC sources and intricate control coordination. The current work has less controlling overhead and fewer sources, and thus, it provides lower THD in favour of compact PV architectures.

Higher-level systems, like the thirty-one-level asymmetric CHB inverter in [24], exhibit very high harmonic properties as they have a larger number of voltage steps. Such topologies, however, are largely dependent on unequal DC inputs, which lead to high voltage stress and difficult balancing of power.

In medium-power PV applications where simplicity and cost-effectiveness are paramount, the thirteen-level scheme suggested offers a more reasonable trade-off between the simplicity of hardware and the power quality. Recently, a reduced-switch multilevel structure aimed at integrating with the grid was reported in [25].

Despite the design achieving the desired current THD (0.5-1.2%) and lowering the number of switches, the voltage THD (0.5-15%) was still very high, which required extensive filtering. The suggested topology generates much lower voltage THD and inherently cleaner output waveform, and this means improved grid compliance and requirements of many filtering stages. The limitations are resolved in the proposed thirteen-level topology, which combines a single DC Source per module through a capacitor voltage divider, fewer devices (five bidirectional switches + one full-bridge), Low THD (2.74), and not with high switching frequency, Scalability, and compatibility with PV, reduced switching and conduction losses. Table 3 illustrates the comparative CHBMLI Topology.

Table 3. CHBMLI topology comparative

Topology	DC Sources	Switch Count	THD (%)	Key Limitations	Advantages of Proposed Topology
Reduced-switch 13-level CHB [21]	1	7	~9.18	High THD with low switch count	Lower THD (2.74%) with similar hardware
Symmetric/ Asymmetric MLI [22]	2	12 switches + 3 diodes + 1 FC	Low (better than prior topologies)	Requires flying capacitor and diodes, slightly higher circuit complexity than minimal topologies	Reduced device count, single DC source per module, PV-friendly, low THD, self-voltage balancing
Hybrid module-based 13-level inverter [23]	3	Moderate	~6.3	Complex modulation and source requirement	Less complex control; fewer sources
31-level asymmetric CHB [24]	Various	High	Very low	Asymmetric sources; high voltage stress	Lower complexity; PV-friendly
Grid-connected reduced-switch MLI [25]	1	Low	~15 (voltage)	High voltage THD requires filtering	Good quality output with no large filters

6. Conclusion

MLIs are now essential in power-electronic systems, because they raise output voltage, enhance power quality, and cut Total Harmonic Distortion (THD). By stacking small voltage steps, these converters form a staircase wave that nearly matches a pure sine curve, so large passive filters become less necessary, and delicate equipment is better protected. The structure explained in the present work gives almost ideal wave using fewer switches compared to standard multilevel switches, in turn regulates the circuit, is less expensive, has a simple design, and eases switching losses. 13-level CHBI provides good quality, minimal distortion energy conversion using a trimmed count of active devices. Novelty in the topology is rightly incorporated for balancing between performance and hardware efficiency to produce renewable plants, electric drives, and grid-tied setups, which experts consider reliable and also cost-controlling. Using MATLAB/SIMULINK and PROTEUS platforms, several simulations on the proposed inverter are conducted to analyze performance and practical feasibility. To track study state behaviour and also transient conditions, the tests are spread across a wide range of functional scenarios. Output waveform obtained, describing that a multilevel voltage profile with precise step magnitudes and minimal harmonic distortion is generated by the inverter. The results obtained clearly indicate that the proposed structure can provide clean, efficient power and a source of viable alternative to conventional multilevel topologies.

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