Architecture Design for an Adaptive Equalizer using LMS 2Tap filters

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Abstract

In this paper, an adaptive equalizer using LMS algorithm has been simulated using Modelsim software. Also the variants of LMS algorithm sign-sign, sign-data and sign-error are simulated for low complexity adaptive equalizer. Analysis of mean squared errors for LMS and its variants have been done. From the results of Modelsim, input data is taken for VHDL code simulation of LMS adaptive equalizer. The output from VHDL simulation is plotted using Modelsim. The two tap process method has improves the Architecture and the LMS adaptive equalizer is discussed here and simulation results have been obtained. The Xilinx simulation used for to finding the error data.

Index – *LMS Filter, Adaptive Equalizer, Model Sim, Xilinx.*

I. INTRODUCTION

Reconfigurable hardwares have many advantages over fixed or dedicated hardwares. Dedicated hardware provides highest performance with lower power consumption but they lack behind the reconfigurable hardware in flexibility and reusability. Reconfigurable hardware provides reprogram ability and flexibility. Numerous reconfigurable hardware platforms are available to perform the required signal processing, each has its own strengths and weaknesses in terms of performance, programmability and power consumption. Two low power techniques are presented for reducing power dissipation in the LMS adaptive filter, this being the main power consuming block within this receiver. These low power techniques are namely the decorrelating transform, this is a differential coefficient technique, and the variable length update algorithm which is a dynamic tap-length optimisation technique.

DA uses bit-serial operations and look-up tables (LUTs) to implement high throughput filters that use only about one cycle per bit of resolution regardless of filter length. However, building adaptive DA filters requires recalculating the LUTs for each adaptation which can negate any performance advantages of DA filtering. By using an auxiliary LUT with special addressing, the efficiency and throughput of DA adaptive filters can be of the same order as fixed DA filters [1]. The most popular because of its robustness, good tracking properties and simplicity, drawback of LMS is that the step size implies a compromise between speed of convergence and final misadjustment. To combine different speed LMS filters serves to alleviate this compromise, as it was demonstrated by our studies on a two filter combination that we call combination of LMS filter [2].

The use of the proposed combination algorithms in other adaptive filtering applications represents an immediate possibility of getting more benefits from the above ideas. Speeding up procedures has been designed to make the previous schemes fully effective. The computational demand of the new algorithms grows linearly with the number of filters and with their length. [3]. the available FELMS algorithms introduce significant delays in updating the adaptive filter coefficients that slow the convergence rate. In this paper, we introduce a novel algorithm called the hybrid filtered-error LMS algorithm (HFELMS) which, while still a form of the FELMS algorithm, allows users to have some freedom to construct the error filter that guarantees its convergence with a sufficiently small step size. The overall preconditioned secondary paths have all-pass responses. Then, the FXLMS and ALMS algorithms can both be applied to this preconditioned system, yielding the preconditioned FXLMS (PFXLMS) and preconditioned FELMS (PFELMS) algorithms, respectively [4].

The scale factors are the results of the correlation between the filter output signal and the I/Q components of the reference signal. Thanks to the negative feedback in the filter, these scale factors are continuously adjusted until the TX leakage is cancelled. the reference signal coupling, and the duplexer group delay. We have shown that the effect of the DC offsets can be minimized by using the sign-data variant of the LMS algorithm and by increasing the gain of the first multipliers. [5].

The estimated filtered reference and the true filtered reference signals are not all located in the right half plane. This cross-correlation matrix has a (block) Toeplitz structure whose dimension is determined by the number of adaptive filter coefficients. In fact, for a sufficiently large number of FIR filter taps, the condition appears to be both necessary and sufficient.

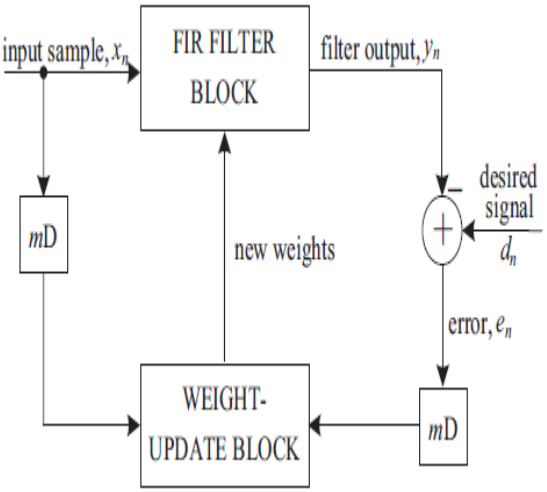
A transient analysis shows that, even if the update equation is stable, the adaptive filter coefficients may initially diverge from their final stationary values, which is called critical behaviour [6]. the number of adaptive filter coefficients is chosen to be greater than or equal to the ratio of the fundamental disturbance period to the sampling period, a simple mathematical description of the error signal is derived that approximates the actual convergence process with numerically given error bounds. The analysis is performed in the time domain, considering a discrete state-space system defining the error signal convergence. The excitation signal is assumed to be stationary. The limits of the deviation between the perturbed and unperturbed system behaviour were numerically approximated. [7].

The added stable gains (ASGs) over the limit gain when AFR subsystems are working in the digital hearing aids are studied for all the categories. The ASG is determined as a trade-off between two measurements: 1) segmented signal-to-noise ratio (objective measurement) and 2) speech quality (subjective measurement). This method is based on an estimation of the powers of the feedback-reduction subsystem output signal and its error signal. This estimation is used every algorithm iteration to update the adaptation parameter. the modelling and parameterization of the AFE path of each digital hearing-aid category is presented [8].

The LMS algorithm does not favour its pipeline implementation when sampling rate is high. One of the useful derivatives of the LMS ADF for fast and computationally-efficient implementation of ADFs. Unlike the conventional LMS ADF, BLMS ADF accepts a block of input for computing a block of output and updates the weights using a block of errors in every training cycle. This results in a significant saving of LUT words and adders which constitute the major hardware components in DA-based computing structures [9].

II. EXISTING METHOD

The Least Mean Square (LMS) adaptive filter is the most popular and most widely used adaptive filter, not only because of its simplicity but also because of its satisfactory convergence performance [1], [2]. The direct-form LMS adaptive filter involves a long critical path due to an inner-product computation to obtain the filter output. The critical path is required to be reduced by pipelined implementation when it exceeds the desired sample period. Since the conventional LMS algorithm does not support pipelined implementation because of its recursive behaviour, it is modified to a form called the delayed LMS (DLMS) algorithm [3]–[5], which allows pipelined implementation of the filter.



Delayed LMS Filter

The modified DLMS algorithm decouples computations of the error-computation block and the weight-update block and allows us to perform optimal pipelining by feed forward cut-set retiming of both these sections separately to minimize the number of pipeline stages and adaptation delay. The proposed structure involved significantly less adaptation delay and provided significant saving of ADP and EDP compared to the existing structures. Adaptive filters are an important part of signal processing. Adaptive filters adjust its transfer function according to an optimizing algorithm. Due to the complexity of the optimizing algorithms, most adaptive filters are digital filters.

LMS Algorithm

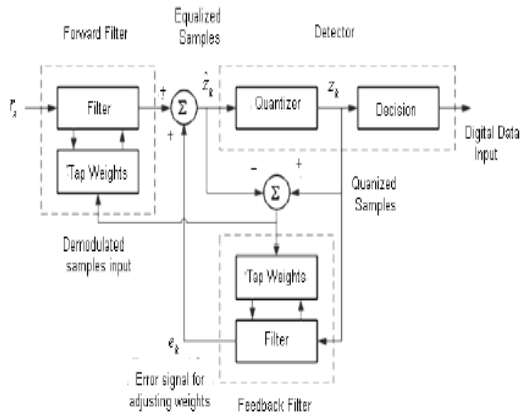
LMS adjusts the adaptive filter taps and modifying them by an amount proportional to the instantaneous estimate of the gradient of the error surface [6]. It neither requires correlation function calculation nor matrix inversions, which makes it simple and easier when compared to other algorithms.

III. PROPOSED METHOD

A. Adaptation Delay

The Adaptive algorithms are classified as Stochastic gradient algorithms and Exact least Square algorithms. Stochastic gradient algorithms include self

orthogonalizing algorithms as a subclass.



Adaptive Feedback Equalizer

The forward and feedback tap weights can be adjusted simultaneously to fulfil a criterion such as minimizing the MSE. The DFE structure is particularly useful for equalization of channels with severe amplitude distortion, and is also less sensitive to sampling phase offset. The improved performance comes about since the addition of the feedback filter allows more freedom in the selection of feed forward coefficients. The exact inverse of the channel response need not be synthesized in the feed forward filter, therefore excessive noise enhancement is avoided and sensitivity to sampler phase is decreased. The advantage of a DFE implementation is the feedback filter, which is additionally working to remove ISI, operates on noiseless quantized levels, and thus its output is free of channel noise. One drawback to the DFE structure surfaces when an incorrect decision is applied to the feedback filter. The DFE output reflects this error during the next few symbols as the incorrect decision propagates through the feedback filter. Under this condition, there is a greater likelihood for more incorrect decisions following the first one, producing a condition known as error propagation. On most channels of interest the error rate is low enough that the overall performance degradation is slight.Blind equalization of the transmission channel has drawn achieving equalization without the need of transmitting a training signal.

B. 2 – Tap Equalizer

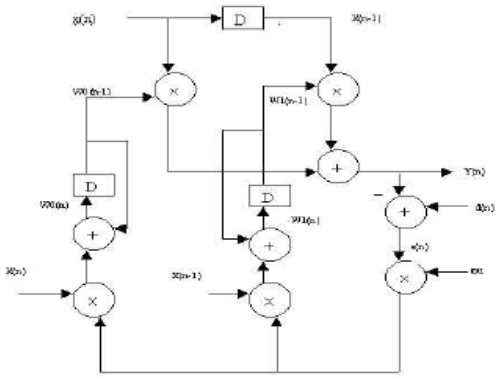


Fig Tap Filter

The multiplexer multiplexes between the filter tap weights and the error values. In other words ,when the multiplexer control bit is set to '1' ,the filtering operation is performed and when the control bit set to '0' , the weight update operation is performed .In this architecture ,multipliers are reused ,i.e.. multiplexed in time, for both filtering and adaptation.

IV. EXPERIMENTAL RESULTS

Existing Model:

Fixed Point Consideration:

The fixed-point representation of a binary number. a fixed-point representation of a binary number where *X* is the word length and *Xi* is the integer length. the hardware designer taking the design constraints, such as desired accuracy and hardware complexity, into consideration. Assuming *(L, Li)* and *(W,Wi)*, respectively, as the representations of input signals and filter weights, the word length of the weights should be increased at every iteration, which is not desirable. The assumption is valid since the weight increment terms are small when the weights are converged.

Steady-State Error Estimation

The MSE of output of the proposed DLMS adaptive filter due to the fixed-point quantization is analyzed. Based on the models introduced in the MSE of output in the steady state is derived in terms of parameters The MSE values are estimated from analytical expressions as well as from the simulation results by averaging over 50 experiments.

Proposed Circuit

To have low complexity architecture ,variants of LMS algorithm sign-data LMS,sign-error LMS and sign-sign LMS are considered. In sign-data LMS and sign-error LMS number of multiplications are reduced in updating operation. In sign-sign LMS no multiplications are required in updating operation.The updating equation is reduced to

$W(n+1)=W(n) + \mu.sign(X(n)).sign(e(n))$.

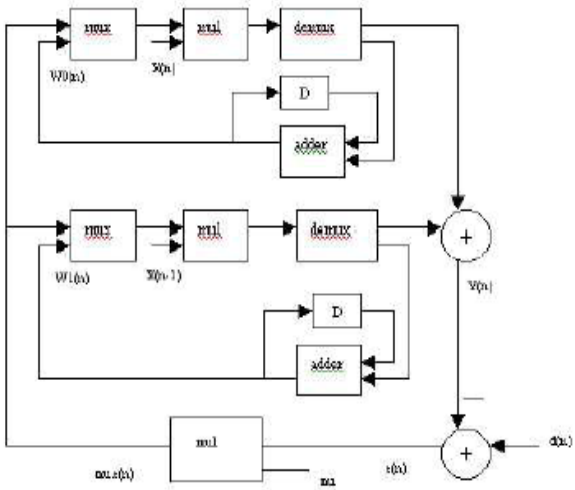
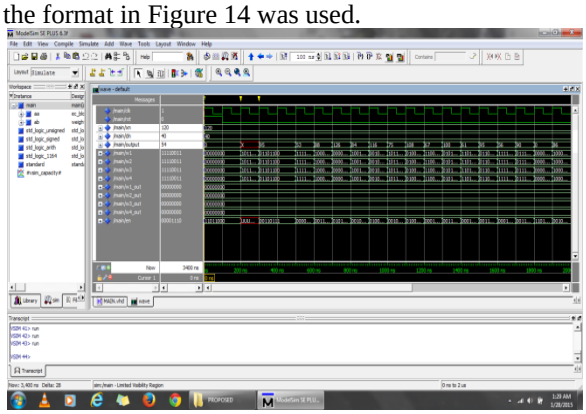


Fig .4 Conventional Circuit

In the above architecture ,each tap requires two multipliers for computing filter output and updating the filter weight. And one more common multiplier for m multiplication.

Floating Point Format Representation

The 18-bit floating point format was used in the design of architecture .This format was chosen to accommodate specific requirement: the dynamic range of the format needed to be quite large in order to represent very large and small, positive and negative real numbers accurately, Based on these requirements the format in Figure 14 was used.



V. CONCLUSION

The LMS algorithm and the variants of LMS algorithm sign-sign LMS, sign-error LMS and sign-data LMS are verified and their feasibility is tested for eleven tap adaptive equalizer. VHDL simulation of two tap adaptive equalizer is tested for LMS algorithm. Multiplexed multiplier architecture is proposed for LMS adaptive equalizer in order to reduce the number of multipliers . To reduce the hardware complexity and feedback latency still more ,sign-sign LMS algorithm can be used for VHDL simulation of adaptive channel equalizer which results in area and power savings. On the other hand the converging speed is low compared to normal LMS algorithm.

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