Design of a CMOS Multiplexer with Ultra Low Power using Current Mode Logic Technology

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Abstract

The current mode logic (CML) function is widely used for the process due to their lower output voltage slap linked to the static CMOS circuits and also used for very fast current switching and discrepancy pair of transistors. In this paper proposed a new method for planning Ultra Low Power and wide energetic series for multiplexing analog indicators. The method is purely designed for weak inversion region and also used for the(CML) circuit. The effective frequency and power consumption can be speckled by the bias current of the gates. The multiplexer strategy hires CMOS transistors are used for increasing the threshold voltage in the transmission gate signals. This schemereveals that the power dissipation is low and active range is high. The main applications of the data selector are signal multiplexing functions, data routing, digital signal converting, sign gating, and number system preparation.

Keywords: *current mode logic function, multiplexing analog signals, the transmission gate signals and data selector.*

I. INTRODUCTION

The dissemination of applications demanding digital indicator dispensation, comprising with digital audio and video presentations, has enlarged market concentration in high-speed high-determination assorted signal ICs, as well as ADC and DAC. The performance of this circuit that equally contains the analog and digital circuit allocations. The latter circuits mainly affected by the noise at the identical substrate. Undeniably, the source current spines through replacing, logic gates engender the power-supply changing noise that combines with the analog circuits over source positions and substrate connection, thus corrupting course determination. In specific, the outmoded CMOS inert logic creates an extraordinary volume of noise, and it is not appropriate for high-definition uses.

Thus the effort mainly improves the ability of sub-threshold source coupled logic (STSCL) for constructing analog circuits and schemes that track very low voltage and commitment to afford appealing performance with delicate energy reserves. For a long battery life, it affords very less energy reserves in fields like bio medical engineering. Further assembly the ultra-low power description, the scheme also be trustworthy and must gathering beneath severe situations. In this paper, STSCL are used to design and analyse the logic gates. They are used for execution of analog subsystems that would be operatedat very low source voltages and ingesta smaller amount of power. The switch discovers many uses in incorporated circuit scheme. In analog designs, the switch is engaged to appliance valuable ranges like multiplexing, variation and other solicitations. They are used as a transmission gate in digital tracks and enhance anaspect of elasticity as initiate inusual logic circuits.

The execution of Ultra Low Power Systems has demonstrated to somewhat revolved in many recent uses in many parts like mobile networks, sensor links and implantable biomedical process. Nowadays electronics industry had been increased Low power consumption. The Requirement for low power has produced a foremost model swing where power degeneracy has convert substantial deliberation in concert. CMOS switches have excessive features and its best significant method, a voltage-controlled resistor that deals very low resistance i.e. less than 95means ON state and very high resistance i.e. several hundred Mega ohms means OFF state with Pico-ampere leak currents. CMOS approach is well-suitedusing logic circuitry and incorporates large number of ICs. Its profligate switching features are well organized with lowest circuit leak. MOSFET transistors offer changing the positive and negative voltages and bearing positive and negative currents with identical comfort. Operation of high presentation systems particularly for low power requests produces many tasks and involves the interchange between speed of operation and power consumption.

II. CURRENT MODE LOGIC THRESHOLD

The rapid process in the CML gate is essentially high then the logic process mostly takes place in current field. An NMOS basis coupled differential pair transistors turns as an adjustment to direct the tail current Iss to one of the output subject on the input logic. While driving the CML gates, the

Load resistor R$_L$ is converted into output voltage. In case of switching, the input discrepancy pair of another phase the output voltage swipe (R$_L$ I$_{SS}$) must be sufficiently high. The channel source above effort voltage input pair must be superior toV$_{dssat}$when V$_{in}$ = 0. The load resistance RL is executed by improving the PMOS device in triode section and also NMOS exchanging network must be organised in a suitable way to attain preferred logic operation. The input logic level navigates the extremity bias current into one of the division of the charge coupled pair and this current is changed to voltage by the load resistance.
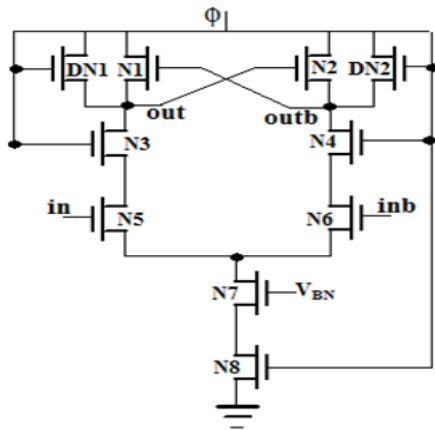

Fig.1:Current Mode Logic-Base Invertercircuit

Many compound logic functions can be executed by using a complex network of NMOS charge coupled pairs as converting part. The load resistance RL is realised by improving the PMOS device in triode section and also NMOS switching network must be organized in a correct way to accomplish preferred logic process. The input logic level directs the conclusion bias current into one of the division of the charge mode and this current is transformed to voltage by the load resistance. Functioning of sub threshold region, the device trans-conductance does not depend upon the devicesize but toughly depends on the temperature. Henceforth by varying the strategy limitations it is not likely to alter the transfer curve.

The voltage swipe and the current essential for charging and discharging the dependent capacitances is a smaller amount in SCL topology, when linked to the CMOS topology, the signal swipe is equal to VDD. The main lead in this topology is decrease in sign strike. Owing to create the extension bias current absolutely shifts to one of the two output divisions, the voltage swipe at the input and output of a logic circuit must be high. It would be sufficiently high to change absolutely the input differential pair of another stage. In a manner CML circuit has been used as a logic circuit with tolerable noise margin if its gain is satisfactorily high. The section of process of the NMOS devices contributes the least acceptable

voltage swing at the output of each CML gate. In the sub threshold expanse the mandatory voltage swing can be as low as 120 mV at room temperature. This is the sub threshold section rest on the sub threshold angle factor and is liberated to the threshold voltage of the NMOS switching devices. In sub threshold region, when the SCL gate is biased then the PMOS device is used as a load scheme. Subsequently all the campaigns are worked in sub threshold area the tail bias current can be compact till equivalent with escape currents in the circuit.

$$G_m - \frac{\partial I_{OUT}}{\partial V_{IN}} - \left(\frac{I_{SS}}{2n_n U_T} \right) \cdot \frac{1}{\cosh^2 \left(V_{IN}/(2n_n U_T) \right)}$$

III. BIASING EFFECT

The change in transistor threshold voltage can be determined by the difference between the voltage difference and the Transistors Source and the Bulk (VSB). Subsequently VSB possessions VT the bulk will be filed as second Gate which pretends to classify how the transistor turns ON and OFF. Biasing effect states that the change in the transistor threshold voltage (VT) resulting from a voltage difference between the transistor source and body. Since the voltage difference between the source and body disturbs the VT, the body would be assumed of as a second gate that assistance to regulate how the transistor turns ON and OFF. The strength of the biasing effect is typically computed by the body coefficient. Consequently fluctuating threshold voltage V$_{th}$ would be altered by changing VSB that can practice dynamic threshold voltage MOSFET(DTMOS).

Generally, the source and body junction is neither zero-biased nor reverse-biased. Forward-body-biased MOSFETs could be used on specific circuit to increase presentation with lower threshold voltage VTh . This model is operated in planning the power analog multiplexer. The transistors are functioned in strong inversion region of using 0.38 V forward body bias. Variations of biasing performances are allowed by strong body consequence and these methods are efficiently employed in elder generation. This bias effect will be applied superficially or internally. The interior tactic usually employs a charge pump circuit offer inverse body bias or potential divider to create forward body bias. Inverse body bias for n channel transistors upsurges the threshold voltage and creates the transistors both slow and less drip. On the other hand forward body bias decreases the threshold voltage creating the transistor fast and with extra leakage. The divergences of the body bias are opposite for P channel transistor.
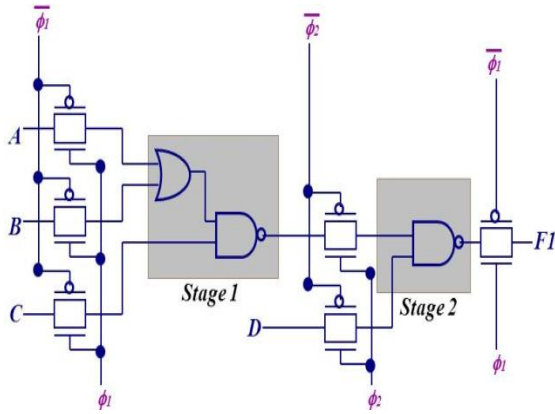
Fig.2: Transmission Gate with Biasing Effect

IV. DESIGN OF MUX

In the past years large number of multiplexers is designed by using the concept of a shift register. Shift registers are built by using synchronously triggered D-latches by connected external clock serially. Each S & H circuit latches are enabled by each D-latch. The major drawback of this system is clock feed-through to the output line. For every positive and negative clock edge, the clock cycle glitches occurred synchronously. This problem can be minimized by using the proposed multiplexer design.

In the place of locating the body bias at once either through design or at construction test, the Dynamic body bias alters the body bias various times while the chip is functioning. Dynamic body bias minimizes the temperature and aging effects and the very low power operation can be optimized by the power management modes. A logic '1' on indicates the gate of NMOS transistors will chance them ON and a flattering SELBR linked to the gate of PMOS transistors will change them ON and the useful signal is permitted to pass from IN to OUT. In addition while the SEL is at logic'0'and its flattering SELBR will change all the transistors OFF thus spoiling the signal from IN to OUT. The output will be required into a high-impedance state through the conversion period from ON to OFF where the junction capacitance will have been exciting to few millivolts.

To overcome this problem the PMOS transistor islinked as a pass transistor between the ground and the output node. On every occasion all the transistors are in OFF state then the PMOS transistor will be revolved ON, compelling the output capacitor to ejection to ground. By using this altered circuit for each stream an analog loss-less multiplexer with eight channels has been considered. Three binary control inputs are selected as channels. The obstruct input is used to Enable or Disable the mux. A low ON resistance of 25 ohms, high OFF resistance of 8Mohms,with very low leakage current about Pico amperes were attained with the analog transmission gate.

V. DESIGN OF DECODER

The circuit is replicated and evaluated by the minimal factors of the STSCL can be used to create a peak level output for the system. Formerly the multiplexers are deliberated using the model of shift registers that are constructed by synchronously triggered D flip flops with external clock. The main drawback of this system is the clock compete the output line and also mal functions occur for each positive and negative clock edge. This difficult has been decreased in the suggested multiplexer proposal. On behalf of the fixed body bias used when either through design or at fabrication the dynamic body bias can be used to change several times and also decreases the temperature and aging effects. The DBB underestimates the temperature and aging effects and also for enhancing very low power process the power management modes are consumed efficiently.
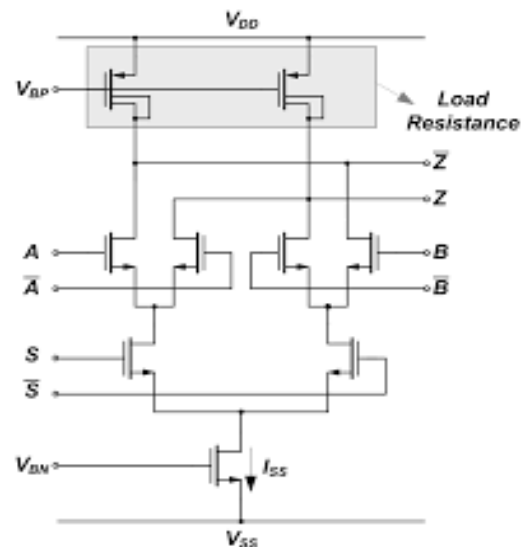

Fig.3: current Mode Logic AND Gate

The above figure shows the source coupled logic AND GATE. It has been developed by using CMOS and PMOS transistors and is purely defines the characteristics of the systems.

This AND gate is altered into SCL and gate and a 3to 8 decoder is executed using this SCL and gate. This is used to produce the select signals for each channel from two binary control inputs. The block diagram and the circuit diagram of the system is shown in fig. 4(a) & 4(b)
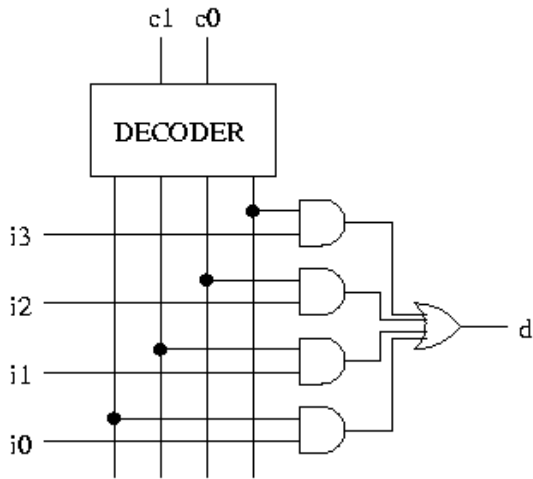
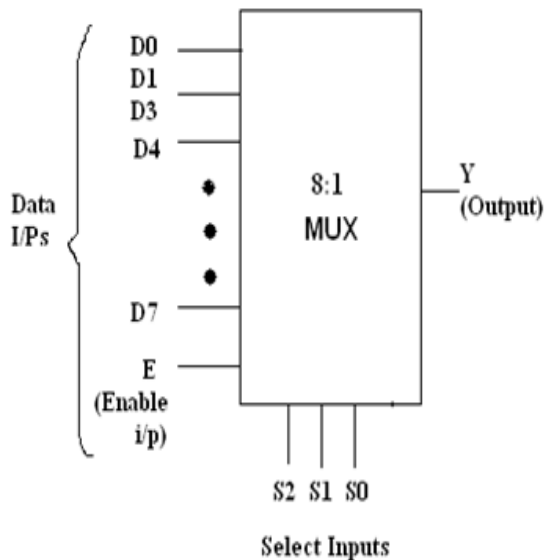**Fig. 4(a): Block Diagram of Mux With Decoder**

Fig. 4(b) Circuit Diagram of MUX

VI. RESULTS

Both NMOS and PMOS devices can be enabled by the use of the dynamic body bias which is provided by means of potential divider using poly resistors. The devices can be driven by the Inverter and Buffer outputs of the SCL gate. The system is confirmed with input signals with altered amplitudes and frequency. The PMOS transistor is ON only when the logic is 0.The NMOS transistor is turned ON only when the complementary Logic 1 is applied that allows the signal to pass from IN to OUT. While the signalgoes to Logic 1, all transistors are revolved OFF delaying the input signal. Throughout the transition period from ON to OFF the output will be enforced into a high-impedance state wherever the junction capacitance will be accused too few millivolts.

To eliminate this disadvantage, a PMOS transistor is cast-off between the output node and ground as a pass transistor. As soon as all the transistors are in OFF state, the PMOS transistor turns ON imposing the output capacitor to release to ground.The scheme is pretended by relating sinusoidal input of 1µV amplitude and the frequency is varied from 1Hz ahead of 1kHz.The total current drained by the circuit is about 1.95 µA causing in the total power ingestion of 0.75 µW. The response of the system is shown in fig.5(a),(b),(c). As the frequency of the input signal is improved the power dissipation also better.
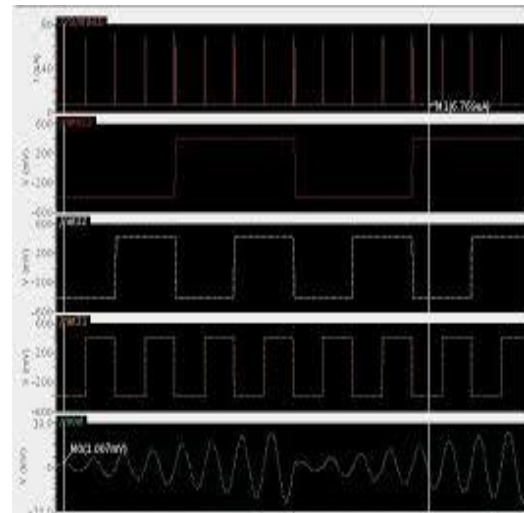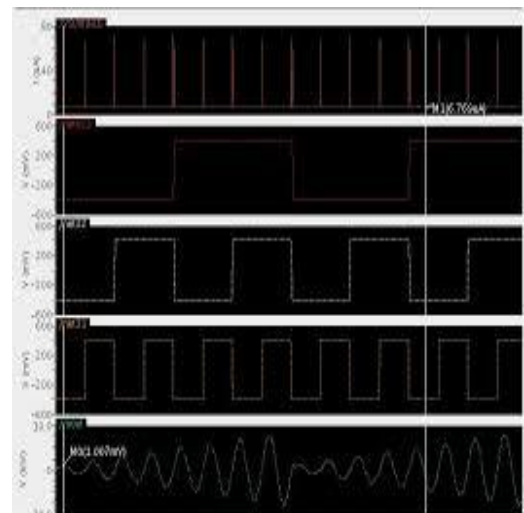

Fig.5(a)Simulated Output of1µV/1KHzsine Wave
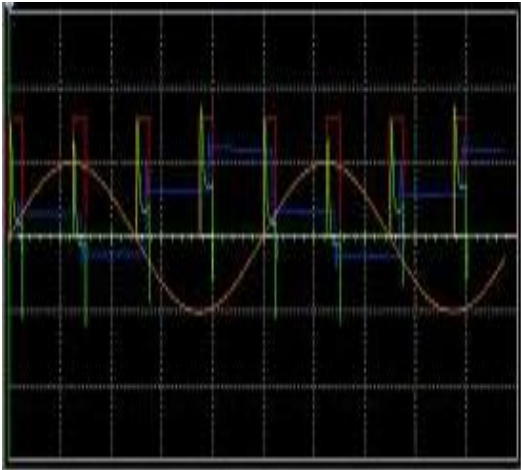

Fig.5(b)Simulated Output of10µV/1KHzsine Wave

Fig.5(c)Simulated Output of 10µV/10KHz Sine Wave

VII.CONCLUSIONS

A low power comprehensive series current mode logic circuits functioned in sub threshold state for swapping analog indications is executed in 175nm knowledge. The essential output voltage swipe for appropriate logic process is delivered by consuming high resistancePMOS load strategies. Transmission gate system was used to switch analog signals with amplitude extending from 0.99µV ahead. The ON and OFF resistance of the gate attained was 28 ohms and 10M ohms respectively. The total power degenerated at a swapping frequency of 10 KHz is about 0.78µW. The STSCL circuit was used to apply 8channel multiplexer for obtaining biomedical signals and the power dissipated was stately as 0.78µW. The number of stations to be multiplexed can be improved further with appropriate extra circuitry.

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