Analysis and Optimization of a Floating Point Representation of a Complex Numbers using FPGA

Dr.A.Nitesh, J.Deveesh
Associate Professors, M.Tech. Department of VLSI Design,
G D Goenka School of Engineering, Haryana

Abstract

This paper proposes the comprehensive processor hardware with the complex floating points. Thus the system performs the different types of arithmetic and logic operations in the 32-bit integer. The floating point representation is defined in the IEEE 754 standard. The arithmetic unit is categorized into 3 types: 32-bit integer arithmetic operations,32-bit floating point numbers, and complex numbers. These units can be accomplished by the arithmetic operations such as addition, subtraction, multiplication. The particular progression in this system is the innovative architecture bring together for complex arithmetic unit. However using such hardware consequences are to compromise among accuracy and number of bits used to indicate the fixed point equal of floating point numbers. The recommended architecture elevates that compromise and it is executed with less number of look-up tables to apart from 5500 logic gates. The instruction set is particularly considered to maintain integer, floating point and complex floating point arithmetic operations. Thus the proposed system enumerates the difficulties which are the complex that are recognised by the past systems.

Keyword: *complex floating points, arithmetic and logic operations, IEEE 754 standard, complex arithmetic unit, instruction set.*

I. INTRODUCTION

Nowadays the design of the processor is very simple and adaptive to all technologies. There are wide range of architecture with processed instruction sets are available. The proposed system describes the architecture with optimized instruction set. The phenomenon comprises capable complex floating point so that accomplish the working out the complex numbers with high amount of the precision. Hence this processor could be able to import as a coprocessor to part the assignment on the main processor in the solicitations wherever demanding calculations are desired. Commonly floating point demonstration is applied in digital signal processing presentations. Nevertheless many times stationary point processors will content the necessities. If anyone select the floating point architectures if they need high accuracy and vigorous series. A number of important features need to be deliberated however choosing this architecture. The projected architecture can also be known as hybrid architecture meanwhile it contains of floating point units like DSP processors, but it does not comprise of any instruction level parallelism, and any particular or committed hardware units, and also does not includes of hardware encompassing appliances. But it has capacity and stock architecture parallel to many DSPs.

The processor present in the system can be able to work out the basic mathematical operations such as addition, subtraction, multiplication, division, as well as square root of the numbers. This well-known architecture is constantly differing from the previous proposed one and it also needs a less amount of look-up tables. Though DSP processors are used in fixed to floating and floating to fixed conversions that will maintenance a less self-motivated series and less precision in order to negotiation with the number of bits cast-off to characterize a fixed point equal of floating point matching part whereas floating to fixed conversion. If a fewer number of bits are used to denote fixed- point correspondent of floating point numbers, apparently about will be a concession for precision. In order to avoid that difficulty and to accomplish a smaller quantity number of look-up tables, it is superior to pick out the projected architecture that can openly implement arithmetic operations on the complex numbers.

Specific mechanisms also strained to achieve complex arithmetic by means of supply allotment and pipelining ideas, by using a single adder and floating multiplier for handling of both real and imaginary portions to develop a typical DSP standard alike accessible FIR filter. Numerous architectures have been technologically advanced for floating point arithmetic that was determined to diminish dormancy. However the key subject of this effort is executing a competent processor which can be processed integer and floating point numbers, as well as complex numbers. Furthermost of the strategy disputes are consuming nearby resemblances with the DSP processor scheme concerns. The formerly described segments are only concentrates on the portion of the processor and do not take care of the

results. But the proposed system should take response on the necessary concerns and rectify the problems.

II. DESIGN AND IMPLEMENTATION OF A PROCESSOR

The usual segments to create any processor are data path and control path. The hardware which is used to execute arithmetic and logic operations on data is the data path. The hardware that is used to control the structure of activities to be achieved by data path, by distributing certain control indications will come below control path. Numerous approaches are used to project control path. Specific of the public procedures are using FSMs or using micro-coded programming. To select the instruction set is the main strategy dispute that will agree the interconnections amongst all segments. Pick out the op-code length will also be the peculiar aspect. The current effort uses 32-bit op-codes. Selecting the suitable size of on-chip remembrances will develop the memory retrieving speed but one should preserve area restrictions in mind. However FPGA sellers are providing augmented embedded memories that can be used very straightforwardly.

The current processor comprising of 8KB on-chip RAM and is extendable up to 64KB. This accelerates the use of the processor for speed and real time requests. The register bank consists of 32 registers each of 32-bit extensive and the two operators can be drawn instantaneously. The bus multiplexer accomplishes the data flow among register bank and arithmetic units, by adding the buses that confine organized by controller. The single precision floating point arithmetic unit is considered founded on predictable algorithms related to other floating point processors. The floating point unit, that is main influence of this effort, uses a new phenomenon and is termed in the following sub-sections.

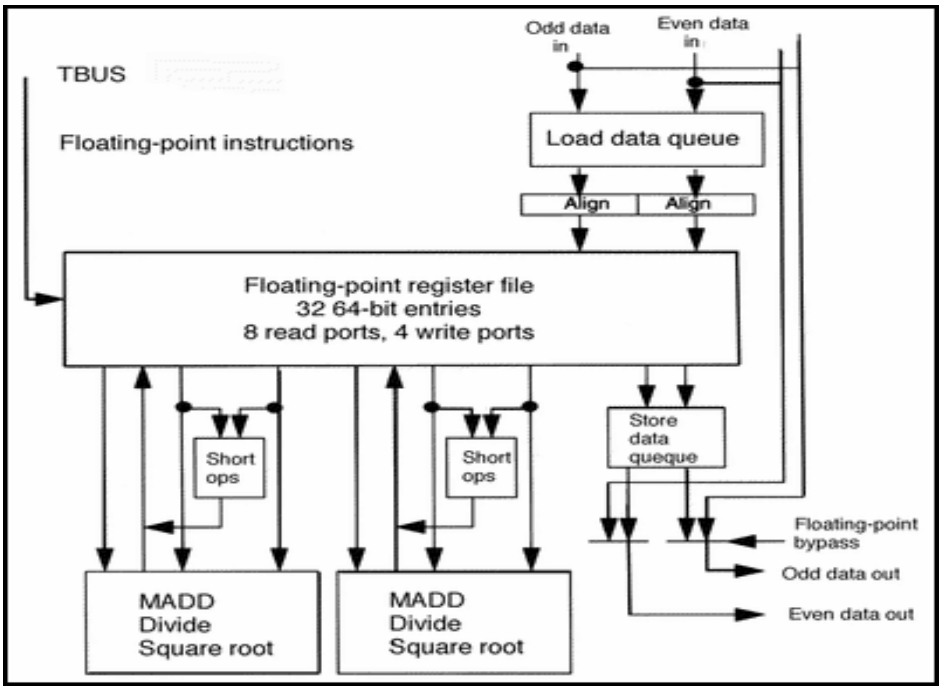

Fig.1: Block Diagram of Floating Point Processor

A. Data Route

The Data route contains of integer arithmetic unit and a single precision arithmetic unit and complex unit. A number of proposal concerns essential to be measured however planning complex arithmetic unit. Complex numbers addition consequences another complex number and is accomplished by the hardware whose architecture. The pre-normalization for addition/ subtraction unit, orders the existence of not a numbers in the inputs and supports the proponents of the operands assumed to the add/sub unit thataccomplishes addition/ subtraction on segmentfragmentssubject on the signal bits of the operands and genuine process that is projected to implement. Lastly the post-normalization unit instructs whether the outcome is a valid IEEE floating point number or not. If the consequence is close to a effective floating point number then it is smoothed according to the rounding mode designated.

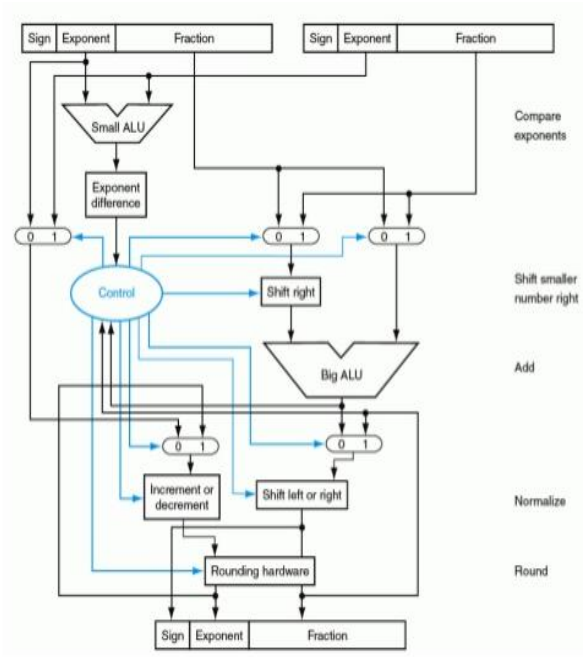

Fig.2: Floating Point Addition Architecture

The purpose of pre-normalization for multiplication is to form for NaNs in the inputs and totalling the essential proponents. To accomplish the product of real parts the pre-normalization unit adds the proponents. The multiplication unit then multiplies the numbers or division fragments of the two operands. The consequence of multiplication of portions will be of 21-bit. Hence the post-normalization unit will abbreviate it and then sequences the product affording to the rounding mode selected, and as a final point packs the signal, proponent, and mantissa bits of the end result of multiplication of operands.

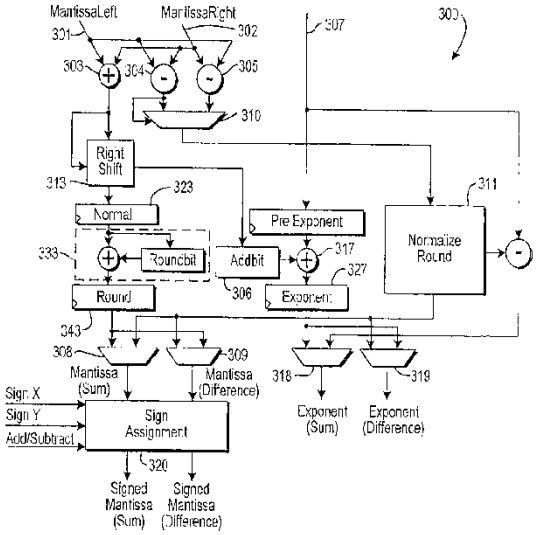

Fig.3: Floating Point Multiplication Architecture

B. Design of a Route

The control route of a processor comprises of a decoder that precedes the op-codes from memory and decrypts them and creates the essential switch signs which will assist the corresponding segments of data route to accomplish the essential deed. The addressing modes will stipulate the causes of operands on which the procedure is to be accomplished. The causes of operands for ALUs are also designated by the decoder. There may be numerous decoders in the processors which sustenance instruction level parallelism like VLIW architectures. Specific additional hardware will also be used to escape addictions in such architectures.

Op-code mapping is one of the most important experiments after the instruction collection. The performance and well-organized utilization of the hardware are decided by those two responsibilities. Then the Competent compiler strategy assignment will exclusively be firm by on suspicious assortment of instruction set and bench marking and op-code planning stages. The proposed design provisions two level pipelining. The control unit precedes the 32-bit op-code from the memory that are fetching from the instruction. The op-code is then work out for creating numerous control signals to various segments. If the operands are extant in registers and the outcome is to be deposited in the register then the control unit produces source register index, target register index, destination register indexes to choice the corresponding registers from the register bank.

C. Single Floating Point Unit

The single floating point arithmetic unit is executed addition, subtraction, multiplication, division and square root operations on the specified 32-bit floating point operands. They are created on the control signals known by the decoder and offer the consequence again in the single floating point format.

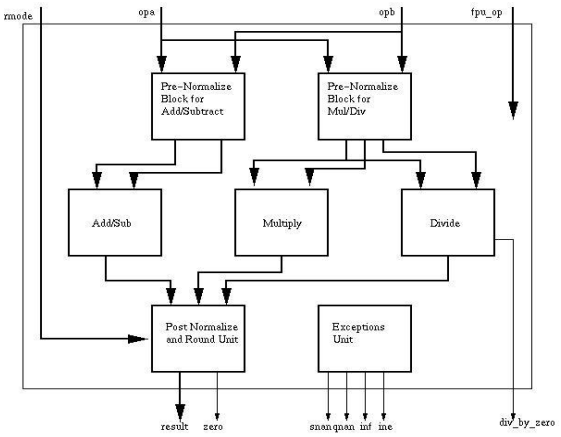

Fig.4: Single Floating Point Arithmetic Unit

III. SIMULATION RESULTS

The section defines the simulation results of the main components of the design like decoder and floating point arithmetic units. The signal requires the procedure to be accomplished on the given complex numbers whether addition or subtraction or multiplication, that is connected to the decoder. The complex numbers are specified in 16-bit floating point format. The amount produced of this segment consists of real and imaginary parts that are in 16-bit floating point format and the exclusion signals.

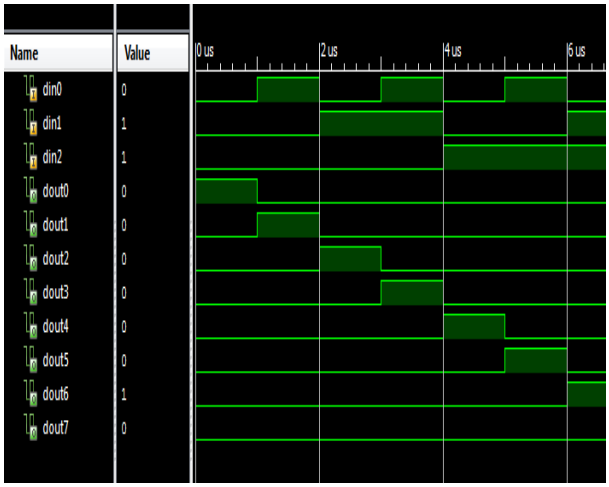

Fig.5: Decoder Simulation Results

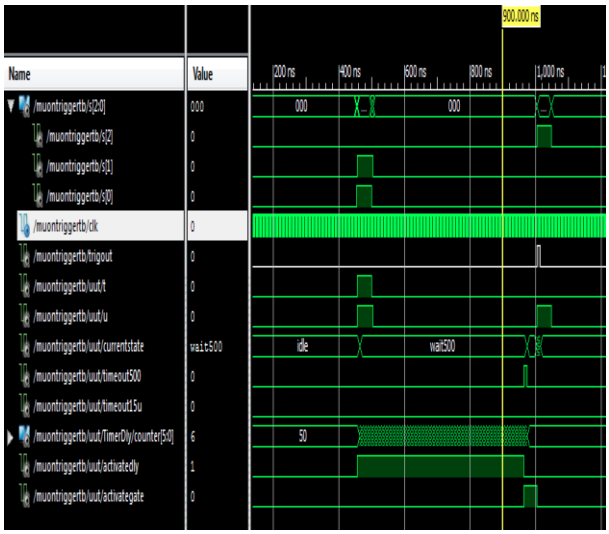

Fig.6: Floating Point Addition Simulation Result

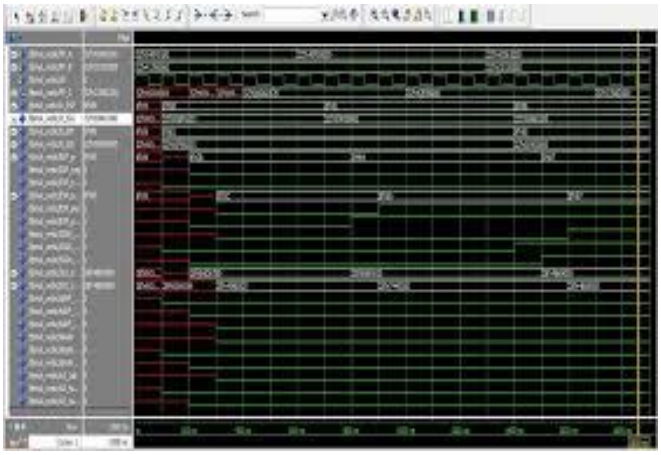

Fig.6: Floating Point Multiplication Simulation Result

IV. CONCLUSION

The work offers a widespread range of processor hardware which comprises three arithmetic units. It can be able to precede integer data and 32-bit floating point data along with complex data that is denoted using subset of IEEE 754 floating point format. The design of complex floating point arithmetic unit offered here is a absolutely innovative architecture that will elude the concession of using limited number of bits to denote fixed point equivalent of floating point numbers and there by partial dynamic range. The processor offered here can uses in real time presentations and also can be used as a co-processor along with a main processor.

V. FUTURE WORK

A resourceful compiler can be established for this processor. This processor is also used as a coprocessor in the execution of numerous DSP bench mark algorithms which require complex computations. Particular additional modules can be encompassed to still develop the progressive structures and to progress the widespread system on similar platform. The equivalent structural design can be applied for the complex numbers that are characterised using other floating point formats.

REFERENCES

[1] A.Beaumont Smith, N.Burgess, S.Lefrere, and C.C.Lim,"Reduced latency IEEE floating-point standard ladder architectures," inProc. IEEE Symp. Comput. Arithmetic, 1999, pp. 35–42.

[2] P. S. Paolucci, "Complex Domain Floating Point VLIW DSP with Data/Program Bus Multiplexer and Microprocessor Interface," U.S. Patent 7 437 540, Oct. 14, 2008.

[3] Dake Liu "Embedded DSP Processor Design" application specific instruction set processors, ELSEVIER.

[4] S. Katayanagi, "Complex Vector Operation Processor with Pipeline Processing Function and System Using the Same," U.S. Patent 20030009502, Jan. 9, 2003.

[5] C. Inacio and D. Ombres, "The DSP decision: Fixed point or floating?," IEEE Spectrum, vol. 33, no.9, pp. 72–74, Sep. 1996.

[6] IEEE Standard for Floating-Point Arithmetic, IEEE Std 754-2008, Aug. 29, 2008, pp. 1–58.

[7] Allison L. Walters, "A Scalable FIR Filter Implementation Using 32-bit Floating-Point Complex Arithmetic on a FPGA Based Custom Computing Platform," M.S. thesis, Dept. Electrical. Eng., Virginia, 1998.

[8] R. G. Cox, M. W. Yeager, and L. L. Flake, "Single Chip Complex Floating Point NumericProcessor," U.S. Patent 4996661, Feb. 26, 1991.

[9] Nadav Cohen and ShlomoWeiss,"Complex Floating Point—A Novel Data Word Representation for DSP Processors" IEEE transactions on circuits and systems—I, VOL.59, no.10, pp.2252-2262 , oct2012.

[10] Mazen A. R. Saghir "Application Specific Instruction-set architectures for embedded DSP Applications" Ph.D thesis, Dept., of electrical and computer engineering, university of Toronto,
canada.