An Enhanced Fault Tolerant System in the Design of ALU using TMR Technique

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Abstract

Nowadays, the technology has been emerged at a peak on Nano dimension in the significant fields of industrial sectors. Meanwhile, the manufacturing process of the concerned system is much unreliable which would directly impact the production. Reliability is one of the significant aspects that have to be evaluated during the planning segment of any Integrated Circuits. Some of the most important applications like Medical and Military field, reliability plays a very crucial part in defining the recognition of product. Attachment of distinct elements in the main proposal for consistency improvement will give substantial quantity of area & power drawback. Consequently, fault tolerant approaches are suitably progressively essential, mainly in safety issues applications. Hence, a unique method is used to invent new ways for reclaiming the previously offered constituents in digital system. According to the system, ALU is a functional block of the central processing unit of a computer. So, it is vital that the system need to be fault free or fault tolerant. With the purpose of having high consistency and high accessibility of the system, used the standard Triple Modular Redundancy technique. This system is customarily used for defending digital logic from the single event upset by triplication the acute modules of the structure to give fault tolerance to system. The main concern of this paper is to attain less power consumption with high consistency while using any new methodologies to design the system.

Keywords: *Fault tolerance, Triple Modular Redundancy technique, Reliability.*

I. INTRODUCTION

From the past decades, the strategic plan of hardware systems has grown into strangely problematical, while the role and significance of the system has improved tremendously. This improvement results in level of integration in the development circuits from small to very large scale, the reliability for the concerned function has sustained its intense progress. The Consistency is responsible in defining the principal representative assets of the devices .Precarious applications claim the improvement of method such that the strategy is more trustworthy and error resilient. Analyzing and authentication is the primary step to improve the consistency of the considered system. It is not abundant to enrich the reliability of the system; the tolerance of the fault which happens in the device setup should be inherent in the design. Along with fault tolerance, fault recovery method also should be integrated in the design .Entirely these finally give a way to the design with the absolutely consistent, fault tolerant and less error system. As a result of the claim for boosted functionality, the complication of systems increased that increase the possibility of failure of system. Moreover, our requirement on calculating systems has developed so great that it becomes intolerable to reoccurrence to less experienced mechanisms. After analyzing all the critical applications, it is mandatory need to improve techniques which will produce a design more consistent and fault resilient. Furthermore, just fault tolerance is not adequate without combining the fault recovery methods in the design, for creating it entirely trustworthy and minimization of fault within the system. A high consistency and unremitting processes in systems are essential in definite applications such as space technology, aeronautical engineering techniques, nuclear power plants, and chemical industries. Failures or erroneous system of any equipment's or constituents in any such application indicates to terrible effects. Therefore, the main concern of this paper is to have great reliable system.

II. LITERATURE REVIEW

Tian Ban et.al (2010) "A simple fault-tolerant digital voter circuit in TMR Nano architectures" [1] proposed the Nano electronic systems are now more and more prone to faults and defects, permanent or transient. Redundancy techniques are implemented widely to increase the reliability, especially the TMR — Triple Modular Redundancy. However, many researchers assume that the voter is perfect and this may not be true. This paper proposes a simple but effective fault-tolerant voter circuit which is more reliable and less expensive. Experimental results demonstrate its improvement over the former TMR structures.

AyonMajumdar et.al (2012) "Fault Tolerant ALU System" [2] presented the design of fault tolerant ALU system by using Triple Modular Redundancy. ALU is a critical component of microprocessor and is the core component of central processing unit. Therefore, it is necessary for making

the ALU to be fault tolerant. The use of voting logic and disagreement detector has been implied in making the ALU system to be fault tolerant. The source code for the following was developed in Verilog HDL. The software used was Xilinx ISE.

R. V. Kshirsagar (2008) et.al "A novel fault tolerant design and an algorithm for tolerating faults in digital circuits" [3] explained a novel fault tolerant algorithm for tolerating stuck-at-faults in digital circuits. We consider in this paper single stuck-at type faults, occurring either at a gate input or at a gate output. A stuck-at-fault may adversely effect on the functionality of the user implemented design. A novel fault tolerant design based on hardware redundancy (replication) is presented here for single fault model to tolerate transient as well as permanent faults. The proposed design approach scales well to larger digital circuits also and does not require fault detection. We have also presented and compared the results of triple modular redundancy (TMR) method with our technique. All possible faults are tested by injecting the faults using a multiplexer.

D. A. Tran et.al "A Hybrid Fault Tolerant Architecture for Robustness Improvement of Digital Circuits" [4] describeda novel hybrid fault tolerant architecture for digital circuits is proposed in order to enable the use of future CMOS technology nodes. It consumes less power than the classical Triple Modular Redundancy (TMR) approaches while utilizing comparable silicon area. It overcomes many permanent faults occurring throughout manufacturing while still tolerating soft errors introduced by particle strikes. The technique combines different types of redundancy: information redundancy for error detection, temporal redundancy for soft error correction and hardware redundancy for hard error tolerance.

Z. Stamenkovic et.al (2016) proposed "A comprehensive approach to fault tolerance: Device, circuit, and system techniques" [5]. In this work, the huge research efforts and respectable scientific achievements, there are still challenges regarding the use of commercial ASIC technologies in space and safety-critical applications. This work presents a design methodology for fault-tolerant ASIC that is based on radiation-hard technology, redundant circuits with latch up protection, additional implementation steps during logic synthesis and layout generation, and power gating. Enhancements have been made within the standard ASIC design flow in order to incorporate redundancy and power-switch cells and, consequently, enable protection against single-event upset (SEU), single-event transient (SET), and single-event latch up (SEL). In order to validate the proposed fault-tolerant circuits, a fault-injection environment including fault models has been developed.

III. FAULT TOLERANCE SYSTEM

Fault tolerance is the asset that empowers a system to endure functioning in the occurrence of the failure of some of its components. It is mainly required after in high accessibility systems. If this method capable to remain its standard process even after weakening of one or more of its constituents, then this property of the system is called fault tolerance. The working excellence is proportional to the cruelty of the failure i.e. working excellence decreases as the crucial effect of the failure rises for simply intended systems. Fault tolerance comes to be significant design principles for the applications where the reliability of hardware is critical. Medicinal, military and future tasks are the defended applications that the fault tolerance of hardware turns out to be a significant concern. These systems are a method of concurrent systems even if a certain part of a system losses; it doesn't disturb the normal process of that system. Hence, there are three types of faults are categorized in this process. They are permanent fault, recurrent fault, and temporary fault. Permanent faults are continuous and can be initiated by physical impairment or design errors. Recurrent faults take place intermittently and usually result from unsecured device action. Temporary fault frequently triggered by outside troubles, occurs for a finite length of time and is non-recurring. The unit of standard operation depends on the amount or severity of the fault. In other words, the common operation turns out to be more and more serious with the growing of severity of the fault.

IV. PROPOSED SYSTEM

With the purpose of enduring the industrial faults, deliberate hardware redundancy. Triple Modular Redundancy (TMR) is frequently used for planning reliable systems to confirm high reliability, obtain ability and data reliability. It has been broadly used as a structural block of fault tolerant of the systems. A TMR unit comprises of three calculating units and a voter. Those units perform the same calculation in similar and their outcomes are applied to the voter. If any one of the three units miscarries, the other two units can exact and cover the error. With the disappointment of voter system, the whole system can ruin. Nevertheless, in a noble system, the voter is much more consistent than other TMR constituents. The voting logic associates the outputs of all the units pass the common output i.e. if all three outputs are same then it develops the final output and if two out of three outputs are similar then the two same outputs turn out to be the final output. Also, if the two same outputs are erred output then it will become the final output.

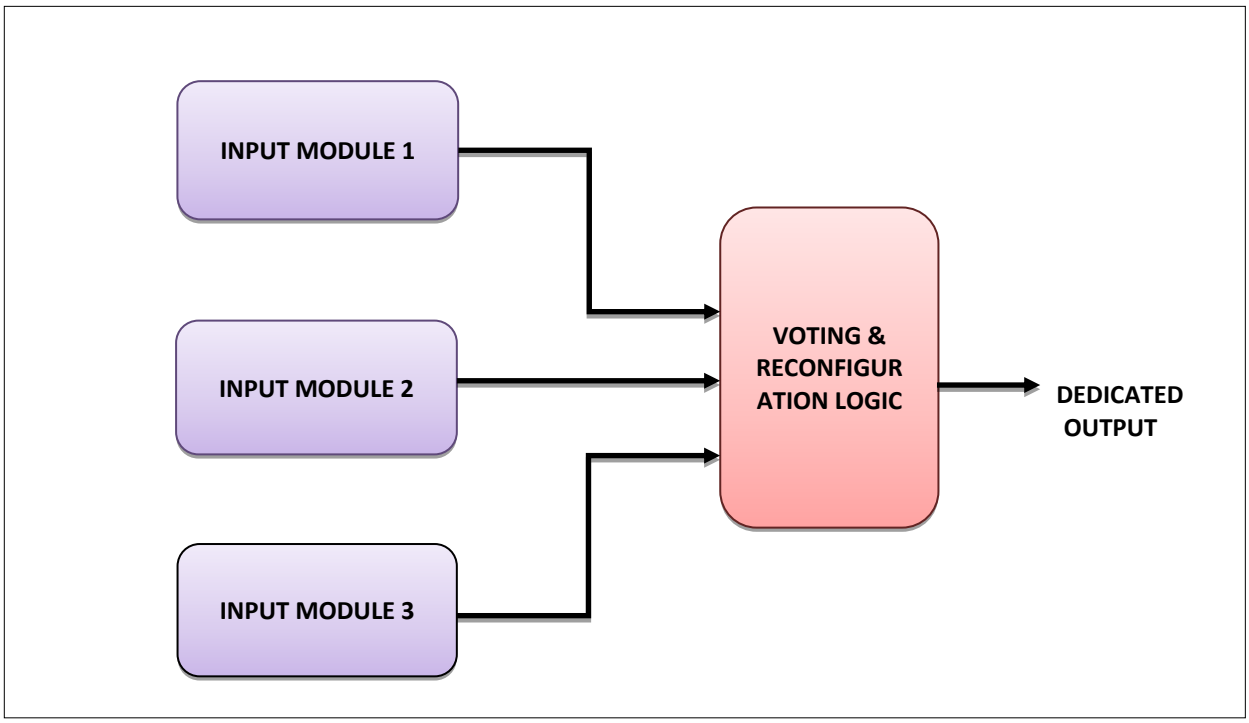

Fig.1: A Single Fault Tolerant System Based Triple Modular Redundancy

A. Fault Tolerance In Arithmetic And Logic Unit

Arithmetic Logic Unit (ALU) is the most significant role in any of the microprocessor or microcontroller. It is also the core and soul of any central processing unit (CPU). ALU implements logic operations, such as AND, NOT, OR etc., and arithmetic operations. An ALU heaps data from input registers, performs the operation and stores the consequence into output registers. The design and function of an ALU may vary between different processors. Some ALUs only accomplish integer calculations, while others are considered to take up the floating-point processes. Irrespective of the system unit is considered; its principal job is to provoke integer operations. Consequently, a computer's numerical performance is secured openly to treating speed of ALU. It can accomplish the resulting operations such as Integer arithmetic operations, bitwise logic operations and bit-shifting operations. Triple modular redundancy has been demonstrated so as to plan the fault tolerant of the ALU system. In this method, the ALU system approved out is triplicate, each consuming the same input, thus creating it triple mode redundant. The output of all the three ALUs is distributed onto the Voting Circuit which compares the outputs and then permits the majority output.

The fault tolerance system of ALU circuit is shown above. Arithmetic and logical unit (ALU) is a digital circuit that is divided into two distinct parts, the AU (arithmetic unit) and the LU (logical unit). The AU performs the arithmetic operations such as Add, Subtract, Multiply etc. and the LU performs the logical operations such as AND, OR, NOR etc. ALUs are designed to perform integer calculations. The ALU is a fundamental building block of the central processing unit of a computer.

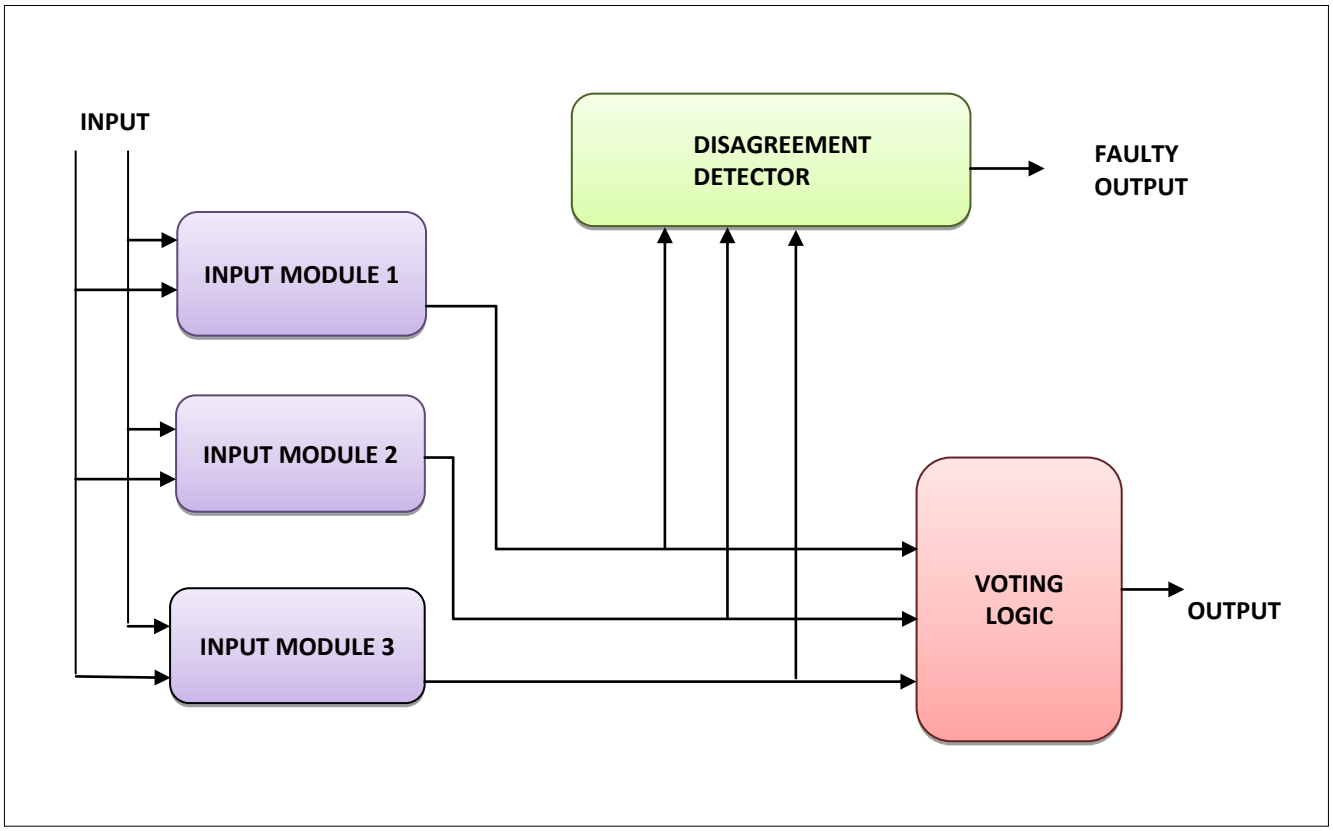

Fig.2. Fault Tolerant of Arithmetic and Logic Unit System

B. Voting Logic Function

In voting logic, the majority function is a function from *n* inputs to one output. The value of the operation is false when *n*/2 or more arguments are false, and true otherwise. It will permit the voting of correct output value in the occurrence of faults. The voting logic design is given in fig.3. Suppose we have three inputs A, B and C and we have to calculate the majority output out of three. Than we can find out it by the Boolean expression:

OUTPUT= AB+AC+BC

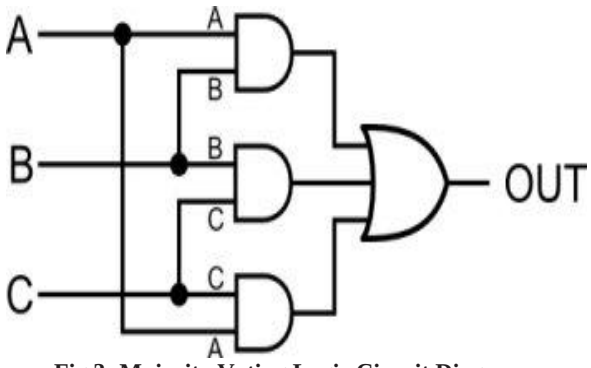

Fig.3: Majority Voting Logic Circuit Diagram

C. Disagreement Detector Circuit

In triple modular redundancy, it is also significant to detect the fault portion. Disagreement detector is used to detect the fault portion of the system. In this system, used AND OR operation method to implement the system. Disagreement detector has three inputs and three outputs. Different outputs give different type of information that it describes in table 1. It is designed by using the logic circuits of XNOR gate. We know that for a XNOR gate if inputs are different than it gives a low output and if inputs are same than it give high output.

$$A= \bar{X}\,Y + \bar{Y}\,X$$
$$B= \bar{Y}\,Z + \bar{Z}\,Y$$
$$C=\bar{Z}\,X + \bar{X}\,Z$$

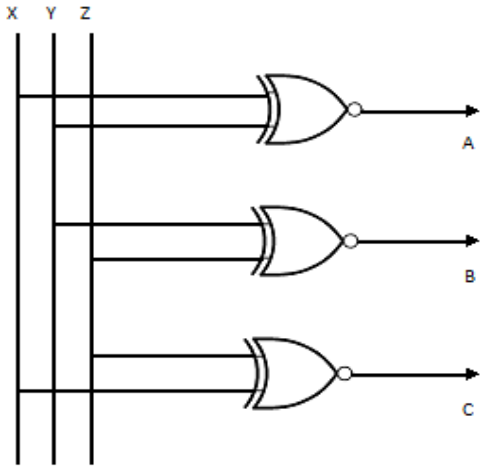

Fig.5. Disagreement Detector Circuit

Table.1. Disagreement Detector Outputs

A	B	C	Output	Output
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	0

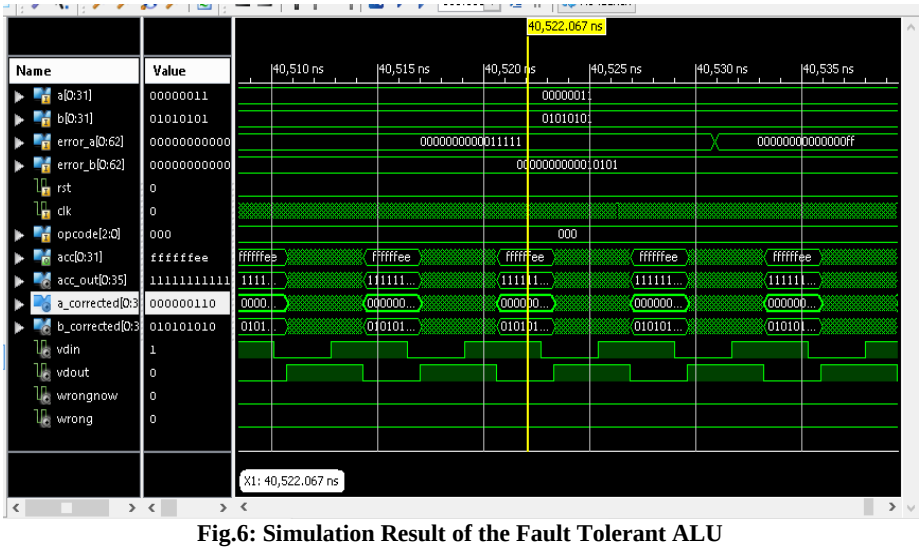

Fig.6: Simulation Result of the Fault Tolerant ALU

V. SIMULATION RESULTS AND ANALYSIS

In the course of the common process, 3 ALUs are functioning in the fundamental part of the system. Once the 3 ALU's are unsuccessful, the Critical ALU comes into effect in the proposed method for the altered ALU takes over the work. This type of practice is come into effect in the most recent system in the current research work. For this technique, there are three methods for amending the mechanism for the Critical ALU to confirm the accuracy of the ALU results. Awide-ranging simulation for 32 bit ALU operation has been shown below.

VI. CONCLUSION

In the world of nanotechnology, highly reliable and low power consumption is the fundamental need of the system. By considering this essential phenomenon, able to contribute a fault tolerant ALU system with the help of the most sensitive to faulty instructions called disagreement detector circuit and the assistance of triple modular redundancy technique. But in the real world, there is no system is cent percent fault free. Therefore the proposed ALU system also has some drawback of negligible fault tolerant and it can be improved by changing the faulty unit and make the system consistent. This proposal can be used in the applications of computing systems that are mainly used in the fields such as medical, industrial and space technologies. It has been used in such precious

field because of its accuracy, reliability and non-faulty output.

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