An Effective Implementation of SOL's Technique for Power and Coding Efficient VLSI Architecture in DSRC Applications

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Abstract

An implementation of similarity oriented logic simplification (SOLS) technique is proposed in this project for effective utilization of VLSI architecture by overcoming the limitations that are encountered in FMO and Manchester codes. FMO codes and Manchester codes are widely used in Dedicated Short Range Communication (DSRC) applications. These codes are adapted to accomplish dc-balance and also to enhance the reliability of the signals. FMO and Manchester codes have number of components which limits the potential to design a fully reused VLSI architecture for both. The Dedicated Short Range Communication (DSRC) is an emerging technique; it is employed in one way or two way short ranges to medium range wireless communication purpose. DSRC is vital in many real time applications such as safety application commercial vehicle application emergency warning system for vehicle and intersection collision avoidance etc. With the use of proposed SOL'S technique 100% hardware utilization rate was attained for both FM0 and Manchester encodings. The power consumption, operation frequencies and core circuit area utilizations will be improved to a greater extent when compared with the existing works. Performance evaluation will be carried out on post layout stimulation in Taiwan Semiconductor Manufacturing Company (TSMC) 0.18-µm 1P6M CMOS technology. This projects not only makes use of VLSI architecture effectively, but it also show cases the efficient performance of the proposed techniques at reduced cost. This system also and supports the DSRC standards of many leading nations.

Keywords: - *Dedicated short-range communication (DSRC), FM0, Manchester, VLSI.*

I. INTRODUCTION

Manchester coding technique is a digital coding technique in which all the bits of the binary data are arranged in a particular sequence. Here a bit '1' is represented by transmitting a high voltage for half duration of the input signal and for the next halftime period an inverted signal will be send. When transmitting '0' in Manchester format, for the first half cycle a low voltage will send, and for the next half cycle a high voltage is send. The advantage of Manchester coding is that, when sending a data having continuous high signals or continuous low signal (e.g.: 11110000), it is difficult to calculate the number of 1 S and Os in the data. Because there is no transition from low to high or high to low for a particular time period (Here it is 4 x T, T is the time duration for a single pulse). The detection is possible only by calculating the time duration of the signal. But when we code this signal in Manchester format there will always be a transition from high to low or low to high for each bit. Thus for a receiver it is easier to detect the data in Manchester format and also the probability for occurrence of an error is very low in Manchester format and it is a universally accepted digital encoding technique. The dedicated short range communication is a protocol for one or two way medium range communication. The DSRC can be briefly classified into two categories:

Automobile to automobile and automobile-to roadside. In automobile-to-automobile, the DSRC enables the message sending and broadcasting among automobile.

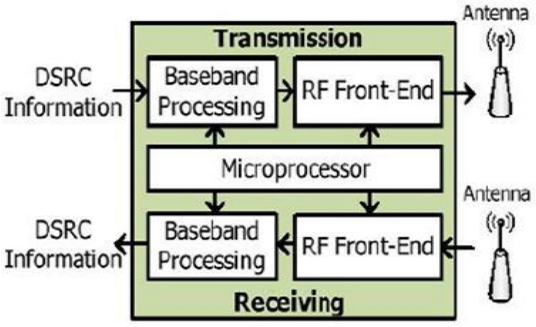

Fig.1. System Architecture of DSRC Transceiver

The automobile-to road side focuses on the intelligent transportation service, such as electronic toll collection (ETC).The DSRC architecture having the transceiver. The transceiver having the baseband processing, RF front end and microprocessor the microprocessor is used to transfer the instruction to the baseband processing and RF front end. The RF front end is used to transmit and receive the wireless signals using the antenna. The baseband processing is responsible for modulation, error correction, encoding and synchronization. The transmitted signal consists of the arbitrary binary sequence, it is very difficult to obtain the dc-balance.the fm0 and Manchester is providing the transmitted signal and then the dc-balance. The (SOLS) similarity oriented logic simplification having the two methods: area compact retiming and balance logic operation sharing. The area compact retiming used to reduce the transistor counts the balance logic operation sharing is used to combine the fm0 and Manchester encoding. The system architecture of DSRC transceiver is shown in Fig1. The upper and bottom parts are dedicated for transmission and receiving, respectively. This transceiver is classified into three basic modules: microprocessor, baseband processing, and RF frontend. The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end. The baseband processing is responsible for modulation, error correction, clock synchronization, and encoding. The RF frontend transmits and receives the wireless signal through the antenna.

Table I. Profile of DSRC Standards for America, Europe, Japan

	Europe	America	Japan
Organization	CEN[1]	ASTM[2]	ARIB[3]
Data Rate	500 kbps	27 Mbps	4 Mbps
Carrier Frequency	5.8 GHz	5.9 GHz	5.8 GHz
Modulation	ASK, PSK	OFDM	ASK
Encoding (Downlink)	FM0	Manchester	Manchester

[1] European Committee for Standardization.
[2] American Society for Testing and Materials.
[3] Association of Radio Industries and Businesses.

The DSRC standards have been established by several organizations in different countries. These DSRC standards of America, Europe, and Japan are shown in Table I. The data rate individually targets at 500 kb/s, 4 Mb/s, and 27 Mb/s with carrier frequency of 5.8 and 5.9 GHz. The modulation methods incorporate amplitude shift keying, phase shift keying, and orthogonal frequency division multiplexing. Generally, the waveform of transmitted signal is expected to have zero mean for robustness issue, and this is also referred to as dc-balance.

II. LITERATURE SURVEY

The transmitted signal consists of arbitrary binary sequence, which is difficult to obtain dc balance. The purposes of FM0 and Manchester codes can provide the transmitted signal with dc-balance. Both FM0 and Manchester codes are widely adopted in encoding for downlink. The VLSI architectures of FM0 and Manchester encoders are reviewed as follows A. review of VLSI Architectures for FM0 Encoder and Manchester Encoder The literature proposes VLSI architecture of Manchester encoder for optical communications. This design adopts the CMOS inverter and the gated inverter as the switch to construct Manchester encoder. It is implemented by 0.35-μm CMOS technology and its operation frequency is 1 GHz. The literature further replaces the architecture of switch by the nMOS device. It is realized in 90-nm CMOS technology, and the maximum operation frequency is as high as 5 GHz. The literature develops a high speed VLSI architecture almost fully reused with Manchester and Miller encodings for radio frequency identification (RFID) applications. This design is realized in 0.35-μm CMOS technology and the maximum operation frequency is 200 MHz. The literature also proposes a Manchester encoding architecture for ultrahigh frequency (UHF) RFID tag emulator. This hardware architecture is conducted from the finite state machine (FSM) of Manchester code, and is realized into field-programmable gate array (FPGA) prototyping system. The maximum operation frequency of this design is about 256 MHz. The similar design methodology is further applied to individually construct FM0 and Miller encoders also for UHF RFID Tag emulator. Its maximum operation frequency is about 192 MHz. Furthermore, combines frequency shift keying (FSK) modulation and demodulation with Manchester codec in hardware realization.

III. DESIGN OF FM0 &MANCHESTER CODE

The need for SOLS technique is to design a fully reused VLSI architecture for FM0 and Manchester codes. SOLS technique is having two core concepts: area-compact retiming and balance logic operation sharing .The VLSI architecture of FM0 and Manchester code is shown in Fig.2.

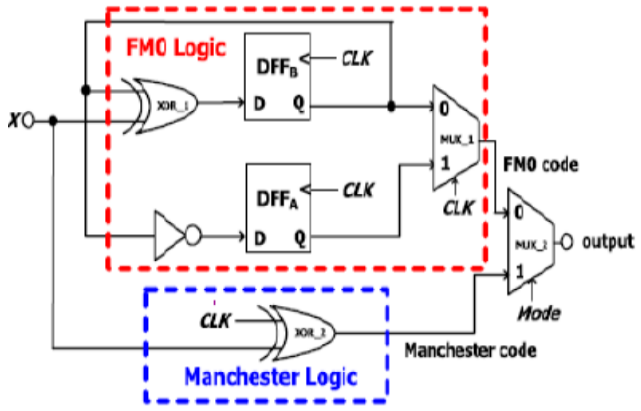

Fig.2. VLSI Architecture of FM0 and Manchester.

The SOLS technique improves the HUR from 57.14% to 100%, whether the FM0 or Manchester code is adopted. Thus, the SOLS technique provides a fully reused VLSI architecture for FM0 and Manchester encodings with the HUR of 100%. The logic functions of SOLS technique can be realized by various logic functions to optimize more performance such as area, power, and speed. The proposed SOLS technique is developed from the architecture perspective to achieve 100% HUR. If the logic components in SOLS architecture are designed using static CMOS, the Manchester delay is seriously limited owing to too many transistors in the critical path of Manchester encoder. To further reduce the transistor count in Manchester encoding path, the transmission-gate logic is considered in the circuit designs of MUX−1, MUX−2 and XNOR. The propagation delay of transmission-gate logic is less than that of static CMOS. Applying the transmission gate logic can compact the transistor count to reduce the propagation delay.

IV. EXPERIMENT RESULTS & DISCUSSION

A. Experiment Environment

This paper is compared with the existing articles. These articles are implemented in two kinds of design-flows. The literatures [5] and [6] are realized with full-custom and the literatures [8]–[10] are designed with FPGA. To give an objective evaluation, the proposed VLSI architecture is realized with both design-flows, as listed in Table II. The design flow of the full-custom is Taiwan Semiconductor Manufacturing Company (TSMC) 0.18-μm 1P6M CMOS technology, and the Xilinx development board is adopted for the FPGA design-flow. The performance of full-custom design flow is from post layout simulation, and its layout view is shown in Fig. 3. The performances of [5], [6], and [8]–[10] are listed in Table III. Note that [7] is excluded since it further involves Miller encoding, which is out of the scope of this performance evaluation. The CMOS technologies of these works include 0.35 μm, 90 nm, which are not identical to 0.18 μm adopted in this paper. To normalize the process parameters due to different CMOS technologies, the CMOS process scaling of the constant field theorem is applied. The normalization equations are given as follows:

TABLE-II: Performance of the Proposed vlsi Architecture of fm0 and Manchester Encodings using the sols Technique

Realization	0.18 um CMOS		Xilinx FPGA Spartan 2	
Supply voltage	1.8 V		3.3 V	
Coding methods	Manchester	FM0	Manchester	FM0
Operation frequency	2 GHz	900 MHz	296 MHz	
Power consumption	1.58 mW	1.14 mW	28.30 mW	
HUR	100%		100%	
Area	65.98 × 30.43 um^2		N/A	
Transistor count	44		N/A	
FPGA resource usage	N/A		Slice : 1 Flip-Flop: 1 LUTs :1 Bonded IOBs : 5	

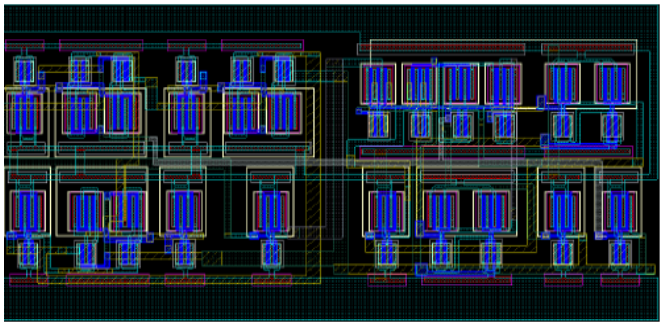

Fig.3. Layout View of This Paper

TABLE III: - Performance Profile

	2003 [4]	2009 [5]	2008 [7]	2009 [8]	2013 [9]
Coding methods	Manchester	Manchester	Manchester	FM0	Manchester
Realization	0.35 um CMOS	90 nm CMOS	Xilinx FPGA Spartan 2	Xilinx FPGA Spartan 2	Xilinx FPGA Spartan 2
Supply voltage	3.3 V	1.2 V	N/A	N/A	N/A
Technique	Gated inverter	CMOS switch	FSM based design	FSM based design	Joint MODEM CODEC
HUR	N/A	N/A	N/A	N/A	N/A
Operation frequency	1 GHz [1.94 GHz]*	5 GHz [2.5 GHz]*	256.54 MHz	192.64 MHz	612 MHz
Power consumption	N/A	N/A	N/A	N/A	34 mW
Area	N/A	N/A	N/A	N/A	N/A
Transistor count	54	26	N/A	N/A	N/A
FPGA resource usage	N/A	N/A	Slice : 1 Flip-Flop : 2 LUTs : 2 Bonded IOBs : 3	Slice : 5 Flip-Flop : 4 LUTs : 10 Bonded IOBs : 4	Slice : 1 Flip-Flop : 0 LUTs : 1 Bonded IOBs : 3

* Normalized to 0.18 um CMOS process with (15) and (16).

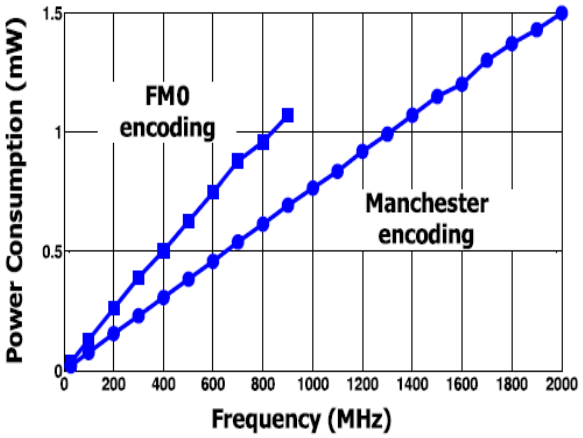

Fig.4. Power Profiling of this Paper for FM0 and Manchester Encodings.

$$\begin{cases} f_{0.18\mu m} = f_{0.35\mu m/90nm \times \alpha} \\ P_{0.18\mu m} = P_{0.35\,\mu m}/90nm \times \frac{1}{\alpha} \\ A_{0.18\mu m} = A_{0.35\mu m/90\,nm} \times \frac{1}{\alpha^2} \end{cases} \quad (1)$$

Where the $f0.18\mu$m, $P0.18\mu$m, and $A0.18\mu$m represent the normalized operation frequency, power, and area for 0.18-μm CMOS process. The α is a scaling factor defined as

$$\alpha = \begin{cases} \frac{0.35\mu m}{0.18\mu m}; \text{from } 0.35\ \mu m \text{ to } 0.18\ \mu m \\ \frac{90nm}{0.18\mu m}; \text{ from } 90 \text{ nm to } 0.18\ \mu m \end{cases} \quad (2)$$

B. Comparison with Sophisticated Articles

This paper adopts the proposed SOLS technique to construct a fully reused VLSI architecture for both FM0 and Manchester encodings. Every logic component of this design is not only used in FM0 encoding, but also in Manchester encoding. None of them is wasted in either encoding function; therefore, the HUR of the proposed VLSI architecture is as high as 100%. The performance evaluation classifies the electrical characteristics into the operation frequency, the power consumption, and the area. They are all normalized to 0.18 μm for an objective evaluation by (1).

Table IV: Implementation Result of Fm0 and Manchester Logics In Fig. 6

	FM0 logic		Manchester logic
Realization	TSMC 0.18 um	Xilinx FPGA Spartan 2	Xilinx FPGA Spartan 2
Supply voltage	1.8 V	3.3 V	3.3 V
Operation frequency	1 GHz	188 MHz	673 MHz
Power consumption	5.87 mW	22.9 mW	36.8 mW
Transistor count	72	N/A	N/A
FPGA resource usage	N/A	Slice : 2 Flip-Flop: 2 LUTs : 2 Bonded IOBs : 3	Slice : 1 Flip-Flop: 0 LUTs : 1 Bonded IOBs : 3
Combination of article	[4], [5]	[7], [9]	[8]

Table V: Performance Evaluation on Fm0 Encoding

	2009 [8]	This work
Design-flow	FPGA	FPGA
FOM_1 (Mbps/device)	6.88	37
FOM_2 (device/coding mode)	14	4
HUR (%)	82.14	100

For Manchester encoding, the operation frequency of this paper is comparable with that of [5], but slower than that of [6]. The literature [6] is dedicated to optimize the signal path by reducing the number of transistors, and thereby has faster operation frequency. Instead, this paper integrates the signal paths of both FM0 and Manchester encodings together. This causes the overhead on the operation frequency of Manchester encoding. Suppose its operation frequency can be scaled up to 2 GHz by 5.14 times and so does its power consumption, which is 1.44 mW at 2 GHz. The proposed design consumes a comparable power of 1.58 mW at 2 GHz. The Manchester encoder of [10] consists of an inverter and a two-input 1-bit multiplexer. To obtain an objective evaluation, it is rebuilt with the identical FPGA device, Xilinx FPGA Spartan 2. This design involves fewer components in Manchester encoding and exhibits a higher operation frequency of 612 MHz. For FM0 encoding, [9] is directly synthesized by FPGA development software from FSM. Note that in full-custom design flow, the power consumption of Manchester encoding is 1.58 mW at 2

GHz. If it is operated at the clock rate of 900 MHz, which is identical to that of FM0 encoding, this power consumption is estimated as 0.71 mW at 900 MHz. It is about 62.28% of that for FM0 encoding, which is 1.14mWat 900 MHz. The reason why FM0 encoding dissipates more power than Manchester encoding is explained as follows: The dynamic power can be given as

$$P = \gamma f C V^2 \qquad \textbf{(3)}$$

where γ, f, C, and V denote the switching-activity, operation frequency, equivalent capacitance of a circuitry node, and supply voltage, respectively. The circuitry node in a CMOS circuit generally means one of three terminals of a CMOS transistor: source, drain, and gate. Note that the body is connected to power supply or ground. Every circuitry node is connected to each other, and total parasitic capacitance of a circuitry node is lumped into C. Both FM0 and Manchester encodings are performed on same VLSI architecture, and their C and V are identical to each other. Suppose that both FM0 and Manchester encoders are operated at the same f.. In the Manchester encoding sets the Mode = 1 and CLR = 0. In other words, the Q of DFF*B* is kept at logic-0 in Manchester encoding. The transistor count of DFF*B* is 44% of total transistor count. It is equivalent that the DFF*B* almost dominates 44% of all switching-activity. The Manchester encoding saves the switching-activity of DFF*B*, and thereby exhibits lower switching-activity. Instead, the FM0 encoding activates all logic components, and certainly leads to a higher switching-activity compared with that of Manchester encoding. The power profiling of both FM0 and Manchester encodings is shown in Fig.4. The operation frequency ranges from 27 to 900 MHz for FM0 encoding and to 2 GHz for Manchester encoding, respectively. Since the switching activity of FM0 encoding is higher than that of encoding, FM0 encoding has more power consumption than Manchester encoding at the same operation frequency. The SOLS technique integrates Manchester and FM0 encodings into fully reused hardware architecture. Obviously, the coding procedure of FM0 is more complex than that of Manchester. The data path of Manchester encoding is restricted to that of FM0 encoding. Then, the operation frequency of Manchester encoding is also limited by that of FM0 encoding. Our work targets at an efficient integration of hardware devices for Manchester encoding and FM0 encoding instead of operation frequency and power consumption. Generally, more coding methods hardware architecture can support more hardware devices it requires

Table VI: - Performance Evaluation on Manchester Encoding

	2003 [4]	2009 [5]	2008 [7]	2013 [9]	This work	
Design-flow	Full-custom	Full-custom	FPGA	FPGA	Full-custom	FPGA
FOM_1 (Mbps/device)	15.39	25.51	15.09	43.71	45.45	37
FOM_2 (device/coding mode)	63	49	8.5	7	22	4
HUR (%)	42.85	26.53	47.05	35.71	100	100

A performance evaluation is given under identical conditions for a more objective evaluation. A building block that can perform FM0 and Manchester encodings is considered an evaluation platform. The literatures [5], [6], and [8] – [10] are dedicated for either FM0 or Manchester encoding. To make these literatures fit the evaluation platform; the FM0 logic is implemented in full-custom to combine [5] and [6] and in FPGA to combine [8] and [10]. The Manchester logic of Fig. 6 is realized in FPGA to combine [9]. Table IV shows the implementation result of FM0 and Manchester logics. The evaluation platform consists of two coding methods, and how to efficiently allocate hardware devices to perform them is a critical design issue for performance evaluation. To measure the device-efficiency of each work, two Figs of merits (FOMs) are defined as follows:

$$\begin{cases} \mathrm{FOM}_1 = \dfrac{\text{Data rate}}{\text{Total devices}}; (\mathrm{Mb/s/device}) \\ \mathrm{FOM}_2 = \dfrac{\text{Total devices}}{\text{Total coding modes}}; (\text{device}|\text{coding mode}) \end{cases} \qquad \textbf{(4)}$$

where the data rate is either for FM0 or Manchester encoding. Total coding modes denote how many coding methods a hardware architecture can support. In this evaluation platform, total coding modes are set to 2, representing FM0 and Manchester encodings. The total devices mean the total transistor count and total FPGA resource for full-custom and FPGA designs, respectively. FPGA resource incorporates Slice, Flop-Flip, LUTs, and Bonded IOBs. The total FPGA resource is a summation of the FPAG resource used in both Manchester and FM0 encodings. Similarly, the total data rate is a summation of the data rates of both FM0 and Manchester encodings. The data date of each work is identical to the operation frequency of each work.

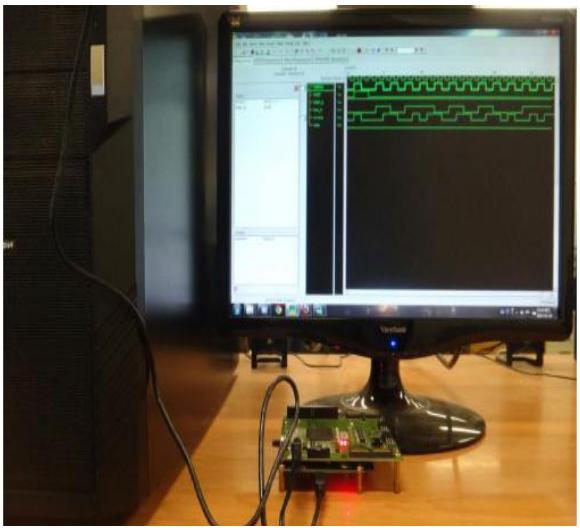

Fig.5. FPGA Prototyping Environment

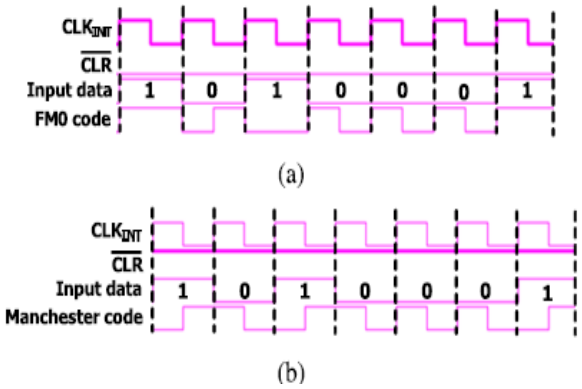

Fig.6. Waveform of FPGA Prototyping (a) FM0 Encoding

(b) Manchester encoding

The operation frequencies designed with non 0.18 μm are normalized to 0.18 μm by (1) and (2), as previously shown in Table VII. Hence, the compensation of technology-dependent differences on data rate is considered in FOM1. The FOM1 means how high the data rate a single device can contribute on average is. The FOM2 represents how many devices are required for a single coding mode on average. This performance evaluation is classified into two categories: FM0 and Manchester encodings in Tables V and VI, respectively. For FM0 encoding, this paper exhibits outstanding FOM1, FOM2, and HUR in comparison with [9]. For Manchester encoding, the FOM1 of this paper is less than that of [10] by 15.35%. However, this paper has almost half the FOM2 of and 2.8 times the HUR. In full-custom design flow, this paper still has higher performance on FOM1, FOM2, and HUR compared with [5] and [6]. Therefore, the SOLS technique presents a quite competitive performance on device-efficiency.

C. FPGA Prototyping

This paper is also implemented with FPGA not only for an objective comparison but also for the functional prototyping, as shown in Fig. 5. However, the signal-transition of FM0 and Manchester codes is not aligned to the positive- or negative-edge trigger. To be compatible with the synchronization of FPGA, two sets of clock, CLKEXT and CLKINT, are adopted in this FPGA prototyping system. The frequency of CLKEXT is twice as fast as that of CLKINT. The faster CLKEXT is used to synchronize every signal inside FPGA. The slower CLKINT is for the encoding manipulation of FM0 and Manchester codes. The waveforms of the functional verification are shown in Fig. 6, where the FM0 and Manchester encodings are shown in Fig. 6(a) and (b), respectively.

V. CONCLUSION.

In this paper, SOL's technique was effective implemented for power and coding efficient VLSI architecture. The SOL'S technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The coding-diversity between FM0 and Manchester encodings causes the limitation on hardware utilization of VLSI architecture design. A limitation analysis on hardware utilization of FM0 and Manchester encodings is discussed in detail The area-compact retiming relocates the hardware resource to reduce the transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. This paper is realized in180nm technology with outstanding device efficiency. The power consumption is 29392.843nW for Manchester encoding and FM0 encoding.

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