

Design of Second Order Adiabatic Logic for Energy Dissipation in VLSI CMOS Circuits

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Abstract

These circuits produce an energy savings of at most one order of $V_{dd} = V_i$. This paper propose a novel class of adiabatic total circuits that fact offer several advantages over existing approaches, the prime one being that, because no diodes are used, switching energy can be decreased to an energy flooring of $O(CV_i^2)$. These second order adiabatic computing circuits produce an energy savings of as much as $O(V_{dd} = V_i^2)$ over general CMOS. The proposed circuits have been simulated and determine adiabatic power savings compared to standard CMOS circuits over an performing frequency range from 1MHz to 100MHz using Cadence virtuoso tool at 45nm technology. We proposed a Basic 2N-2P differential buffer/inverter, 4-Phase shift register bit, Complex gate. Basic 2N-2N2P Inverter/Buffer Gate, adiabatic Full Adder using CADENCE EDA tool at 45nm technology.

Keywords— Standard CMOS circuits, adiabatic full adder, low frequency, low power, Energy dissipation, ,Complex gate, 4-Phase shift register bit, VLSI.

I. INTRODUCTION

A. Energetic and Adiabatic Charging

The energetics of standard CMOS (or any other switching system based on a single fixed DC power rail) are straight forward, at the charging switch is closed to charge the load C up to the rail voltage V, a charge $Q = CV$ is pulled out of the positive power rail. At the discharging switch is closed to discharge the load C to ground, the same charge $Q = CV$ is transferred to the ground terminal of the power supply. Over an entire charge/discharge cycle, a total charge of $Q = CV$ was taken from the positive rail of the power supply and returned to the ground terminal, and thus the total energy dissipated over the entire cycle corresponds to

$Ed_{total} = Ed_{charge} + Ed_{discharge} = QV = (CV)V = CV^2$. Since there were two switching events involved, the average energy dissipated during charging and discharging is one half of this total dissipated energy,

$Ed_{average} = \frac{Ed_{total}}{2} = \frac{CV^2}{2}$. In the case where all switch resistors and load capacitors are linear, the energetics are symmetric and the energy dissipated during charging or discharging is exactly equal to this average switching energy:

$Ed_{charge} = Ed_{discharge} = \frac{CV^2}{2}$. In the case of

non ideal or nonlinear circuit elements, the energy dissipated during charging and discharging need not be equal, but because all of the charge was taken from the positive rail and returned to ground, total energy dissipated over the charge/discharge cycle must always equal twice the average switching energy:

$$Ed_{total} = Ed_{charge} + Ed_{discharge} = 2Ed_{average} = CV^2$$

This energy is dissipated by the integrated I^2R loss of the charging and discharging currents through the effective resistance of the circuit (switch resistances (transistor channels) and parasitic resistances from the power rail to the load C and from C to the ground node):

$$Ed_{total} = \int I^2(t)R(I,t)dt \dots(1)$$

Where we have used $R(I,t)$ to include all changes in effective current path resistance either as a function of time (ie: from switching) or as a function of current (from nonlinearities). The key point is that independent of the sizes and/or function of this effective resistance R, the integration of I^2R over the entire charging/discharging cycle is always the same and is equal to

$$Ed_{total} = Ed_{charge} + Ed_{discharge} = QV = (CV)V = CV^2$$

.The reason for this is that in a fixed DC-powered switching system, the circuit elements and the switching current are related: the only way to change the switching current is to change the circuit elements (the linearity of R or C, or the size of R for example), but the dependency between the two will result in no change in the average dissipated energy:

$Ed_{total} = CV^2$: For standard single supply-rail

switching systems, the only way to reduce energy consumption is to reduce the supply voltage V , or the load capacitance C . Of course, architectural approaches can also be employed at the system level to reduce the number of switching events in the system. The essential point is that for systems of this type, if a particular load must be switched to a particular voltage with a particular average frequency, there is nothing that can be done to reduce energy consumption. Adiabatic computing is compatible with the energy savings that can be achieved through reductions in V or C , yet achieves additional reductions in dissipated energy by avoiding the single-rail DC power supply architecture. If a single non-DC power supply rail is used both to charge and discharge a switching node, the energetics change considerably. In this case, total dissipated energy over the charging/discharging cycle need not be related to transfer charge and can in fact be made arbitrarily small. While for the DC power supply case analyzed above, where nodes are charged from the DC power supply rail and discharged into the ground node, the total dissipated energy must be related to the transferred charge:

$$Ed_{total} = Ed_{charge} + Ed_{discharge} = QV, \text{ in the case}$$

that the power supply rail charges the switching node by ramping up and the same power supply rail later discharges the node by ramping down, this dependency between transferred charge and dissipated energy need no longer be true because charge transferred from the power supply to charge the node can be recovered by the same power supply when it later discharges the node. By taking advantage of adiabatic charging principles and charge recovery, this approach to switching breaks the dependency between the switching current and the circuit elements so that

the energy dissipated as I^2R losses during the charging/discharging cycle can be made arbitrarily small. This is accomplished by making use of periodic ramp-like clocked power supplies. How this is done can most easily be seen by considering the I^2R dissipation losses in the adiabatic charging case. For a given ramp time T , the transferred charge in the adiabatic and non-adiabatic cases must be the same: $Q = CV$. The difference between the two in terms of energy dissipated is that, while in the non-adiabatic case the current is highly non uniform, in the adiabatic case, because of the ramp, it can be made much more uniform over the ramp time T , and in fact ideally constant ($I = Q/T$). By slowing down the ramp (increasing T), the charging current can be made arbitrarily small. The energy dissipated during the charging cycle is $Ed_{charge} = I^2RT = IRQ$.

Increasing time T by a factor of α will decrease current I by a factor of α (transferred charge $Q = IT$ will remain the same), but because I^2 is not linear in I , dissipated energy $Ed_{charge} = I^2RT$ will decrease

by a factor of α . Adiabatic charging principles allow dissipated energy to be an arbitrarily small percentage of transferred energy by transferring charge at a constant and arbitrarily slow rate.

In the non adiabatic case, maximum switching current typically flows when the voltage difference between the load C and the voltage rail V or ground are greatest, leading to energy dissipation spikes. While it might be possible to devise a non adiabatic circuit which had a uniform current flow, perhaps even equal to that of the adiabatic circuit, this would only be possible with a highly non uniform resistor which had greatest resistance when the voltage across it was greatest. Because of charge loss, the resistor needed for uniform current would also lead to the same total dissipated energy:

$$Ed_{total} = \int I^2(t)R(I,t)dt = QV \dots\dots(2)$$

The system specification is the processor: Intel (R) core (TM) i5-4570 CPU@3.20GHz.,3.20GHz.Installed memory (RAM) 4 GB (3.43GB Usable) and system type: 32bit operating system.

This paper is formed as follows Section II presents the literature review on adiabatic logic second order energy dissipation and DSP Section III presents the methodology for a Basic 2N-2P differential buffer/inverter, 4-Phase shift register bit, Complex gate. Basic 2N-2N2P Inverter/Buffer Gate and adiabatic Full Adder of Energy Dissipation Section IV shows the simulation results and they are discussed clearly, finally the paper is concluded with Section V.

II. LITERATURE REVIEW

A. Design Work

Programmable reversible logic is developing as a expected logic design style for implementation in low power, low frequency applications point minimal impact on circuit heat generation is desirable, such as reduction of differential power analysis attacks [1]. Major limits of CMOS-based adiabatic logic are analyzed. Analytic relations describing the energy-performance for sub-threshold adiabatic logic are also explicitly derived and optimized [2].Power optimization in circuits and systems is the demanding factor for most of the designers and industries. Many power dissipation techniques have been introduced but most of these techniques have some pact [3]. Although the concepts of adiabatic charging have been well-established for some time [4,5], early circuit proposals, Although very interesting from a theoretical standpoint, were not practicable for large-scale implementation due to the bulkiness and complexity of the circuits, the large overheads involved, the complexity of the timing and power supply/clock generation and the relatively slow speeds at which

they would operate. Currently interest has resulted in several much more practical circuit implementations of adiabatic computing circuits [6, 7,8,9,10,11,12,13]. These circuits, rather than aiming to achieve energy dissipation floors approaching the theoretical minimum, achieve much more practical implementations by aiming for energy floors which are only a factor of 2 - 20 less than that of conventional static CMOS logic is called vanilla CMOS from now on Several recently design uses make use of the fact that diodes can be used to provide very compact and efficient adiabatic charging elements [4,5,8,11]. These circuits exhibit adiabatic energy savings, but the use of diodes for adiabatic charging in any circuit limits this saving to a factor of $V = V_t$ over that of conventional circuits. The reason for this is that a diode will have a voltage drop which is to first order constant and equal to V_t for any positive current driven through it. This means that for a diode, $IR = V = V_t$ (it is a nonlinear current-dependant resistor), and energy dissipated in adiabatic charging through a diode cannot be less than $E_d = I^2RT = IT * IR = QV_t = CV_t$. The maximum energy savings possible though any diode-based adiabatic charging circuits is thus limited to $1/(QV/QV_t) = 1/(V/V_t)$, no matter how slowly the charging occurs.

III. DESIGN METHODOLOGY

A. Order of Adiabatic Dissipation

We have found this factor of $V = V_t$ to be a useful reference in analyzing energy dissipation in adiabatic circuits as compared to conventional switching circuits. First order adiabatic losses correspond to losses which have a floor of $O(CVV_t) = O(QV/[V/V_t])$, such as the diode charging losses described above. Second order adiabatic losses correspond to losses which have a floor of $O(CV_t^2) = O(QV/[V/V_t]^2)$, such as a non adiabatic switching event from V_t to ground. By this convention, theoretical energy floors which are independent of V_{dd} and V_t such as kT would be called Nth order adiabatic losses. Practical adiabatic computing circuits typically contain first and/or second order loss terms, and thus have energy floors which are high compared to the theoretical minimum. While it would seem that first order losses are more important than second order losses, $V = V_t$ is typically not very large and any loss term has a scaling factor in front of it, so it does not take many second order loss terms to equal a first order loss term. In fact, while diode based adiabatic charging systems must have a first order energy loss, they often have one more second order losses which may dominate the actual energy floor.

B. Second Order Adiabatic Circuits

This work proposes a new class of circuits with a low energy floor. The essential energy advantage of these circuits comes from the fact that they have been adiabatically designed to eliminate all first order energy losses and to minimize second order losses as much as possible. This is accomplished primarily by charging nodes through minimal switch resistances rather than diodes. The circuits we describe realize this advantage with minimal additional overhead and complexity over diode-based circuits, either at the circuit or system level. These circuits are at most two times the size of the smallest diode-based adiabatic circuits, making them about the same size as vanilla CMOS, and they operate at similar frequencies of greater than 100MHz. Another advantage of these new circuits is that, while most diode-based adiabatic computing circuits have output levels which are floating during their output valid time, these new circuits provide outputs which are clamped during their output valid time (like vanilla CMOS). This is important at the system level in terms of reducing crosstalk and restoring logic levels.

C. Basic operation of the 2N-2P Family

The first of these circuits we will introduced is called 2N-2P. The name is based on our convention of using the number of transistors in a gate because the cost for each input in terms of transistors is 2 Nfets and the overhead for each complete gate is 2 Pfets. The circuit uses differential logic, so each gate computes both a logic function and its complement, and each input to a gate requires both polarities to be represented. The basic circuit for a inverter-buffer is shown in Fig 1. Each Nfet input gets the corresponding positive and negative polarity inputs and the cross-coupled Pfets are connected to the clock-supply. The timing and logical operation of the gate is as follows (Fig 2):

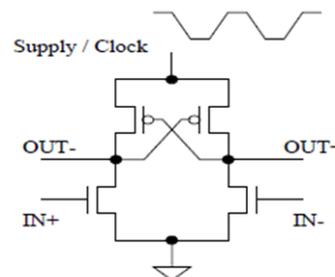


Figure 1: Basic 2n-2p Differential Buffer/Inverter.

D. Complex Gates and Sequences of Gates

Because there are four phases to the timing, there must be four quadrature clocks in a complete system, each clock 90 degrees in advance of the previous clock. In this way, each logic phase in the system holds its outputs valid while its successor is evaluating (ramping up) and its predecessor is

resetting (ramping down) and waits with its outputs both low while its successor is resetting (down) and its successor is evaluating (up).

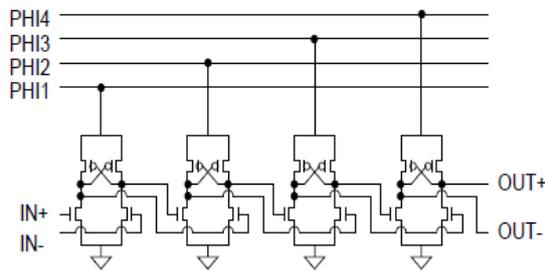


Figure 2: 4-Phase Shift Register Bit.

A shift register can be constructed by making a sequence of buffer/inverter gates connected sequentially and in the proper phase relationship, that is: PH1, PH2, PH3, PH4, PH1, ..(figure 2). We have simulated an cadence virtuoso 45nm technology CMOS implementation of such shift registers using minimum size transistors at speeds in excess of 100 MHz

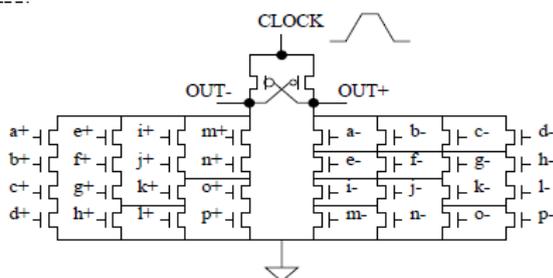


Figure 3: Complex Gate.

More complex gates can be constructed by replacing the single Nfets used in the inverter/buffer with an arbitrary Nfet-based logic tree and its inverse (fig 3). Because the differential logic provides both negative and positive polarity signals, providing both positive and negative logic trees using only Nfets is straightforward: while in vanilla CMOS the positive logic tree is created by connecting a single input polarity to Nfets and the negative logic tree is created by connecting the same input polarity to the Pfet-based inverse tree, in the case of differential logic both the logic tree and its inverse can be Nfet-based as every Nfet connected to an input in the logic tree has a corresponding Nfet connected to the inverted input in the inverse logic tree. We have simulated logic gates with up to 4x4=16 inputs at speeds up to 100MHz.

E. 2N-2N2P and System Issues

A variant on the 2N-2P logic family described above is that of the 2N-2N2P family, the only difference being that 2N-2N2P has a pair of cross-coupled Nfets in addition to the cross-coupled Pfets common to both families (fig 4). 2N-2N2P thus has cross-coupled full inverters and thus is very similar to a standard SRAM cell. The timing and

logical operation of 2N-2N2P is identical to that of 2N-2P.

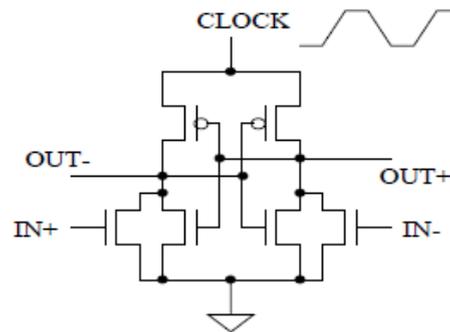


Figure 4: Basic 2n-2n2p Inverter/Buffer Gate.

Fully-static logic such as vanilla CMOS has outputs which offer two important advantages at the system level. The first of these is that its outputs are always clamped to either V_{dd} or Gnd. This is important to restore logic levels and reduce the effects of crosstalk. The second advantage is that fully-static logic has static outputs which are always valid; if the inputs do not change neither do the outputs. This is important for simplifying timing and system design. Dynamic logic such as domino CMOS enjoys neither of these advantages.

F. Energy Dissipation

The analyses of the energetics of the 2N-2P and 2N-2N2P adiabatic logic families are identical. The analysis requires a more electrical description of the timing. As already described in the logical timing description, during the RESET phase, when the clock is ramping down and the inputs are held low, one output is already low and the other output "rides" the clock down. The high output will ride down only to V_t , rather than gnd, because at that point the Pfet ceases to conduct. Following RESET then, both outputs are not low but rather the low output is low while the high output is floating at V_t . If during the EVALUATE phase, the logical state of the gate has not changed (the high output should continue to be high), the high output which is floating at V_t will ride the clock up, beginning its conduction when the rising clock has again reached a voltage of V_t . These details do not really change the analysis of the energetics in the case when the logical state of the gate has not changed. Because the upward and downward ramp on the output is fully adiabatic, energy loss can be made arbitrarily small by making the ramp time arbitrarily long. During the HOLD phase, when the outputs are floating, there is no energy loss. When the gate output state makes a transition from one logical state to the other, the fact that the old high output was floating at V_t becomes critical however. During the HOLD phase the inputs become valid and the logical state of the gate will change. This means that the floating

output, which in the previous state was high and thus had a non conducting logical Nfet tree, will now have a conducting tree. These valid inputs will thus connect the floating output, which is at a voltage of V_t , to ground and the result is a non adiabatic charge transfer of $Ed_{discharge} = O(CV_t^2)$. The same is true for the old low output which now must ride the ramp up; it will make a non adiabatic transition from Gnd to V_t when the ramp reaches V_t and this will dissipate energy of $Ed_{discharge} = O(CV_t^2)$. Because charge of $Q = CV_t$ was supplied from the ramp to the load when the ramp was at a voltage of V_t and this charge was later transferred to Gnd, the total energy dissipation for the charge/discharge cycle can be determined as before:

$$Ed_{total} = Ed_{charge} + Ed_{discharge} = CV_t^2$$

. Because this energy loss is non adiabatic, there is no way to reduce it; it is independent of clock speed. These 2 logical families will thus lose some arbitrarily small energy at each clock cycle corresponding to adiabatic I^2R losses in the Pfets and will lose CV_t^2 at each gate transition cycle. This can be compared to vanilla CMOS, which will lose some small energy as leakage at all times and will lose CV^2 for each transition cycle.

IV. SYNTHESIS AND SIMULATION RESULTS

The Simulations of Basic 2N-2P differential buffer/inverter using Cadence Virtuoso EDA tool at 45nm technology. These simulations are obtained using the specifications shown in table 1.

TABLE 1: NMOS AND PMOS SPECIFICATIONS

Specification	NMOS	PMOS
Library name	Gpdk 45	Gpdk45
Length	45 nm	45 nm
Total width	120 nm	240 nm
Finger width	120nm	240 nm
Rise/fall time	100f s/100f s	
Load Capacitance	5fF	

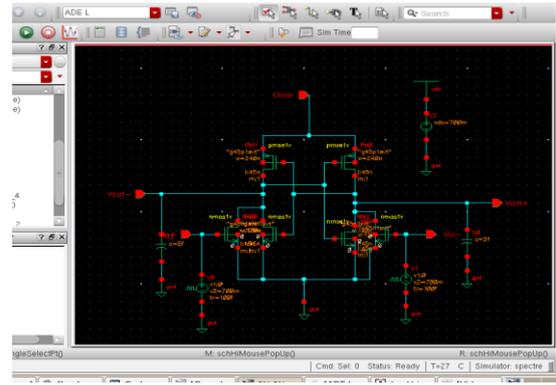


Figure 5 Basic 2N-2P Differential Buffer/Inverter Of Schematic Diagram.

Figure 5 gives Basic 2N-2P differential buffer/inverter with the inputs of Vin+, Vin- and outputs of Vout+, Vout-. For all inputs combinations frequency of 100MHz signal is applied and verified

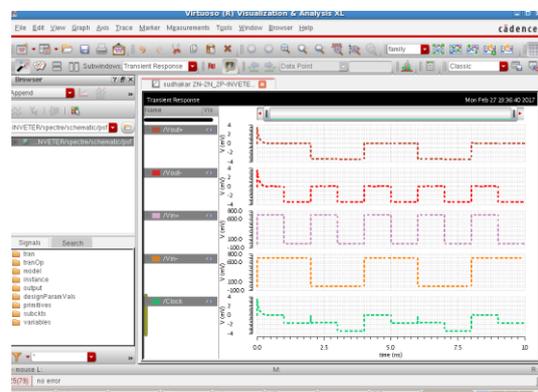


Figure 6 Basic 2N-2P Differential Buffer/Inverter Of Simulation Output Waveform At The Frequency 100M Hz.

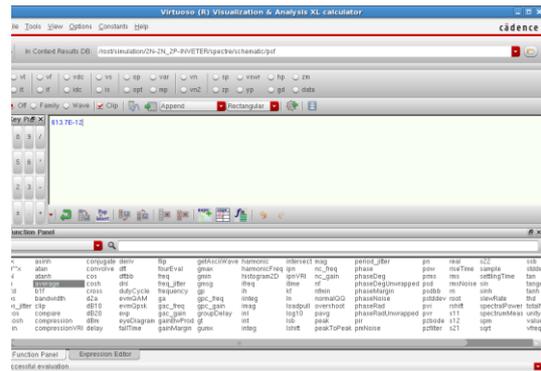


Table 7 Basic 2N-2P Differential Buffer/Inverter Power Dissipation,

Table 2 Basic 2N-2P Differential Buffer/Inverter

Voltage (V)	Frequency (MHz)	Power (pW)	Energy Dissipation (fJ) $Ed_{charge} = (I^2R) * T$
0.7	1	611.1	0.61100
	2	611.2	0.305600
	10	611.4	0.061140
	20	611.8	0.030590

100	613.7	0.006131
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outputs of V_{out+} , V_{out-} . For all inputs combinations frequency of 100MHz signal is applied and verified

Table 2 is observed that the power and energy dissipation and 1MHz to 100MHz frequency range at 0.7V.

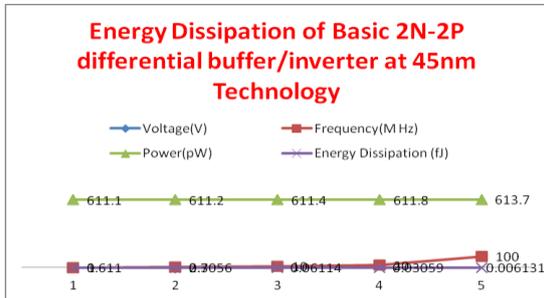


Figure 8 Energy Dissipation of Basic 2N-2P Differential Buffer/Inverter at 45nm Technology.

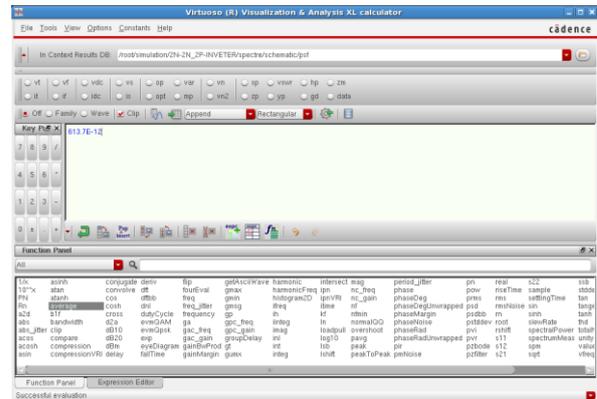


Figure 11 2N-2N2P Buffer/Inverter Of Power Dissipation

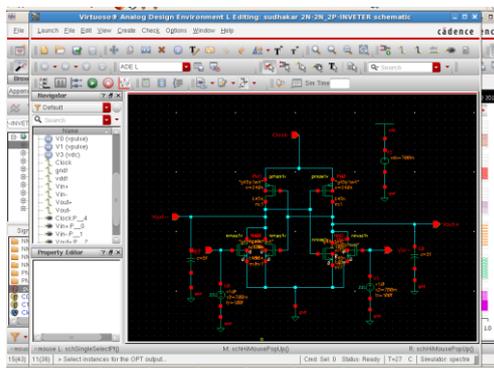


Figure 9 Basic 2N-2N2P Inverter/Buffer Gate of Schematic Diagram

Table 3 Energy Dissipation Of Basic 2N-2N2P Buffer/Inverter

Volta ge(V)	Frequen cy(M Hz)	Power(pW)	Energy Dissipation(fJ) $E_{d_{charge}} = (I^2 R) * T$
0.7	1	613.7	0.613700
	2	611.8	0.305900
	10	611.4	0.061120
	20	611.2	0.030560
	100	611.1	0.006111

Table 3 is observed that the power and energy dissipation and 1MHz to 100MHz frequency range at 0.7V

The Simulations of Basic 2N-2N 2P Inverter/Buffer using Cadence Virtuoso EDA tool at 45nm Technology. These simulations are obtained using the specifications shown in table 2, Figure 9 gives Basic 2N-2N2P differential buffer/inverter with the inputs of V_{in+} , V_{in-} and outputs of V_{out+} , V_{out-} .

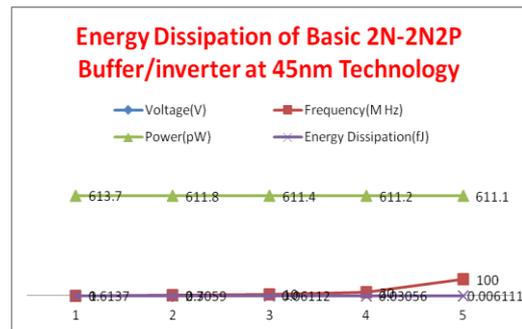


Figure 12 Energy Dissipation Of Basic 2N-2N2P Buffer/Inverter



Figure 10 Basic 2N-2N2P Buffer/Inverter Output Wave form at Frequency 100mhz.

Figure 10 gives Basic 2N-2N2P differential buffer/inverter with the inputs of V_{in+} , V_{in-} and

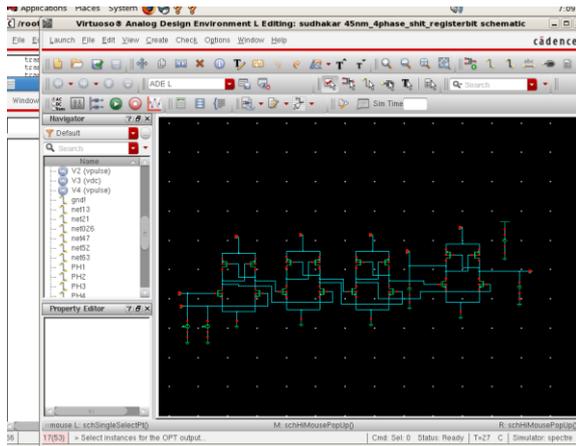


Figure 13 4-Phase Shift Register Bit Of Schematic.

Figure 13 is the Simulations of 4-Phase shift register bit using Cadence Virtuoso EDA tool at 45nm technology at 0.7V.



Figure 14 4-Phase Shift Register Bit Of Output Waveform

Figure 14 4-Phase shift register bit of output waveform, for all inputs combinations frequency of 100MHz signal is applied and verified.

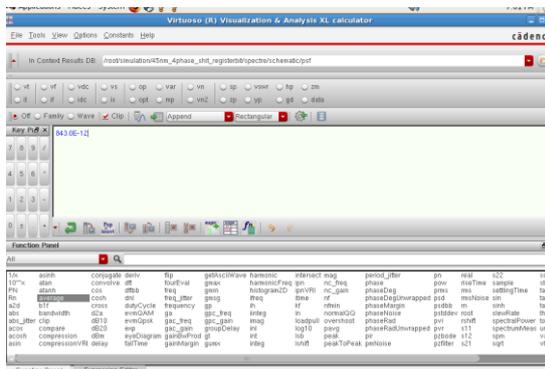


Figure 15 4-Phase Shift Register Bit Of Power Dissipation

Table 4 4 Phase Shift Register Bit

Voltage(V)	Frequency(MHz)	Power(pW)	Energy Dissipation(fJ) $E_{d_{charge}} = (I^2R)*T$
0.7	1	668.6	0.668600
	2	670.1	0.335050
	10	682.5	0.068250
	20	702.2	0.035110
	100	843.0	0.008430

Table 4 is observed that the power and energy dissipation and 1MHz to 100MHz frequency range at 0.7V. The Simulations of 4 phase shift register bit using Cadence Virtuoso EDA tool at 45nm technology. These simulations are obtained using the specifications shown in table 4.

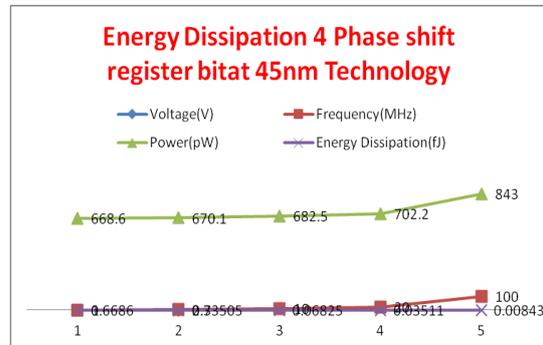


Figure 16 Energy Dissipation Of 4 Phase Shift Register Bit

Figure 16 4-Phase shift register bit of power and energy dissipation of waveform.

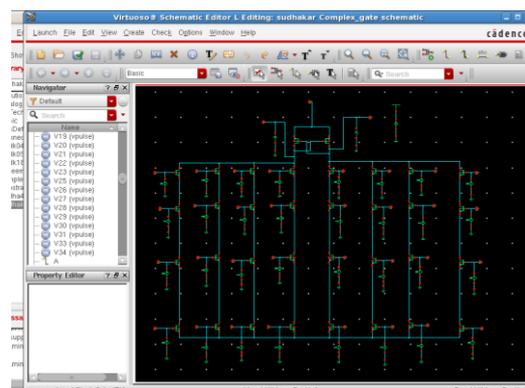


Figure 17 Complex Gate Of Schematic Diagram

Figure 17 is the schematic diagram of Complex gate using Cadence Virtuoso EDA tool at 45nm technology at 0.7V.

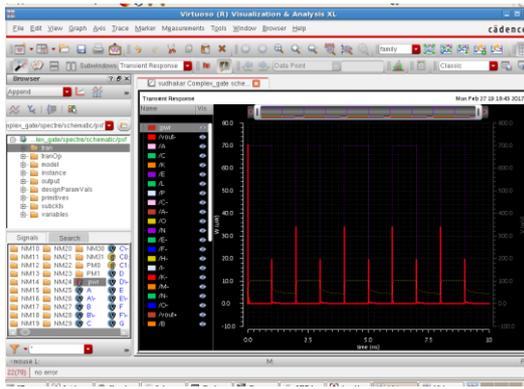


Figure 18 Complex Gate Output Waveform

Figure 18 Complex gate of output waveform, For all inputs combinations frequency of 100MHz signal is applied and verified.

Table 5 Complex Gate

Voltag e(V)	Frequen cy(MHz)	Power(nW)	Energy dissipation (pF) $Ed_{charge} = (I^2 R)$
0.7	1	116.0	0.116000
	2	100.5	0.050250
	10	98.66	0.009866
	20	98.37	0.0049185
	100	100.4	0.001004

Table 5 is observed that the power and Energy dissipation and 1MHz to 100MHz frequency range at 0.7V.

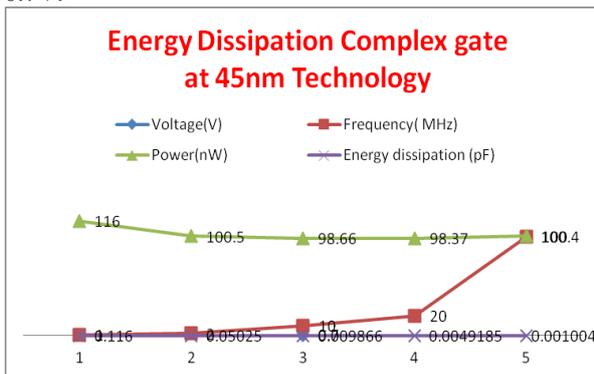


Figure 19 Energy Dissipation Of Complex Gate

Figure 19 Energy Dissipation of Complex gate of using Cadence Virtuoso EDA tool at 45nm technology.

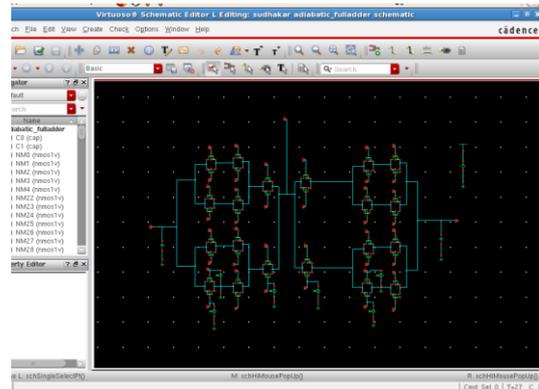


Figure 20 Sum Generation Block Of An Adiabatic Full Adder

Figure 20 Sum generation block of an adiabatic Full Adder of using Cadence Virtuoso EDA tool at 45nm technology load capacitor 10f F applied

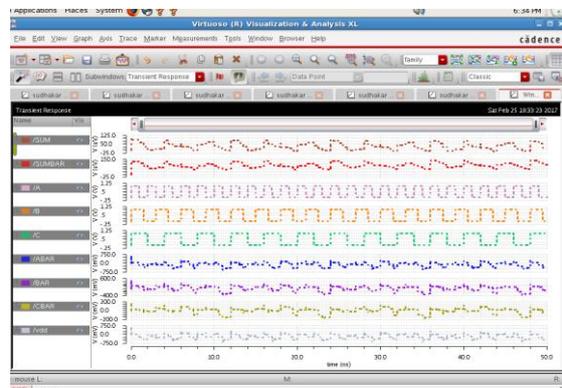


Figure 21 Sum Generation Block Of An Adiabatic Full Adder Of Output Wave Form

Figure 21 Sum generation block of an adiabatic Full Adder of output wave for all inputs combinations frequency of 100MHz signal is applied and verified

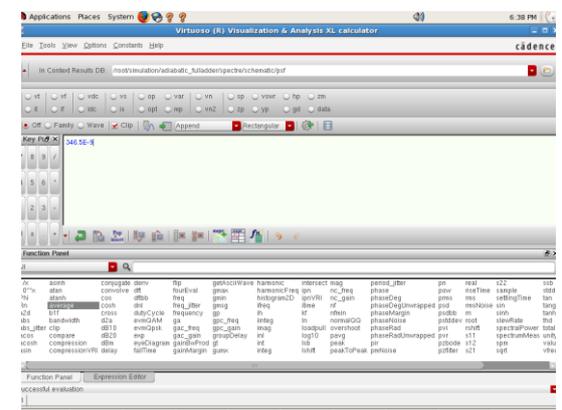


Figure 22 Sum Generation Block Of An Adiabatic Full Adder Of Power Dissipation

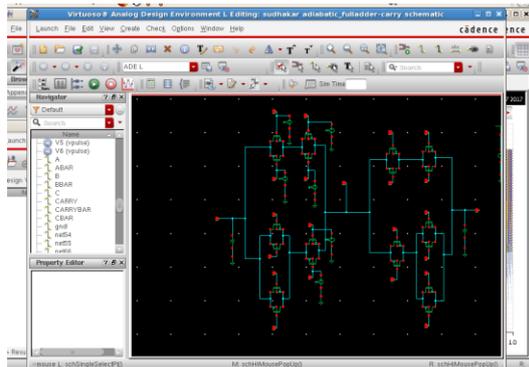


Figure 23 Carry Generation Block Of An Adiabatic Full Adder

Figure 23 Carry generation block of an adiabatic Full Adder using Cadence Virtuoso EDA tool at 45nm technology and load capacitor 10f F applied.

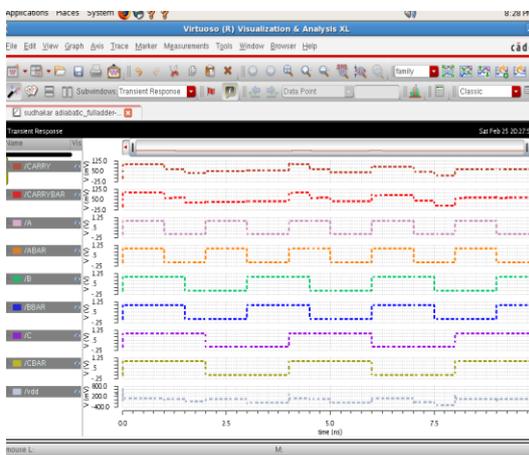


Figure 24 Carry Generation Block Of An Adiabatic Full Adder Output Wave Form.

Figure 24 Carry generation block of an adiabatic full adder output wave form. for all inputs combinations frequency of 100MHz signal is applied and verified.

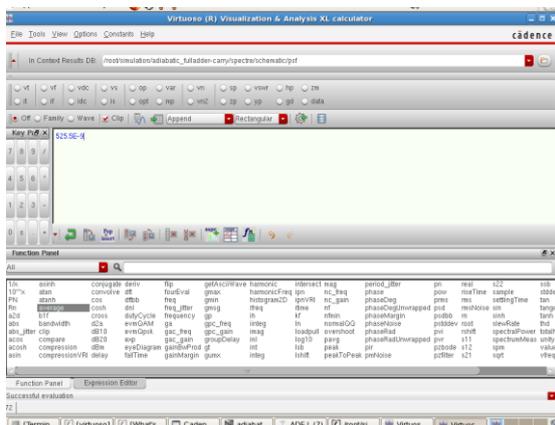


Figure 25 Carry Generation Block Of An Adiabatic Full Adder Of Power Dissipation

Table 6 Comparison In Energy Dissipation Of Adiabatic Full Adder

Vo lta ge(V)	Freq uenc y(M Hz)	Full adder (Sum) Power(nW)	Energy dissipatio n of full adder SUM (pJ)	Full adder (Carr y) Powe r(nW)	Energy dissipation of full adder CARRY (pJ) $E_{d_{change}} = (I^2R)*T$
1	1	674.7	0.674700	504.5	0.504500
	2	675.7	0.337850	505.3	0.252650
	10	354.4	0.35440	505.6	0.050560
	20	358.0	0.017900	508.1	0.025405
	100	346.5	0.003465	525.5	0.005255

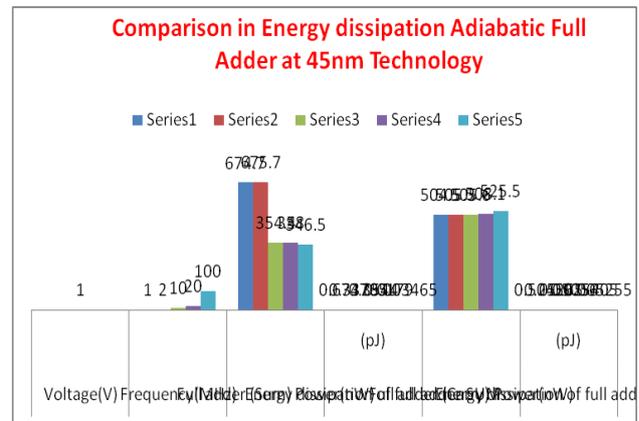


Figure 26 Comparison of power and Energy dissipation Adiabatic Full Adder at 45nm Technology.

Figure 26 Comparison of power and Energy dissipation of adiabatic full adder.

Table 7 Comparison in energy dissipation of Basic 2N-2P Buffer/inverter and 2N-2N2P Buffer/inverter

Basic 2N-2P Buffer/inverter Energy Dissipation(fJ)	Basic 2N-2N2P Buffer/inverter Energy Dissipation(fJ)
0.61100	0.613700
0.305600	0.305900
0.061140	0.061120
0.030590	0.030560
0.006131	0.006111
0.61100	0.613700

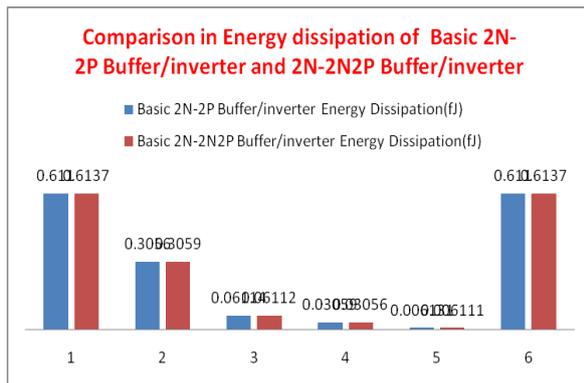


Figure 27 Comparison in energy dissipation of Basic 2N-2P Buffer/inverter and 2N-2N2P Buffer/inverter

Figure 27 Comparison in energy dissipation of Basic 2N-2P Buffer/inverter and 2N-2N2P Buffer/inverter of Comparison in Energy dissipation of adiabatic full adder.

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V. CONCLUSION

In this paper, we designed a Basic 2N-2P differential buffer/inverter, 4-Phase shift register bit, Complex gate. Basic 2N-2N2P Inverter/Buffer Gate, adiabatic Full Adder using CADENCE EDA tool at 45nm technology, Table 2 Comparison of power and energy dissipation of Basic 2N-2P differential buffer/inverter, Table 3 Comparison of power and energy dissipation Basic 2N-2N2P differential buffer/inverter, Table 4 Comparison of power and energy dissipation of 4-Phase shift register bit, Table 5 Comparison of power and energy dissipation of Complex gate, Table 6 Comparison of power and energy dissipation of adiabatic full adder, Table 7 Comparison in energy dissipation of Basic 2N-2P Buffer/inverter and 2N-2N2P Buffer/inverter.

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