Realisation of Vedic Sutras for Multiplication in Verilog

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Abstract

*This project involves application of the Sutras to design a 8*8multiplier circuit based on Vedas. Mathematics, derived from the Vedas, provides one line, mental and superfast methods along with quick cross checking systems.In this Project, four different multiplication sutras are considered, namely, Ekanyunena Purvena, Anurupyena, Antyayor-Dasakepi, Urdhva-Tiryagbhyam for multiplication process. Each multiplication sutras are having their own unique features to determine the product terms. An adaptive multiplication unit will be designed which consists of all these four sutras and a control unit. The intelligent control unit dynamically invokes the suitable multiplication algorithm based on the input data. The final Product will be available in minimum delay with optimized area. The entire hardware including the control unit is designed using Verilog and it is to be implemented in FPGA.*

Keywords — *Ekanyunena Purvena, Anurupyena, Antyayor Dasakepi, Urdhva Tiryagbhyam, Vedic mathematics.*

I. INTRODUCTION

Multiplication is one of the significant arithmetic operation used in the computers which always a challenging task. Researchers had developed a number of multiplication techniques with the advancement of technology to meet several constraints such as fast computation, low power consumption and reduced area occupancy. Thus there is always a demand for the high speed multipliers which can fulfill all the constraints. The speed of the multiplier is always an important constraint and it determines the performance of the multipliers. For meeting such a demand the number of steps in the multiplication process must be reduced. To increase the efficiency of doing the multiplication process, in this project we have used the Vedic which glorify the richness of our Indian traditions. Vedic mathematics is the name given to the ancient system of mathematics, or, to be precise, a unique technique of calculations based on simple rules and principles with which any mathematical problem can be solved. It includes arithmetic, algebra, geometry or trigonometry problems too.

II. VEDIC MATHEMATICS SUTRAS

A. Ekanyunena purvena

The Sutra Ekanyunena purvena comes as a Sub-sutra to Nikhilam which gives the meaning 'One less than the previous' or 'One less than the one before'.It is used for multiplying the numbers having 9's as their multiplier.To illustrate this scheme, let us consider the multiplication of two decimal numbers 70 and 99 by Ekanyunena Purvena method as shown below in figure 1.

Step 1:

70-1=69

Step 2:

99-69=30

The answer is **6930**

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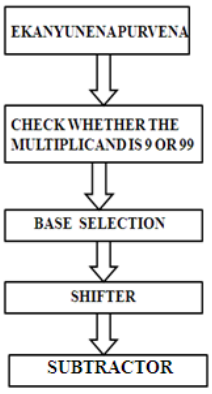

Figure 1: Flow Diagram of Ekanyunena Purvena

The Figure 1 shows the logical implementation of the Ekanyunena Purvena. The inputs from control unit are given to arithmetic unit to check whether the multiplier is 9 or 99. Then the base is selected in Base selection unit. Then the shifter shifts the Multiplicand based on the base selected and the subtractor subtracts the multiplicand from the base.

B. Anurupyena

The upa-Sutra 'anurupyena' means 'proportionality'. This Sutra is highly useful to find products of two numbers when both of them are near the Common bases i.e powers of base 10. It is very clear that in such cases the expected 'Simplicity ' in doing problems is absent. To illustrate this scheme,

let us consider the multiplication of two decimal numbers 46 and 43 by Anurupyena method as shown below in figure 2.

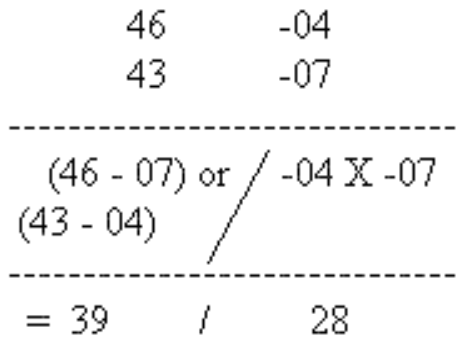

Figure 2: Example for Anurupyena

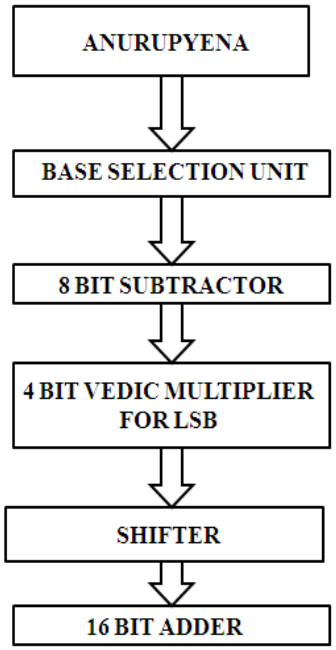

Figure 3: Flow Diagram of Anurupyena

The figure 3 shows the flow diagram of implementing Anurupyena Sutra. The Base Selection Unit selects the nearest whole number. For example if the multiplicand is 43 then the base chosen is 50. Then the subtractor is used to retrieve the least significant bits. Then the multiplier is used to multiply the least significant bits retrieved. The Shifter is used to shift the subtracted bits then it is added to the multiplied LSB.

C. Antyayor Dasakepi

The Sutra signifies numbers of which the last digits added up to give 10. i.e. the Sutra works in multiplication of numbers for example: 25 and 25, 47 and 43, 62 and 68, 116 and 114. Note that in each case the sum of the last digit of first number to the last digit of second number is 10. Further the portion of digits or numbers left wards to the last digits remain the same. To illustrate this scheme, let us consider the multiplication of two decimal numbers 47 and 43 by Antyayor Dasakepi method as shown below.

Example:

47 x 43 = (4 + 1) x 4 | 7 x 3

= 20 | 21

= 2021.

Generally:

AB*AC= (A+1) A | B*C

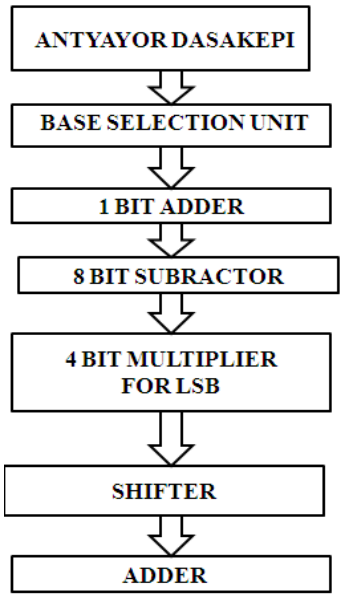

Figure 4: Flow Diagram of Antyayor Dasakepi

The figure 4 shows the flow diagram of implementing Antyayor Dasakepi Sutra. The Base Selection Unit selects the nearest whole number. For example if the multiplicand is 43 then the base chosen is 50. The adder adds 1 to the MSB.Then the operation is similar to that of the Anurupyena.

D. Urdhva Tiryagbhyam

Urdhva – tiryagbhyam is the general formula applicable to all cases of multiplication and also in the division of a large number by another large number. An example for 3 bit Urdhva multiplication and 4 bit multiplication are shown in figures 5 and 6 respectively.

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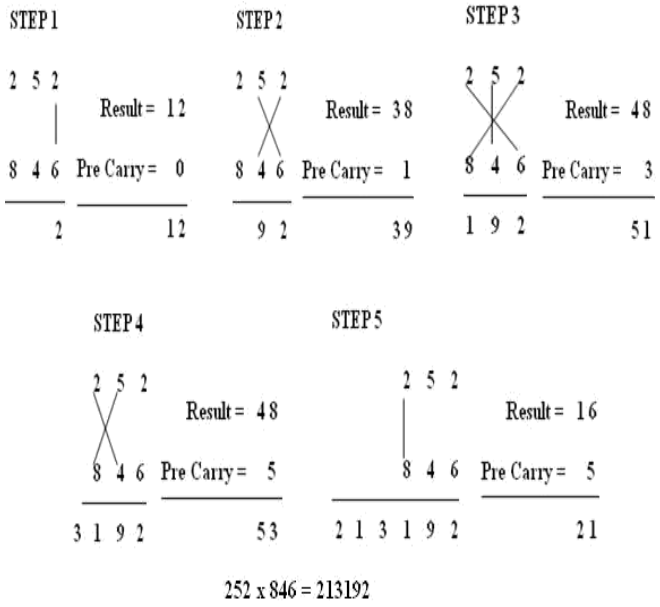

Figure 5: 3 bit Multiplication

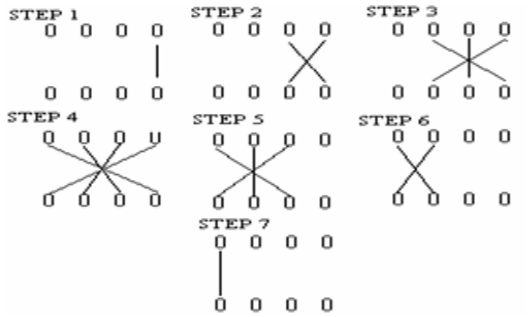

Figure 6: 4 bit Multiplication

1) *Multiplier for 2*2*

The 2x2 bit Vedic multiplier (VM) module is implemented using four input AND gates & two half-adders which is displayed in Figure 7.

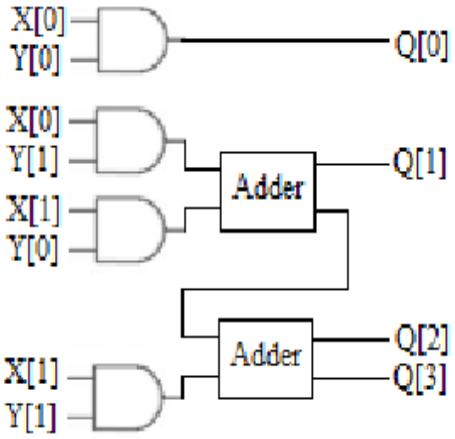

Figure 7: 2*2 Vedic Multiplier using Urdhva Tiryagbhyam

2) *Multiplier for 4*4*

The 4*4 bit Vedic multiplier (VM) module is implemented using four 2*2 Vedic multiplier unit, three 4 bit ripple carry adders & one OR gate which is shown in the figure 8.

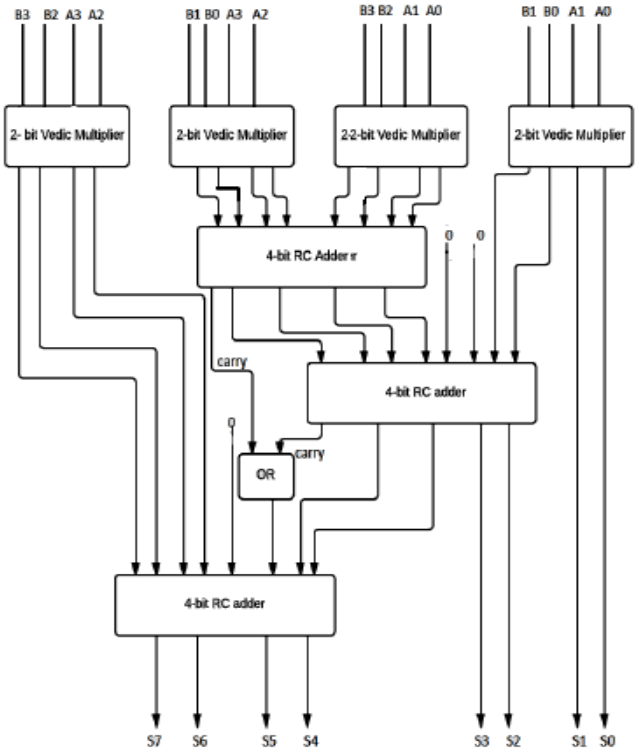

Figure 8: 4*4 Vedic Multiplier using Urdhva Tiryagbhyam

3) *Multiplier for 8*8*

The 8*8 bit Vedic multiplier module is implemented using four 4*4 Vedic multiplier unit, three 8 bit ripple carry adders & one OR gate which is the same as that of the above figure 8.

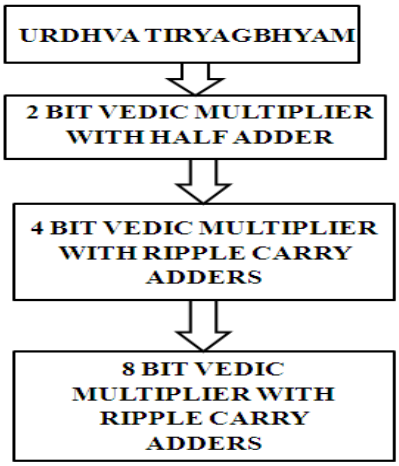

Figure 9: Flow Diagram using Urdhva Tiryagbhyam

The figure 9 shows the flow diagram for implementing Urdhva Tiryagbhyam Sutra. This sutra

is implemented for 8*8 by using 4*4 which in turn is implemented using 2*2.

III.PROPOSED VEDIC MULTIPLIER ARCHITECTURE

Control Unit

The proposed design of the multiplier is using all these four Sutras by adaptively using these Sutras to obtain the Product term in minimum delay with optimum area. The simple Block Diagram which depicts the logic is shown below in figure 10.

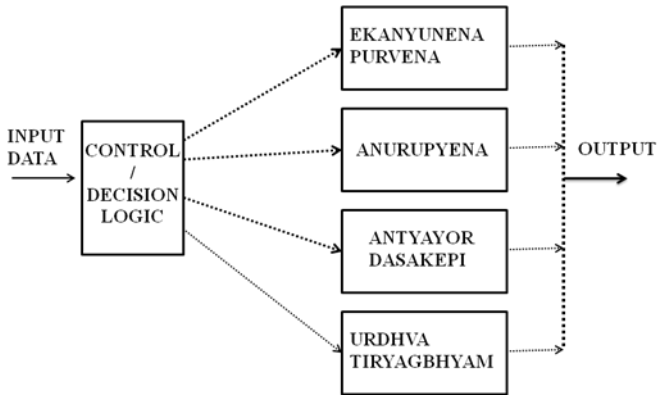

Figure 10: Basic Block Diagram

The proposed Vedic Multiplier uses an eight bit multiplicand and an 8 bit multiplier which is given as an input to the Control unit. The Control unit gets the input and decides which sutra is to be used. It decides adaptively. The product term is computed by any one of the sutras.

CONTROL UNIT

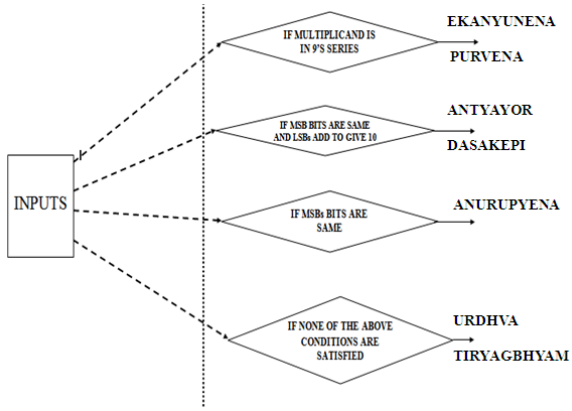

Figure 11: Control Unit

The Control Unit in figure 11 is an intelligent unit which determines when the multiplier is in 9's series then the inputs are forwarded to Ekanyunena Purvena unit. When the MSBs are same then the inputs are fed to the Anurupyena unit. When the inputs are same and the LSBs add to give 10 then the inputs are given to Antyayor Dasakepi unit. When none of the above conditions are satisfied the inputs are forwarded to Urdhva Tiryagbhyam unit. The product term arrives from any one of the arithmetic block.

IV. IMPLEMENTATION RESULTS

In this work, 8*8 bit VM (Vedic multiplier) using "Urdhva Tiryakbhyam" Sutra, "Ekanyunena Purvena" Sutra, "Anurupyena" Sutra and "Antyayor Dasakepi" Sutra and is implemented in Verilog. Simulation was done using Modelsim and Logic Synthesis was observed using ISE Design Suite and implemented in Xilinx Spartans 6. Table 1 displays the comparison of synthesis results of various multipliers in terms of time delay (in nanoseconds).

Table 1 Comparison of Multipliers (in nanosecond)

MULTIPLIERS *[8]*	**DELAY(ns)**
Booth Multiplier	**29.549**
Wallace Tree Multiplier	**25.923**
Array Multiplier	**32.01**
Dadda Multiplier	**20.171**

Table 2 displays the comparison of synthesis results of multipliers using various sutras in terms of time delay (in nanoseconds).

Table 2 Comparison of Vedic Sutras (in nanosecond)

MULTIPLIERS	**DELAY(ns)**	**No. of Slices LUT**
Urdhva Tiryagbhyam	**17.516**	**109**
Ekanyunena Purvena	**9.382**	**14**
Anurupyena	**13.691**	**152**
Antyayor Dasakepi	**11.790**	**149**

In behavioral simulation we have tested for input bits: - "10101010" (in decimal number system 170) and "01100011" (decimal number system 99) as inputs and we get output as"100000110111110" (decimal number system 16830) which invokes Ekanyunena Purvena. For input"10011001" (decimal number system 153) and "10011101" (decimal number system 157) we get the output as"101110111010101" (decimal number system 24021) which invokes Antyayor Dasakepi. For input"1101011" (decimal number system 107) and "1101101" (decimal number system 109) we get the output as"10110110001111" (decimal number system 11663) which selects Anurupyena. For input"1111100" (decimal number system 124) and "10011111" (decimal number system 159) we get the output as"100110100000100" (decimal number system 19716) which selects Urdhva Tiryagbhyam.

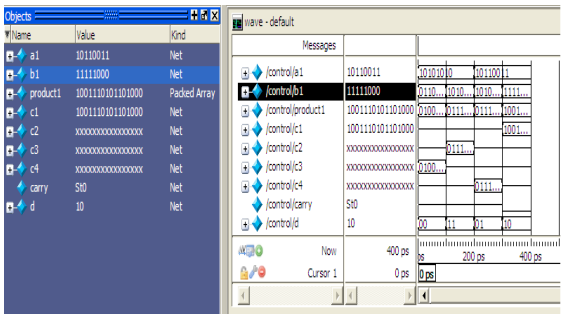

Figure 12: Simulation Result

V. CONCLUSION

This paper presents a new method of multiplication using "Ekanyunena Purvena", "Anurupyena", "Antyayor Dasakepi" and "Urdhva Tiryagbhyam" Sutra based Vedic Multiplier. The design of the proposed 8*8 bit Vedic multiplier is implemented on Spartan xc6slx16-3ftg256 device. The computational path delay of the Vedic multiplier is ound to be 17.59ns. Hence it can be concluded that the performance of the proposed 8*8 bit Vedic multiplier seems to be highly efficient in terms of speed when compared to Conventional multiplier methods. Reducing the time delay is very essential requirement for many applications and Vedic Multiplication technique is very much suitable for this purpose. The idea proposed here may set path for future research in this direction.

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